First Self-Consistent Full-Band 2D Monte Carlo 2D Poisson Device Solver for Modeling SiGe Heterojunction *p*-Channel Devices

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***Abstract*— In this work we are concerned with proper calculation of the valence band-structure of Si and strained SiGe material systems. The hole band-structure is complicated by the strong anisotropy, nonparabolicity and warping of the heavy-hole and light-hole bands. As the spin-orbit splitting is about 44.2 (296) meV in Si (Ge), one also needs to take the split-off band into account to account for inter and intra-band scattering events to model transport properly. Thus, ignoring the contribution of the distant conduction bands in Si, one has to consider at the very minimum six bands (the heavy-hole, the light hole and the split-off bands multiplied by 2 due to spin degeneracy).**

key words: SiGe devices, strain, particle-based device simulations

I. INTRODUCTION

For digital circuits, a figure of merit for MOSFETs for unloaded circuits is CV/I, where C is the gate capacitance, V is the voltage swing, and I is the current drive of the MOSFET. For loaded circuits, the current drive of the MOSFET is of paramount importance. Keeping in mind both the CV/I metric and the benefits of a large current drive, we note that device performance may be improved by: (1) inducing a larger charge density for a given gate voltage drive; (2) enhancing the carrier transport by improving the mobility, saturation velocity, or ballistic transport; (3) ensuring device scalability to achieve a shorter channel length; and (4) reducing parasitic capacitances and parasitic resistances. For capitalizing these opportunities, the proposed technology options generally fall into two categories: new materials and new device structures. In many cases, the introduction of a new material requires the use of a new device structure, or vice versa. To fabricate devices beyond current scaling limits, IC companies are simultaneously pushing the planar, bulk silicon CMOS design while exploring alternative gate stack materials (high-*k* dielectric and metal gates), band engineering methods (using strained Si [1,2,3] or SiGe), and alternative transistor structures. The concept of a band-engineered transistor is to enhance the mobility of electrons and/or holes in the channel by modifying the band structure of silicon in the channel in a way such that the physical structure of the transistor remains substantially unchanged. This enhanced mobility increases the transistor transconductance (g_m) and on-drive current (I_{on}). A SiGe layer or a strained-silicon on relaxed SiGe layer is used as the enhanced-mobility channel layer. It has already been demonstrated experimentally that at T = 300 K (room temperature), effective hole enhancement of about 50% can be achieved using the SiGe technology [4]. Intel has adopted strained silicon technology for its 90 nm process [5]. The results were nearly a 20% performance improvement, with only a few additional process steps.

II. SIGE TECHNOLOGY

The performance of *n*- and *p*-MOS transistors are strongly asymmetric because the electron mobility is much higher than the hole mobility in silicon. To improve *p*-MOSFET performance and reduce this asymmetry, various heterostructure devices with SiGe-layers have been proposed to improve the hole mobility [6]. The most promising method for improving *p*-MOSFET performance is through the use of a strained SiGe-layer grown on relaxed or bulk Si because this does not require a thick relaxed SiGe buffer layer which is expensive and difficult to process.

It is imperative to review the effect of strain on the electronic band-structures of SiGe before we explore the design of the SiGe heterostructure devices. When a thin SiGe film is pseudomorphically grown on Si, it experiences biaxial compressive strain. The HH and LH bands in strained-SiGe become non-degenerate at the Γ point. In addition, the existence of biaxial compressive strain in the $Si_{1-x}Ge_x$ film couples the HH and LH bands and introduces band-mixing which reduces the effective mass in the top-most HH band. Consequently, the hole mobility in compressively-strained SiGe is increased. By introducing 30% Ge in the pseudomorphic layer, the in-plane mobility is expected to be enhanced by more than 33% [7]. Figure 1 (a) shows the design of a thin-body transistor with a graded $Si_{1-x}Ge_x$ heterostructure channel.

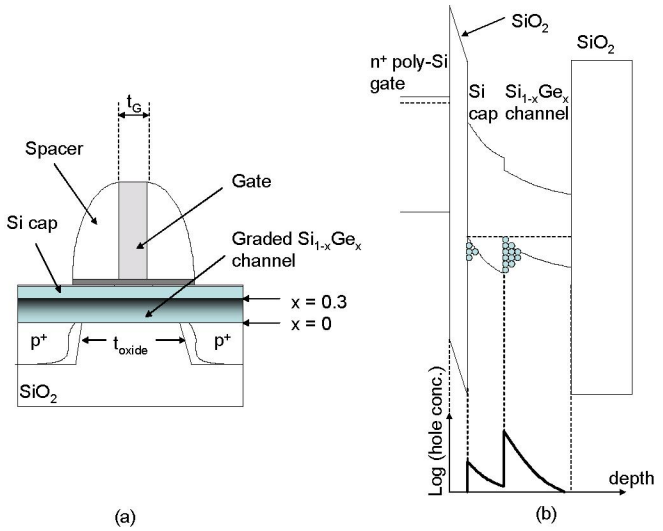

Figure 1. (a) Cross section of a thin-body transistor with a SiGe heterostructure channel. The energy band diagram along the center portion of the device is shown in (b). Most of the holes in the inversion layer are found in the SiGe layer.

The Ge mole fraction is graded from 0 to 0.3 (bottom-to-top) in the 15-nm thick $Si_{1-x}Ge_x$ layer. The energy-band diagram along the device cross section is shown in Figure 1 (b). The top Si cap layer has a thickness of 4 nm and serves to provide a good Si/SiO_2 interface quality. Nearly all of the band-gap difference between $Si_{1-x}Ge_x$ and Si appears at the valence band. As a result, the majority of the holes are confined in the SiGe-channel where the mobility is enhanced [Figure 1 (b)]. The carrier profile under a typical inversion bias is schematically shown below the energy band diagram.

By integrating the charge density over the regions of the Si-cap and the SiGe-channel, one can determine the ratio of the amount of charge in the SiGe-channel to that in the parasitic Si-channel (Si-cap). It is advantageous to ensure that this ratio is larger than unity in the operation regime of the transistor so that most of the holes are in the high-mobility SiGe layer. There is a gate voltage, $V_{G,Si\text{-}cap}$, above which the parasitic surface Si-channel contains more carriers than the SiGe-channel. Thus, at $V_G = V_{G,Si\text{-}cap}$, the total integrated charge density in the SiGe-channel is equal to that in the Si-cap. Parameters which are critical in determining $V_{G,Si\text{-}cap}$ include the relative thicknesses of the gate oxide, the thickness of the SiGe layer, and the Ge mole fraction of the SiGe layer. A larger Ge mole fraction and band offset at the Si/SiGe interface results in better hole confinement, but strain relaxation issues set the upper limit on the mole fraction of Ge that can be incorporated. Other innovative approaches have also been suggested. These include the use of Schottky source/drain *p*-MOSFETs with a SiGe channel [8], use of double SiGe heterostructures to increase strain in surface channel strained Si p-MOSFETs [9], incorporation of a SiGe channel with a graded Ge concentration along the depth, as well as SSOI and SGOI structures (strained Si on Insulator and strained SiGe on Insulator).

III. Description of the Simulator Developed

This work presents a novel approach to model hole transport in *p*–channel Metal – Oxide – Semiconductor - Field – Effect – Transistors (MOSFETs). In this approach, a full band Monte Carlo technique has been employed to investigate hole transport and band-structure effects are incorporated by using a six band model, thereby giving an accurate picture of the coupling between the heavy-hole, light-hole and the split-off bands. Carriers in the source and drain regions are treated as quasi-3D like particles while the effect of the confining potential under the gate is included by self-consistently coupling the Poisson-the six band solver and the Monte Carlo transport kernel in the device simulator. All relevant scattering mechanisms were incorporated including acoustic and optical phonon scattering (within the isotropic approximation), surface roughness scattering as well as Coulomb scattering. For the case of the strained SiGe MOSFET, alloy scattering was included in the transport model. Self-consistent device simulation of hole transport in a 25 nm p-channel Si MOSFET confirm the obvious fact of the increasing impact of surface roughness scattering on the device performance at higher gate bias. The performance enhancement expected by using strained SiGe devices in place of conventional Si devices was investigated. The performance enhancement in terms of drive current enhancement was found to be higher at smaller values of drain voltage corresponding to the low field regime in which mobility enhancement is expected for such structures. At higher gate and drain biases, the performance of the strained SiGe MOSFET with respect to the conventional Si MOSFET degrades. The full potential of this approach will be realized when a host of device technologies will be investigated by making relatively minor modifications to the code. This will aid in the design and technology aspects of *p*-channel MOSFETs.

IV. Simulation Results

The output characteristics of a 25 nm *p*-channel conventional Si MOSFET are shown in Figure 2 (top panel). Significant DIBL and short channel effects are seen in the output characteristics in this case. It should be noted that the device under consideration has not been optimized but is merely a prototypical structure on which we have tested our simulator. The device transfer characteristics calculated at a drain voltage of -50 mV are shown in the bottom panel of Figure 2. The threshold voltage of the device is determined to be -0.8 V. The device exhibits a peak transconductance of ~175 μS/μm. The roll-off of the drain current at higher gate voltages is due to the increased surface roughness scattering that holes experience as they are confined closer to the $Si\text{-}SiO_2$ interface.

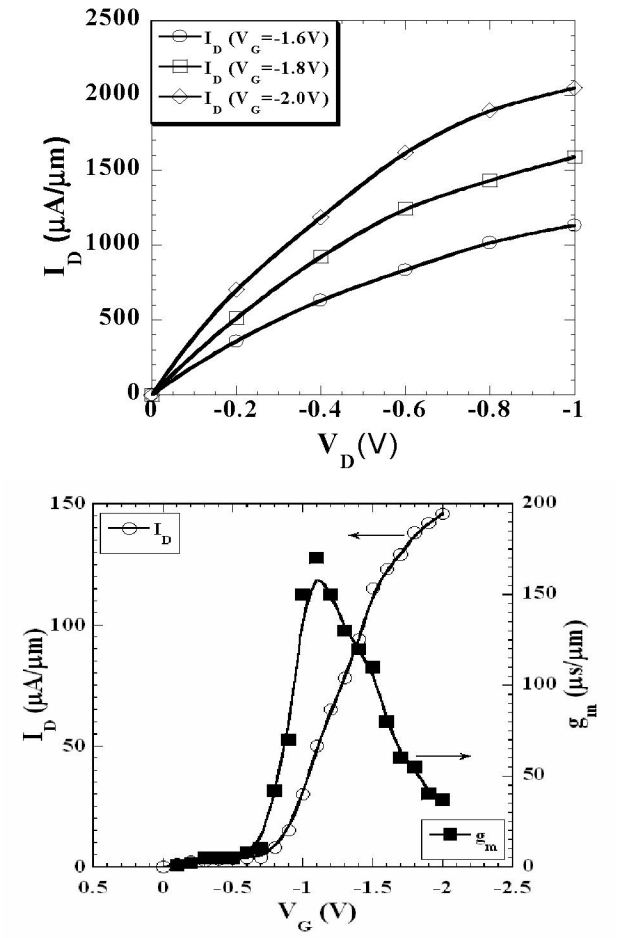

Figure 2. Top panel - Output characteristics of the 25 nm *p*-channel MOSFET. The gate oxide thickness is 1.2 nm. Bottom panel - Transfer Characteristics of the 25 nm *p*-channel MOSFET.

The output characteristics of a 25 nm *p*-channel strained SiGe MOSFET are shown in the top panel of Figure 3. Just as in the conventional MOSFET, significant DIBL and short channel effects are seen in the output characteristics. The strained SiGe MOSFET has a threshold voltage difference with respect to the conventional Si MOSFET of about 0.22 V. This is not unexpected since the strained SiGe MOSFET has the carriers confined in the strained SiGe quantum well and the valence band-offset of 0.254 eV means that the strained SiGe device can be driven into inversion at a lesser value of gate voltage than the conventional Si MOSFET. The transfer characteristics of this device, calculated at a drain voltage of -50 mV, are shown in the bottom panel of Figure 3. The threshold voltage of the device is determined to be -0.58 V. The device exhibits a peak transconductance of ~220μS/μm. Thus, the enhancement in transconductance of the strained SiGe MOSFET over the Si MOSFET is about 26%. The roll-off of the drain current at higher gate voltages is due to the increased surface roughness scattering that holes experience as they spill over from the strained SiGe quantum well into the Si cap region.

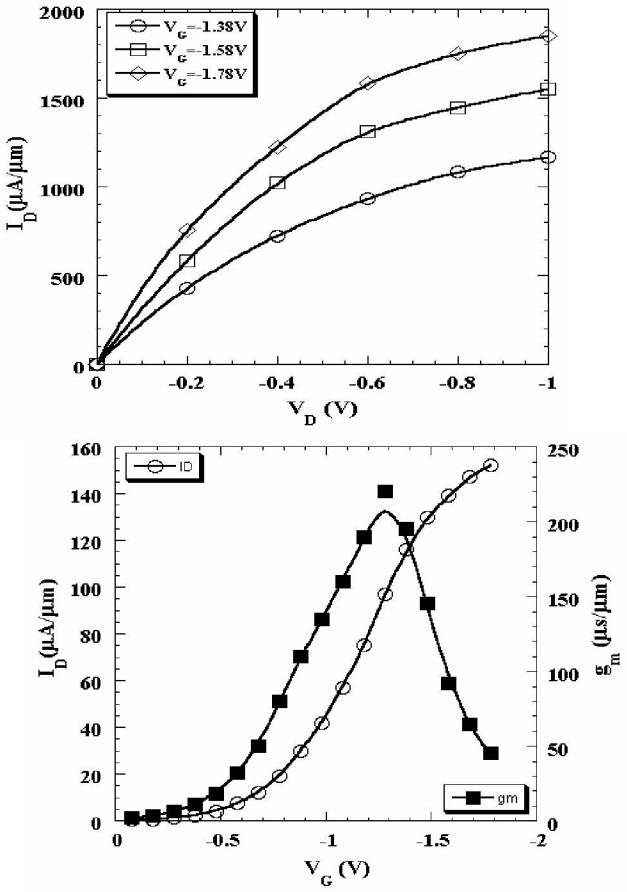

Figure 3. Top panel - Output characteristics of the 25 nm *p*-channel strained SiGe MOSFET. Bottom panel - Transfer characteristics of the 25 nm *p*-channel strained SiGe MOSFET.

The drain current enhancement ratio of the strained SiGe MOSFET over the conventional Si MOSFET as a function of the applied drain bias for different gate voltages is shown in Figure 4. It is seen that:

1. The peak enhancement comes at low values of drain bias, in the low-field transport regime. As the drain voltage and hence the electric field increases, the current enhancement ratio drops: meaning that the performance of the Si *p*-channel MOSFET device is comparable to that of the strained SiGe MOSFET. Put differently, the performance of the strained SiGe MOSFET worsens as the drain bias increases, performing just as badly as the conventional Si device.
2. As the gate voltage increases, the current enhancement drops. This can be explained in the following manner: Increasing the gate voltage increases the surface electric field, pulling the carriers closer to the Si-SiO_2 interface and thereby causing the carriers to experience greater surface roughness scattering. At still higher values of gate voltage, the carriers spill over from the quantum well into the Si cap region and the device performance degrades even further.

3. Thus, it is seen that the SiGe MOSFET clearly performs better than the conventional Si MOSFET at low values of applied drain bias (low field regime) and moderate values of the gate voltage. This is the regime in which the hole mobility enhancement is predicted for device structures using a strained SiGe layer as the active layer for carrier transport.

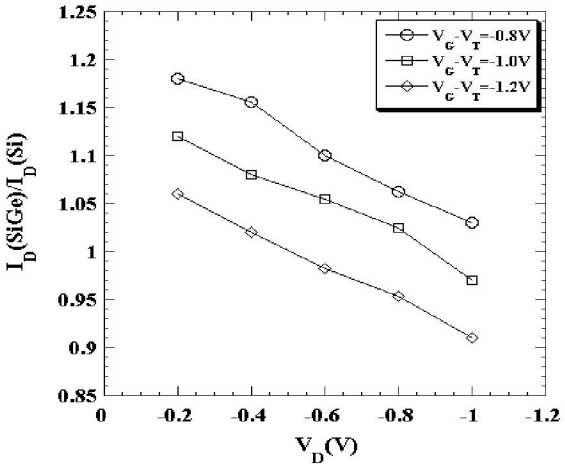

Figure 4. Drain current enhancement of the strained SiGe MOSFET over the conventional Si MOSFET.

CONCLUSIONS

In summary, this work has presented a novel way of incorporating band-structure and quantum effects on hole transport in *p*-channel MOSFETs. In this approach, a full band Monte Carlo technique has been employed to investigate hole transport and the effect of valence band-structure on transport probed using a six band k.p model giving an accurate picture of the coupling between the heavy-hole, light-hole and the split-off bands. Further, within the scope of this approach, for lack of an accurate and computationally feasible and a reasonably fast method to incorporate open boundary conditions to model the contacts, carriers in the source and drain regions are treated as quasi-3D like particles with the band-structure information obtained by solving for the eigenstates of the more compact six band k.p Hamiltonian proposed initially by Dresselhaus, Kip and Kittel. The effect of carrier spatial confinement in the channel (along the depth direction) due to the confining potential under the gate is included by self-consistently coupling the Poisson, the discretized six band k.p solver and the Monte Carlo transport kernel in the device simulator. The results showed that the drive current performance of the strained SiGe MOSFET and the conventional Si MOSFET were comparable at the same normalized gate voltages (V_G-V_T) at moderate and high values of drain bias. In fact the drive current enhancement ratio I_D(SiGe)/ I_D(Si) is lower than 1.0 at high values of V_D ~ 0.8-1.0V, meaning that the expectation of performance enhancement expected out of the strained SiGe MOSFET is misplaced.

Having obtained simulation results of investigations on hole transport by incorporating band-structure effects into the Monte Carlo transport kernel, the direction for future work in this area is now detailed. Obtaining these preliminary results of effects of strain on the valence band-structure is a start in investigating hole transport in other strained heterostructure MOSFETs. The approach that was adopted to incorporate band-structure effects for the case of a *p*-channel MOSFET is versatile as it can allow one to probe hole transport in *p*-channel devices of alternate device technologies as well. This includes technologies like Surface channel strained Si, Strained Si on Insulator (SSOI), Strained SiGe on Insulator (SGOI), among others. Other device technologies that can be investigated are related more to conventional Si MOSFET but involving interesting MOSFET structures such as double gate MOSFETs, finFETs etc.

In summary, the major contribution of this work is a novel way of the inclusion of band-structure effects on hole transport in *p*-channel MOSFETs within the Monte Carlo framework self consistently. The basic framework of the method and the approach exists and has been tested. Modifying this approach would entail relatively minor changes to simulate different devices. This approach can then be rigorously tested against different device technologies and contribute significantly as a predictive tool in the design and technology aspects of strained heterostructure *p*-channel MOSFETs..

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REFERENCES

[1] Welser, J. L. Hoyt and J. F. Gibbons, "NMOS and PMOS transistors fabricated in strained silicon/relaxed silicon-germanium structures", *IEDM Tech. Dig.*, 1992, pp. 1000-1002.

[2] G. Formicone, D. Vasileska, D.K. Ferry, "2D Monte Carlo simulation of hole and electron transport in strained Si", VLSI Design, Vol. 6, pp. 167-171, 1998.

[3] D. Vasileska, G. Formicone and D.K. Ferry, "Doping dependence of the mobility enhancement in surface-channel strained-Si layers", *Nanotechnology,* Vol. 10, pp. 147 -152, 1999.

[4] P. M. Garone, V. Venkataraman, and J. C. Sturm, "Hole mobility enhancement in MOS-gated Ge_xSi_{1-x}/Si heterostructure inversion layers, *IEEE Electron Device Lett.* Vol. 13, pp. 56-58, 1992.

[5] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P.Smith, K. Zawadzki, S. Thompson and M. Bohr, "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors", *IEDM Tech. Digest*, 2003, pp. 978-980.

[6] F. Schäffler, "High mobility Si and Ge structures", *Semicond. Sci. Technol.*, Vol. 12, no. 12, pp. 1515 –1549, 1997.

[7] C. Jungemann, S. Keith, and B. Meinerzhagen, "Full-band Monte Carlo simulation of a 0.12 μm Si-PMOSFET with and without a strained SiGe-channel", in *IEDM Tech. Dig.*, 1998, pp. 897–900.

[8] K. Ikeda,. Y. Yamashita, A. Endoh, T. Fukano, K. Hikosaka,T. Mimura, "50-nm gate Schottky source/drain p-MOSFETs with a SiGe channel", *IEEE Electron Device Lett.*, Vol. 23, pp.670-672, 2002.

[9] T. Mizuno, N. Sugiyama, T. Tezuka, S. Takagi, "Novel SOI p-channel MOSFETs with higher strain in si channel using double SiGe heterostructures", *IEEE Electron Device Lett.*, Vol. 49, no. 1, pp. 7- 14, 2002.