Theory of Fermi Level Pinning of High-k Dielectrics

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***Abstract*— Fermi-level pinning of poly-Si and metal-silicide gate materials on Hf-based gate dielectrics has been systematically studied theoretically. Fermi-level pinning in high-work-function materials is governed by the O vacancy generation and subsequent formation of interface dipoles near gate electrodes due to the electron transfer. On the other hand, O interstitial formation plays a crucial role for Fermi-level pinning in low-work-function materials. From our theoretical considerations, we have found that the work-function pinning-free-region generally appears due the difference in the mechanism of Fermi-level pinning of high- and low-work-function materials. The widening of this work-function pinning-free-region is the key issue for the fundamental relaxation of Fermi-level pinning in high-k gate dielectric.**

Keywords-component; Fermi-level pinning; poly-Si gates; metal silicide gates; O vacancy; O interstitial; high-k dielectrics; interface dipoles; theory; flatband voltage shift

I. INTRODUCTION

The aggressive downscaling of Si devices has required a continuing need for significant reduction in gate dielectric film thickness, and even current commercial based large scale integrated (LSI) circuits have SiO_2-related dielectrics with less than 2nm thickness. As a result, increasing gate leakage current has become a serious issue for future LSI devices. Efforts to reduce the leakage current have given rise to the application of alternative high-*k* gate dielectrics, which are still being studied intensively. Among these, HfO_2 and its related alloys ($HfSiO_x$, HfSiON), have attracted much attentions due to their promising properties such as their thermal stabilities when they are in contact with Si and sufficiently large band offset values for both electrons and holes [1,2]. Although Hf-based dielectrics have been studied intensively, many obstacles still remain. One of them is the difficulty in controlling the effective work functions (Φ_{Meff}) of gate materials.

The Φ_{Meff} of gate electrodes on Hf-based high-k dielectrics reveals unusual behaviors that are much different from those both in vacuum and on SiO_2: Conventional poly-Si gates reveal Fermi-level pinning. The effective work-function difference between n+ and p+poly-Si gates is only about 0.2 eV in Hf-related high-*k* gate stacks [3]. Typical CV curves are given in Fig. 1. The Fermi level of p+poly-Si elevates by about 0.6 eV, whereas that of n+poly-Si decreases by about 0.2 eV. As a result, the difference in Fermi-levels of n+ and p+poly-Si gates becomes only 0.2 eV and this small Fermi-level difference makes it difficult to construct CMOS. Fermi-level pinning is also observed in metal silicide gates [4]; Fermi levels of n-like metal silicides are usually located between the pinning position of n+ and p+poly Si gates, and those of p-like metal silicides are located near the pinning position of p+poly-Si gates. The schematic view of Fermi level pinning of various gate materials is described in Fig.2.

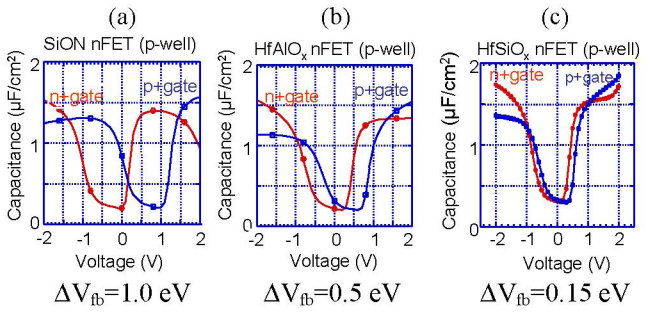

Fig.1: C-V characteristics of SiON, $HfAlO_x$, and $HfSiO_x$ dielectrics.

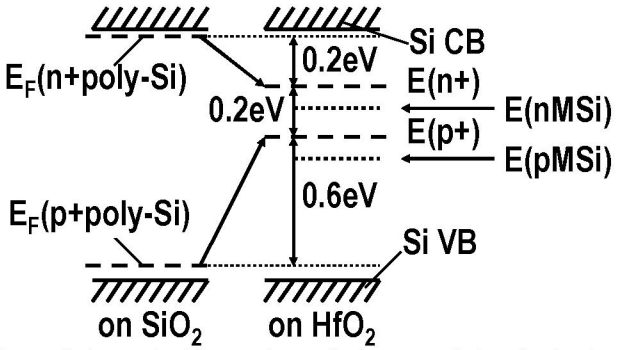

Fig.2: Schematic illustration of the Fermi level pinning observed in poly-Si and n-like MSix gates. E(n+), E(p+), E(nMSi), and E(pMSi) are the pinning positions of n+ and p+ poly-Si, and n- and p-like metal silicide gates

In this study, we systematically investigate the above Femi level pinning by carefully considering the interface reaction between gate electrodes and high-k dielectrics, and clarify the microscopic origin of Fermi-level pinning on high-k dielectrics.

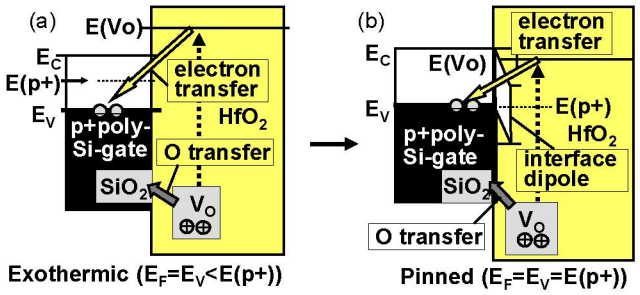

Fig.3: Schematic illustration of the mechanism of Fermi-level pinning in p+poly-Si gates.

II. Fermi-Level Pinning of Poly-Si Gates

Since Fermi-level pinning of poly-Si gates is mainly due to the significant flat band voltage (V_{fb}) or the threshold voltage (V_{th}) shifts of p+poly-Si gates, the mechanism of Fermi level pinning of p+poly-Si gates has been intensively studied. For example, interfacial Hf-Si bonds (interfacial Hf-Si bond model) [3] and a B-dopant induced flat band (V_{fb}) shift (B-dopant model) [5, 6] have been proposed as possible mechanisms. Further, we have proposed that oxygen vacancies (Vos) in ionic Hf based high-*k* dielectrics is the cause of large V_{fb} shifts based on an estimation of the Vo induced interface dipoles (oxygen vacancy model) [7-9]. Although the pinning mechanism of n+poly-Si gates has not been intensively studied because the shift of Femi-level is much smaller compared with p+poly-Si gates, we have recently proposed that O interstitial (Io) formation in Hf-based high-k dielectrics are the main cause of n+pinning (oxygen interstitial model) [10]. In this section, we combine our "oxygen vacancy model" with "oxygen interstitial model", and construct a unified theory of Fermi-level pinning of poly-Si gates that includes interfacial reaction accompanied with O and electron transfer across the interface.

Schematic illustration of the mechanism of Fermi-level pinning in p+poly-Si gates is given in Fig. 3. As shown in this figure, the interface reaction that includes Vo formation in HfO_2 accompanied with partial oxidation of poly-Si gates and subsequent electron transfer from Vo level in HfO_2 to Fermi level of p+poly-Si gates, is exothermic due to the large energy gain of electron transfer, although Hf can bind much stronger to O than Si. Above key interface reaction is described as the following reaction equations.

$$\tfrac{1}{2}Si + (HfO_2) \rightarrow \tfrac{1}{2}SiO_2 + (HfO_2) + Vo^{2+} + 2e \qquad (1)$$

Equation (1) contains energy loss of O transport from HfO_2 to poly-Si gates,

$$\tfrac{1}{2}Si + (HfO_2) \rightarrow \tfrac{1}{2}SiO_2 + (HfO_2) + Vo^{0} - \Delta G_1, \qquad (2)$$

and energy gain of electron transfer

$$Vo^{0} + (HfO_2) \rightarrow Vo^{2+} + (HfO_2) + 2e + \Delta G_2. \qquad (3)$$

ΔG_1 can be estimated by the first principles total energy calculations. By combining the Vo formation energy in HfO_2

(6.3 eV) and SiO_2 formation energy (9.4 eV), ΔG_1 is estimated as 1.6 eV. ΔG_2 can also be estimated by using the recent experimental results. Since the position of Vo level is located 0.4 eV above Si conduction band by the spectroscopic ellipsometry experiments [11], energy gain of two electron transfer ΔG_2 is given as

$$\Delta G_2 = 0.8 + 2x, \qquad (4)$$

where x is the Fermi-level position of a poly-Si gate measured from the conduction band bottom of Si. Since the Fermi-level position of p+poly-Si gates corresponds to x=1.1, ΔG_2 becomes 3.0 eV for p+poly-Si gates. As a result, total energy gain of the considering interface reaction $\Delta G_{total}(x)$ ($=\Delta G_1 + \Delta G_2 = -0.8+2x$) is 1.4 eV for p+poly-Si gates (exothermic). Thus, the considering interface reaction occurs for p+poly-Si gates and interface dipoles due to the electron transfer from Vo in HfO_2 to poly-Si gates are generated (Fig. 3(b)). On the other hand, the considering reaction does not occur in n+poly-Si gates (x=0), since $\Delta G_{total}(x)$ becomes −0.8 eV (endothermic).

In p+poly-Si gates, Fermi-level elevates as the interface reaction proceeds due to the electron transfer. The elevation of Fermi-level decreases energy gain of the above interface reaction, and our considering interface reaction stops when the total energy gain $\Delta G_{total}(x)$ becomes zero. This condition is described by $-0.8 + 2x = 0$. Thus, Fermi-level should be pinned by the equilibrium condition of interface reaction, and the pinning position is located about 0.4 eV below Si conduction band bottom (x=0.4) in good agreement with experiments. As discussed above, Fermi-level pinning of p+poly-Si gates can naturally explained by considering the thermal equilibrium condition of the interface reactions that include O and electron transfer across the interface. The key point of our mechanism is interface reaction. Thus, we performed the transmission electron microscope (TEM) observation to confirm the interface reactions. As shown in Fig. 4, our TEM image clearly indicates the existence of some interfacial reaction layers in a p+poly-Si gate Hf-based high-k MISFET. Further, such reaction layers have not been observed in n+poly-Si gate MISFETs [7-9]. These experimental results finely corroborate the finding of our investigations.

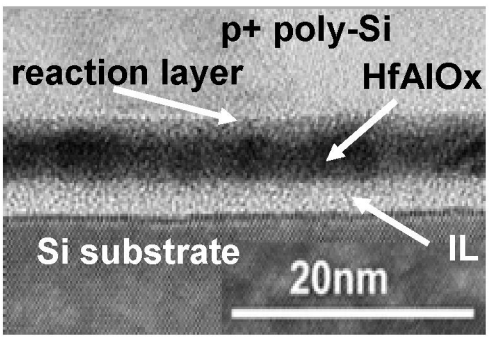

Fig.4: Cross section of replacemnt p+gate $HfAlO_x$ MISFET observed by TEM.

As far as I know, interface reaction-induced Fermi level pinning has not been proposed in the field of interface physics, although other pinning mechanisms such as interface state induced pinning have been proposed. Thus, our proposed model gives a new insight to interface physics as well as to the high-k technologies in modern LSI fields.

Next, we investigate the mechanism of Fermi-level pinning of n+poly-Si gates [10]. Before considering n+pinning, it is convenient to reconsider the p+pinning mechanism from another view point. In Fig. 5, we show another aspect of p+pinning: In thermal equilibrium condition that is equivalent to the p+pinning situation, Vo generation reaction and Vo annihilation reaction should be balanced.

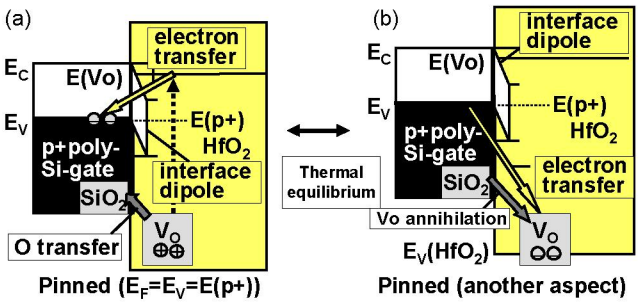

Fig. 5: Another understanding of the Fermi-level pinning of p+poly-Si gates. Vo generation and annihilation reaction are balanced.

Now, we turn to discuss the mechanism of Fermi-level pinning of n+poly-Si gates. Poly-Si films are deposited conventionally by low-pressure chemical vapor deposition (LPCVD) and typically have significant O concentration ~10^{18} cm^{-3} [12]. This means that poly-Si films contain excess O atoms. As a result, SiO_2 can be formed near the interface between a poly-Si gate electrode and a high-k gate-dielectric, during device fabrication as schematically described in Fig. 6.

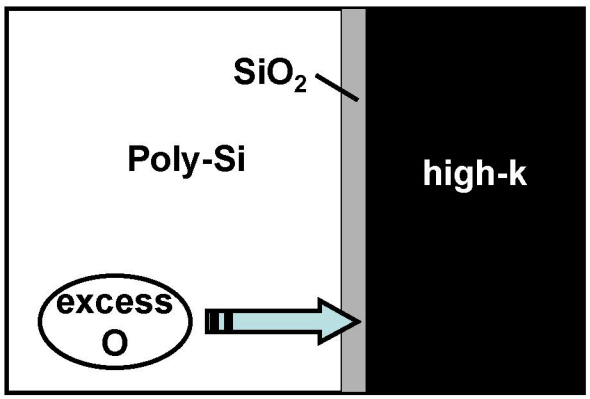

Fig. 6: Schematic illustration of the slight oxidation of the interface between poly-Si and a high-k dielectric by excess O in the poly-Si.

As discussed in the p+pinning mechanism, Vo formation does not occurs when the Fermi-level of a poly-Si gate is higher than p+pinning position due to the energetics of interface reaction described by eq. (1) (Vo formation reaction is endothermic). Pre-existing Si oxide layers can act as O source when Fermi-level of a poly-Si gate is sufficiently high.

In other word, interface reaction accompanied with Io generation can be exothermic, although Vo formation is endothermic. As described in Fig.5, at p+pinning position energy gain (loss) of Vo annihilation reaction is zero. Vo annihilation reaction resembles Io generation reaction, since O transfer from poly-Si to high-k dielectrics occurs in both reactions. However, Io generation reaction needs additional energy compared to Vo annihilation reaction. Electron transfer from gate Fermi-level to HfO_2 valence band top occurs in Vo annihilation reaction as shown in Fig. 5. However, since Io level is located above HfO_2 valence band top, electron transfer from Fermi level to Io level occurs in Io formation reaction. As a result, Io formation reaction needs additional energy. This situation is schematically illustrated in Fig. 7.

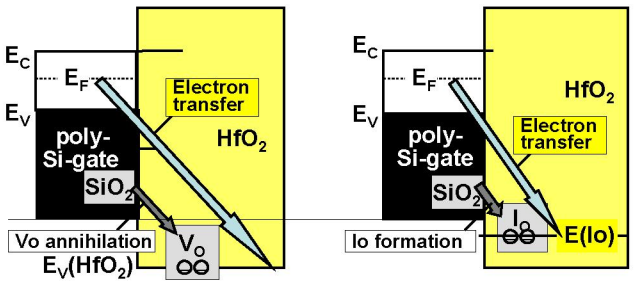

Fig.7: Schematic illustration of the difference in reaction energies between Vo annihilation and Io formation reactions. (a) Vo annihilation. (b) Io formation.

By taking into account the above energy difference originated from the higher energy level position of Io, we can estimate the n+pinning position. In the estimation, we assume that energy losses of O transfer from SiO_2 in poly-Si gates to HfO_2 in both reactions of Io formation and Vo annihilation are the same. In other words, we attribute additional energy in Io formation to the difference in energy gain due to electron transfer in our framework. Io formation reaction is governed by the following reaction equation.

$$\tfrac{1}{2}SiO_2 + (HfO_2) + 2e \rightarrow \tfrac{1}{2}Si + (HfO_2) + Io^{2-}. \quad (5)$$

Eq. (5) can be divided into two parts of O and electron transfers, as follows.

$$\tfrac{1}{2}SiO_2 + (HfO_2) \rightarrow \tfrac{1}{2}Si + (HfO_2) + Io - \Delta G_O, \quad (6)$$

$$(HfO_2) + Io + 2e \rightarrow (HfO_2) + Io^{2-} + \Delta G_e^I, \quad (7)$$

Further, Vo annihilation reaction can also divided into two parts of O and electron transfer as follows, considering the assumption that the energy loss for O transport in Vo annihilation is the same as that in Io formation ΔG_O as mentioned above.

$$\tfrac{1}{2}SiO_2 + (HfO_2) + Vo^{2+} \rightarrow \tfrac{1}{2}Si + (HfO_2)^{2+} - \Delta G_O, \quad (8)$$

$$\tfrac{1}{2}Si + (HfO_2)^{2+} + 2e \rightarrow \tfrac{1}{2}Si + (HfO_2) + \Delta G_e^V. \quad (9)$$

At p+pinning position, E(p+), $\Delta G_e^V - \Delta G_O = 0$ should be satisfied because the energy gain (loss) of Vo annihilation reaction becomes zero as previously described in Fig. 5. The energy gain of electron transfer in Vo annihilation reaction ΔG_e^V can be expressed as $2(E(p+) - E_v(HfO_2))$, E(p+) satisfies

$$2(E(p+) - E_v(HfO_2)) - \Delta G_O = 0, \quad (10)$$

where $E_v(HfO_2)$) is the valence band top of HfO_2.

When the original Fermi-level is sufficiently high, pinning position should be governed by the interface reaction including Io generation from pre-existing SiO_2 component in poly-Si. This pinning position E(n+) satisfies $\Delta G_e^I - \Delta G_O = 0$. Further, energy gain by electron transfer in Io formation reaction ΔG_e^I can be written as $2(E(n+) - E(Io))$, E(n+) satisfies

$$2(E(n+) - E(Io)) - \Delta G_O = 0, \quad (11)$$

By combining Eq. (10) and (11), we can obtain

$$E(n+) = E(p+) + (E(Io) - E_v(HfO_2)) \quad (12)$$

As shown in Eq. (12), n+pinning position E(n+) is located higher than p+pinning position E(p+), since E(Io) is located above $E_v(HfO_2)$. By choosing parameter E(Io) as

$$E(Io) = E_v(HfO_2) + 0.2\ eV, \quad (13)$$

we can obtain

$$E(n+) = E(p+) + 0.2\ eV, \quad (14)$$

reproducing experimental results illustrated in Fig.2.

As discussed above, we have elucidated that there are two mechanisms that govern Fermi-level pinning. When original Fermi-level is sufficiently high, O interstitial formation determines the pinning position E(n+). Whereas, when the original Fermi-level is sufficiently low, O vacancy formation determines the pinning position E(p+).

It should be noted that both Io formation and Vo formation are endothermic, in the energy region between E(p+) and E(n+). Thus, Fermi-level pinning does not occur in this energy region (Fig. 8). We call this region work-function pinning free region. Another noticeable fact is that characteristics of high-k dielectrics determine the pinning natures from our theory. In high-k dielectrics in which O vacancies are likely to be introduced, p+pinning is dominant. On the other hand, n+pinning is dominant in high-k dielectrics in which O interstitials tends to be generated. This tendency also reproduces experiments. In Io former such as Al_2O_3, n+pinning

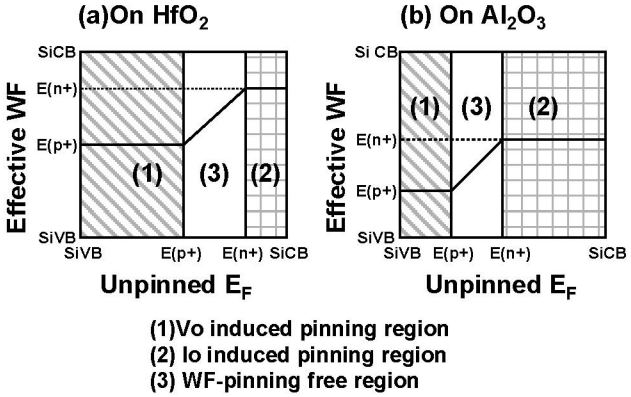

Fig. 8: Model for WF-pinning by oxygen transport mechanism. Dielectric dependence can be explained by difference in Io and Vo generation.

is really dominant, although p+pinning is dominant in HfO_2 which is a typical Vo former. This tendency is schematically illustrated in Fig. 8.

Above results also reproduce the recent experiments that Al incorporation into HfO_2 reduces the p+pinning region and symmetric Vth for nMOS and pMOS can be obtained [13], since Al incorporation induces Io generation due to the fact that Al_2O_3 is a typical Io former as mentioned before.

As discussed above, we can achieve the systematic understanding of Fermi-level pinning of n+ and p+ poly-Si gates by considering the Io and Vo formation by the interface reaction. At first glance, Io and Vo mechanisms are much different each other, However, we think that both mechanisms are essentially the same, since both mechanisms contain O and electron transfer across the interfaces in the important interface reaction.

Moreover, we can give a guideline for the fundamental relaxation of Fermi-level pinning. This is the widening of the pinning-free region. Very recently, metal/$HfLaO_x$ high-k gate stacks reveal pinning free natures [14]. At present, we suppose that La incorporation contributes to the widening of the pinning-free region. However, further detailed studies are necessary for clarifying the La incorporation effects.

III. Fermi-Level Pinning of Metal Silicide Gates

Fermi level pinning of metal silicide gates can also be explained by the similar framework to poly-Si gates. In case of metal silicide gates Io and Vo also play crucial roles in determining pinning positions of n-like and p-like metal silicde gates, respectively.

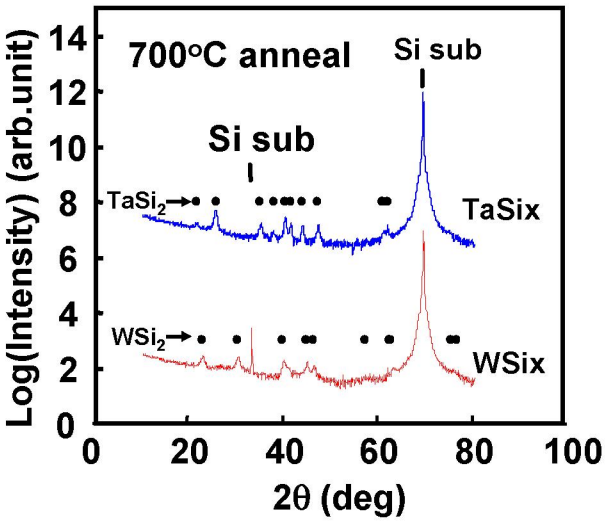

Fig.9 XRD spectra of WSix and TaSix

First, we show the pinning mechanism of n-like metal silicides. Fermi-level pinning occurs in a similar manner for n-like metal silicide gate material, if the excess O atoms also slightly oxidize Si within the metal silicides. We can test this theory on n-like tungsten silicide and tantalum silicide gate materials, by comparing with the experiments. From the X-ray diffraction (XRD) experiments, our considered WSi and TaSi mainly contain WSi_2 and $TaSi_2$ respectively as shown in Fig. 9.

Both WSi_2 and $TaSi_2$ films have metal-rich phases W_5Si_3 and Ta_5Si_3, respectively, which indicate that partial oxidation of Si has occurred within the metal silicides (MSi_2) as follows.

$$(5/14)MSi_2+½O_2 \rightarrow (1/14)M_5Si_3+½SiO_2 \qquad (15)$$

For the case of n-like MSi_2, Io generation in the gate dielectric occurs until the following reaction is balanced, *i.e.* when $E_F = E(nMSi)$:

$$(1/14)M_5Si_3+½SiO_2+HfO_2+2e \leftrightarrow (5/14)MSi_2+HfO_2+Io^{2-} \qquad (16)$$

The metal-rich M_5Si_3 phase is slightly more stable than the Si-rich MSi_2 phase as shown in Table I. Thus, Io formation in the Hf-based gate dielectric is expected to be a little easier for an n-like MSi gate than for n+ poly-Si gate as shown in Fig.

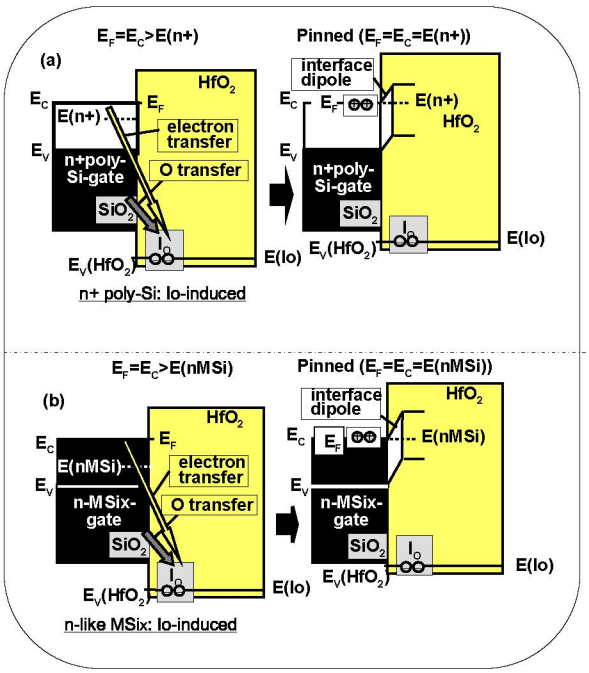

Fig. 10: Comparison between the Fermi level pinning of n+poly-Si gates and n-like metal silicides.

Table I:
Reported heat of formation of metal silicides.

MSi_X	Heat of Formation(eV)
WSi_2	0.96
$TaSi_2$	1.24
W_5Si_3	2.02
Ta_5Si_3	3.47

Table II:
Calculated and observed pinning position of n-like WSi_2 and $TaSi_2$ gates measured from E(n+).

MSi_X	E(nMSi)–E(n+) on HfSiON (eV)	
	Theory	Experiment
WSi_2	–0.10	–0.09
$TaSi_2$	–0.10	–0.10

10. Theoretical estimates of the Fermi-level pinning positions for typical n-like $TaSi_2$ and WSi_2 gate materials by combining Eqs. (5) and (16) give that pinning positions of n-like metal silicides are located ~0.1 eV lower than E(n+), in good agreement with experimental observations as described in Table II.

Similar discussions can be adopted for p-like metal silicides. Generally, heat of formation of metal silicides is considerably smaller than that of SiO_2 or HfO_2. Thus, pinning position is similarly lowered a little due to the fact that metal-rich metal silicides are a little more stable than the Si-rich metal silicides. As a result, each Fermi-level pinning position of n+, and p+poly-Si, n-like and p-like metal silicides are schematically described in Fig. 2.

IV. Approaches to Achieving Near-Band-Edge Φ_{MEFF} for n-like Gate

According to our model, removal of pre-existing SiO_2 originated from excess O atoms in poly-Si will be effective to relax n+pinning. One possible way is incorporation of Ge in n+poly-Si gates [15,16] . Due to the low reactivity of Ge with O, SiO_2 formation by excess O atoms in poly-Si will be suppressed. In Fig. 11, cross-sectional transmission electron microscopy images of n+ poly-Si and n+ poly-SiGe gate electrodes on HfO_2 gate dielectrics are shown. A rough interface structure is observed for the n+ poly-Si gate, but not for the n+ poly-SiGe gate. The presence of Ge prevents partial oxidation by the excess O atoms because of the low reactivity of Ge with O. The experimentally measured Φ_{Meff} for the n+ poly-SiGe gate is ~0.1 eV lower than that for the n+ poly Si gate (Fig. 12), although the vacuum work functions of n+ poly-Si and n+ poly-SiGe are nearly identical. These results indicate that n+ poly-SiGe is a promising near-conduction-band-edge Φ_{Meff} gate material for Hf-based dielectrics.

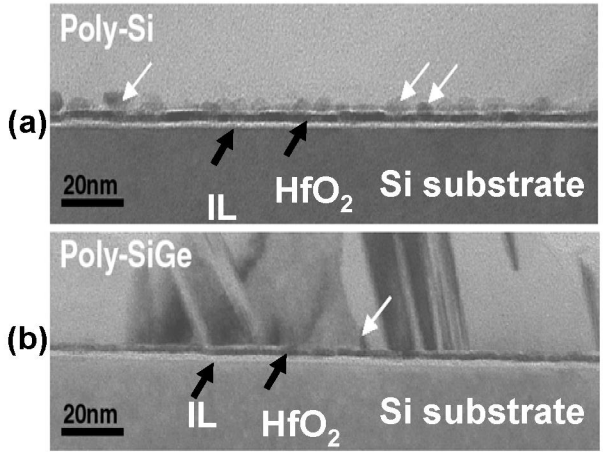

Fig. 11 Cross-sectional TEMs for HfO_2 gate stacks annealed at 950°C with either (a) poly-Si or (b) poly-$Si_{0.75}Ge_{0.25}$ gate material.

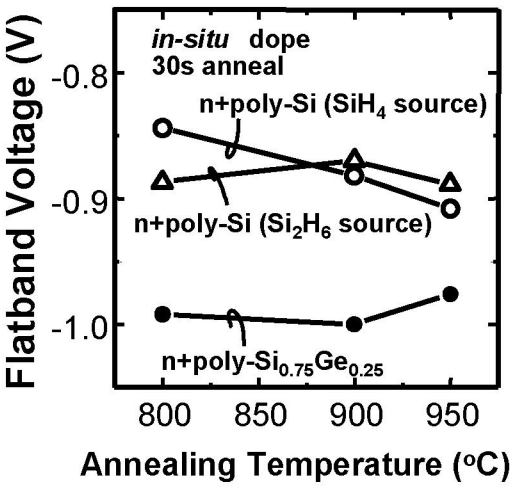

Fig.12 Anneal temperature dependent flat band voltage of HfO_2 gate stacks with n+ poly-Si and poly-$Si_{0.75}Ge_{0.25}$ gates.

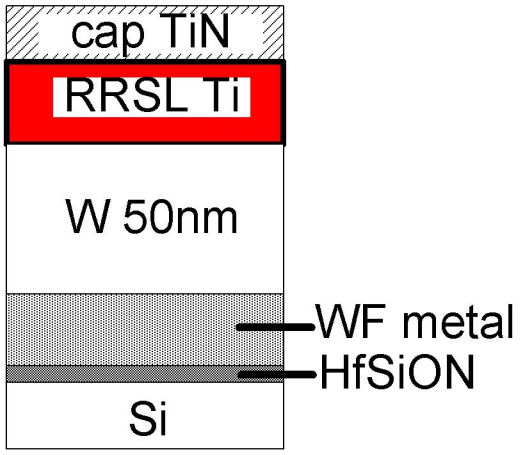

Fig. 13: Schematic cross-section of gate stack with a reactive Ti capping layer. Ti layer is inserted between cap TiN and W.

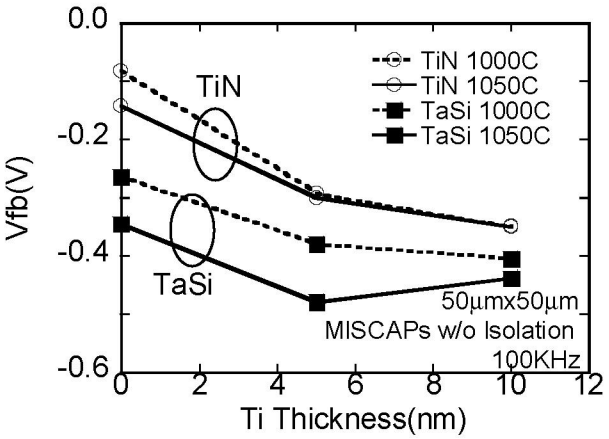

Fig. 14 Ti thickness dependence on Vfb.

Other approaches to minimize O transport into the gate dielectric include minimizing the process thermal budget, and gettering O away from the gate dielectric interface. Recently, it was reported that Hf-silicide gate electrodes formed by a low-temperature process exhibit near-band-edge Φ_{Meff} [17]. A possible explanation is that the Hf atoms in the gate act as sinks for excess O atoms. Further, we have confirmed experimentally that a reactive Ti metal capping layer (remote reactive sink layer (RRSL)) over the MSi gate improves pinning of n-like material (TaSi) [18] (Fig. 13, 14). This result can naturally be explained by considering that a Ti capping layer effectively getters O.

V. SUMMARY

Fermi-level pinning of poly-Si and metal-silicide gate materials on Hf-based gate dielectrics has been systematically studied theoretically. Fermi-level pinning in high-work-function materials is governed by the O vacancy generation and subsequent formation of interface dipoles near gate electrodes due to the electron transfer. On the other hand, O interstitial formation plays a crucial role for Fermi-level pinning of low-work-function materials.

Fermi-level pinning of high-work-function and low-work-function materials can be systematically understood by considering the O and electron transfer across the interfaces in the Io and Vo formation reactions near the interface. Further, we propose some recipes in order to obtain near-band-edge work-functions for n-like gates.

Moreover, we have found that the work-function pinning-free-region generally appears due the difference in the mechanism of Fermi-level pinning of high- and low-work-function materials from our theoretical considerations. The widening of this work-function pinning-free-region is the key issue for the fundamental relaxation of Fermi-level pinning in high-k gate dielectrics.

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REFERENCES

[1] G. D. Wilk and R. M. Wallace, "Electrical properties of hafnium silicate gate dielectrics deposited directly on silicon", Appl. Phys. Lett, vol. 74, pp.2854-2856, May 1999.

[2] G. D. Wilk, R. M. Wallace, J. M. Anthony, "Stability and band offsets of nitrogenated high-dielectric-constant gate oxides", J. Appl. Phys., vol. 89, pp.5243-5275, May 2001.

[3] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, P. Tobin, "Fermi Level Pinning at the PolySi/Metal Oxide Interface", Technical Digest of 2003 Symposium on VLSI Technology, Kyoto, Japan, pp.9-10, June 2003.

[4] E. Cartier, V. Narayanan, E. P. Gusev, P. Jamison, B. Linder, M. Steen, K. K. Chan, M. Frank, N. Bojarczuk, M. Copel, S. A. Cohen, A. Callegari, S. Zafar, M. Gribelyuk, M. Chudzik, C. Cabral Jr., R. A. Carruthers, C. D'Emic, J. Newbury, D. Lacey, S. Guha, R. Jammy, "Systematic Study of pFET Vt with Hf-Based Gate Stacks with Poly-Si and FUSI Gates", Technical Digest of 2004 Symposium on VLSI Technology, Honolulu, USA, pp.44-45, June 2004.

[5] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi, A. Nishiyama, "Effect of Nitrogen in HfSiON Gate Dielectrics on the Electrical and Thermal Characteristics", Technical Digest of 2002 IEEE International Electron Devices Meeting, San Francisco, USA, pp.849-852, December 2002.

[6] M. Takayanagi, T. Watanabe, R. Iijima, A. Kaneko, S. Inumiya, I. Hirano, K. Sekine, A. Nishiyama, K. Eguchi, Y. Tsunashima, "HfSiON Gate Dielectric for CMOS Application", Extended Abstracts of International Workshop on Gate Insulator, Tokyo, Japan, pp.174-175, November 2003.

[7] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Konno, T. Chikyo, H. Kitajima, T. Arikado, "Physics in Fermi Level Pinning at the PolySi/Hf-based High-k Oxide Interface", Technical Digest of 2004 Symposium on VLSI Technology, Honolulu, USA, pp.108-109, June 2004.

[8] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Konno, T. Chikyo, H. Kitajima, and T. Arikado, "Oxygen Vacancy Induced Substantial Threshold Voltage Shifts in the Hf-based High-k MISFET with p+poly-Si Gates -A Theoretical Approach", Jpn. J. Appl. Phys. Part 2, vol. 43, pp.L1413-L1415, November 2004.

[9] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Konno, T. Chikyow, H. Kitajima, T. Arikado, and Y. Nara: "Oxygen-vacancy-induced threshold voltage shifts in Hf-related high-k gate stacks", Thin Solid Films, vol. 508, 305-310, June 2005.

[10] K. Shiraishi, H. Takeuchi, Y. Akasaka, H. Watanabe, N. Umezawa, T. Chikyow, Y. Nara, T.-J. King Liu, and K. Yamada, "Mechanism of Fermi-Level Pinning for n-like Metal Silicides on Hf-based Gate Dielectrics", Proc. IEEE 2006 Si Nanoelectronics Workshop, Honolulu, USA, pp.115-116, June 2006.

[11] H. Takeuchi, D. Ha and T-J King, "Observation of bulk HfO_2 defects by spectroscopic ellipsometry", J. Vac. Sco. Tech. A, vol. 22, pp.1337-1341, July-August 2004.

[12] R. J. Stroh, F. Plais, T. Kretz, P. Legagneux, 0. Huet, M. Magis, D. Pribat, N. Jiang, M.C. Hugon, B. Agius, "Low-temperature (*< 600°C)* polysilicon thin-film transistors", IEE Proc. Circuits, Devices, Syst., vol .141, pp. 9-13, February 1994.

[13] M. Kadoshima, A. Ogawa, H. Ota, K. Iwamoto, M. Takahashi, N. Mise, S. Migita, M. Ikeda, H. Satake, T. Nabatame, and A. Toriumi, "Symmetrical threshold voltage in complementary metal-oxide-semiconductor field-effect transistors with $HfAlO_x(N)$ achieved by adjusting Hf/Al compositional ratio", J. Appl. Phys. vol. 99, Art. No. 054506, March 2006.

[14] H.R. Alshareef, H.C. Harris, C.S. Wen, C.S. Park, C. Huffman, K. Choi, H.F. Luan, P. Majhi, B.H. Lee, R. Jammy, D.J. Lichtenwalner, J. S. Jur, and A.I. Kingon, "Thermally Stabel N-Metal Gate MOSFETs Using La-Incorporated HfSiO Dieletric", Technical Digest of 2006 Symp. on VLSI Tech. Honolulu, USA, pp.10-11, June 2006.

[15] Q. Lu, H. Takeuchi, X. Meng, T-J. King, C. Hu, K. Onishi, H-J. Cho and J. Lee, "Improved Performance of Ultra-Thin HfO_2 CMOSFETs Using Poly-SiGe Gate", Techincal Digest of 2002 Symp. on VLSI Tech. Honolulu, HI, USA, pp.86-87, June 2002.

[16] D. Ha, Q. Lu, H. Takeuchi, T-J. King, K. Onishi, Y-H. Kim, and J. C. Lee, "Impact of Gate Process Technology on EOT of HfO_2 Gate Dielectric", Mat. Res. Soc. Proc. vol. 765, paper D2.2.1, April 2003.

[17] T. Hirano, T. Ando, K. Tai, S. Yamaguchi, T. Kato, S. Hiyama, Y. Hagimoto, S. Takesako, N. Yamagichi, K. Watanabe, R. Yamamoto, S. Kanda, S. Terauchi, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, S.

Kadomura, and N. Nagamune, "High Performance nMOSFET with HfSix/HfO_2 Gate Stack by Low Temperature Process", Technical Digest of 2005 IEEE International Electron Devices Meeting, Washington D.C., USA, pp.911-914, December 2005.

[18] Y. Akasaka, K. Shiraishi, N. Umezawa, O. Ogawa, T. Kasuya, T. Chikyow, F. Ootsuka, Y. Nara and K. Nakamura, "A Novel Remote Reactive Sink Layer Technique for the of N and O concentration in Metal/High-k Gate Stacks", Technical Digest of Symp. on VLSI Tech., Honolulu, USA, pp.206-207, June 2006.

