Effect of Body Doping on the Scaling of Ultrathin SOI MOSFETs

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***Abstract*—This paper presents a detailed simulation study on the body doping effect on scaling of ultrathin silicon-on-insulator (SOI) MOSFETs with standard thick buried oxide (BOX). By employing high-κ dielectrics, it is demonstrated that the minimum scalable channel length L_{min} for fully-depleted (FD) SOI MOSFETs can be significantly improved from L_{min} ~$5t_{Si}$ for undoped case [1] to L_{min} ~$2t_{Si}$ with doping. By scaling the gate insulator thickness toward its tunneling limit, it is possible to scale doped body FDSOI to ITRS 45nm technology node (TN). Quantum mechanical and threshold considerations will ultimately limit how high a body doping can be used.**

Keywords-Buried oxide (BOX) thickness; body doping; short-channel effect; silicon-on-insulator (SOI) MOSFET.

I. INTRODUCTION

Since bulk CMOS technology is approaching its scaling limit, fully-depleted (FD) silicon-on-insulator (SOI) MOSFET has been recognized as the potential candidate for developing high performance consumer electronics. The ultrathin silicon body of a SOI MOSFET is electrically isolated from underlying substrate by a thick buried oxide (BOX). The source/drain junction surface is reduced and hence less junction capacitance can be observed. The short-channel effect can be well suppressed by directly thinning down the silicon film and BOX thickness. Whereas scaling down BOX thickness below 5nm of a FDSOI MOSFET leads to a double-gate-like device, the process technology is still complex and immature. In contrast to BOX thickness scaling, the channel thickness scaling is more technically achievable [2] and, therefore, interest in ultrathin body FDSOI MOSFETs is growing. Previous published experimental studies [3] already show the viability of nanoscale ultrathin body, undoped FDSOI MOSFETs with thick BOX.

According to the design study for ultrathin body, undoped FDSOI MOSFETs in [1], sub-20nm FDSOI device requires silicon film thickness below ~2nm with gate oxide. The minimum scalable channel length is limited by ~$5t_{Si}$ even with high-κ gate dielectrics. To further understand the possibility to relax the design space of silicon film thickness, the effect of body doping on electrostatic integrity is investigated in this paper. To successfully assess the threshold rolloff and minimum scalable channel length in short channel doped FDSOI MOSFETs, an extensive 2-D numerical simulation-based design study is carried out by state-of-the-art device simulator DESSIS. 1-D Schrödinger solver and drift-diffusion model are both activated to gain a clear picture of threshold limitation imposed by quantum mechanical effect. The feasibility of doped FDSOI design for 45nm TN is evaluated with scaling high-κ gate dielectrics down to its tunneling limit.

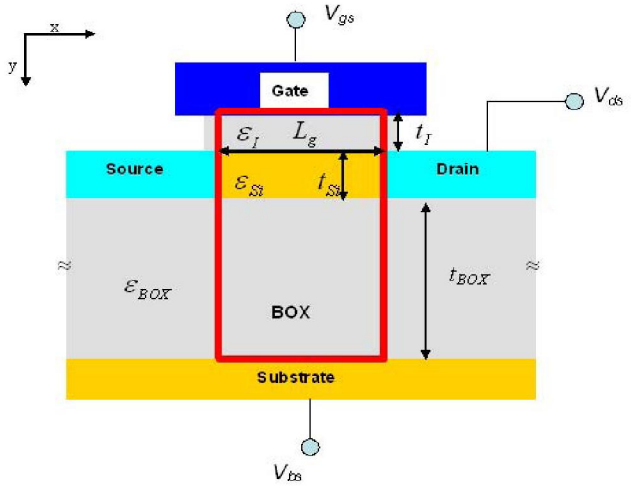


Fig. 1. Schematic of ultrathin SOI MOSFET. The source/drain junction is abrupt and L_g is the metallurgical channel length.

II. GENERAL SCALING IN DOPED FDSOI MOSFETS

The schematic device cross section used in our simulation study is shown in Fig. 1. Source, drain, substrate, and body regions are doped uniformly. DIBL and low-drain threshold rolloff are defined with V_{ds}=1V and 50mV, separately. The maximum allowable threshold rolloff is set to be 100mV. The substrate bias is fixed at 0V to avoid its effect on threshold rolloff. Fig. 2 [1] shows that light channel doping in SOI only causes threshold voltage shift without any short-channel effect (SCE) improvement [4]. SCE can be mitigated with high doping in thin silicon films (t_{Si} ≈4 -10nm), but the tradeoffs are higher threshold voltage and lower carrier mobility due to impurity scattering. Fig. 2 indicates that L_{min} is 25% improved with the channel doping concentration raised

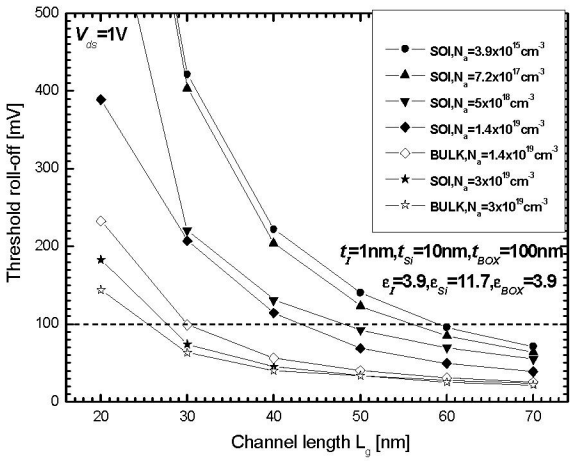


Fig. 2. High drain threshold voltage rolloffs for SOI with varying channel doping concentration. [1]

to N_a=1.4x10^{19}cm^{-3}. For N_a>3x10^{19}cm^{-3}, the SOI device exhibits a short-channel behavior similar to that of a bulk MOSFET because the body becomes partially depleted.

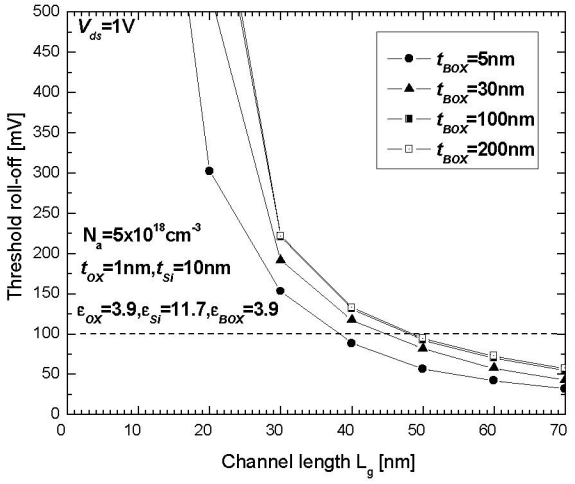
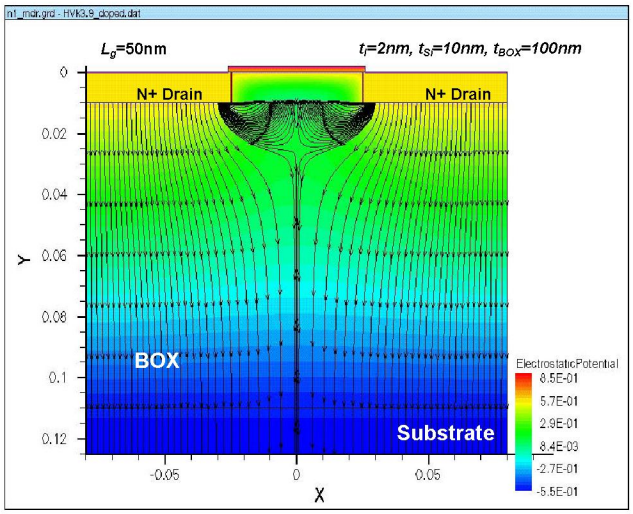


Fig. 3. High drain threshold voltage rolloffs for doped FDSOI with different BOX thicknesses.

The scaling limit of bulk and DG MOSFETs are governed by the scale-length model and the minimum scalable channel length is limited to 1.5~2 λ, where λ is the scale length determined by the eigenvalue equation derived from boundary conditions [5], [6]. In contrast to bulk and DG MOSFETs, there is no clear guideline for short-channel scaling in doped FDSOI MOSFETs. The BOX is too thick to define an enclosed region with well-defined conditions in solving the 2-D boundary value problem for Poisson's equation. Fig. 3 shows the simulated high-drain threshold voltage rolloffs in sub-0.15um doped FDSOI MOSFETs for various BOX



V_{gs}=0.6V, V_{ds}=V_{bs}=0V, N_a=8.8x10^{18}cm^{-3}

Fig. 4. Field pattern inside BOX of the short channel doped FDSOI device with ε_I=35.1

thicknesses by using drift-diffusion model in DESSIS. In order not to have a high-threshold SOI device, a metal gate with work function between mid-gap and N+ poly gate work function is assumed to be technically available so that the long channel SOI threshold voltage is ~0.4V. For t_{BOX}=5nm, the L_{min}≈38nm and increases with a thicker buried oxide layer. However, for t_{BOX}=100nm and 200nm, the L_{min} is 48nm for both cases. The simulation result shown in Fig. 3 implies that the depth of source/drain lateral field coupling in the BOX does not increase with BOX thickness after t_{BOX} is two times larger than the channel length of the device with 100-mV threshold rolloff. The field pattern in the BOX indicated in Fig. 4 shows that the depth of lateral field coupling depends on the source/drain spacing. The effective BOX thickness is not equal to the physical BOX thickness and, therefore, scaling in short channel doped SOI device is independent of BOX thickness.

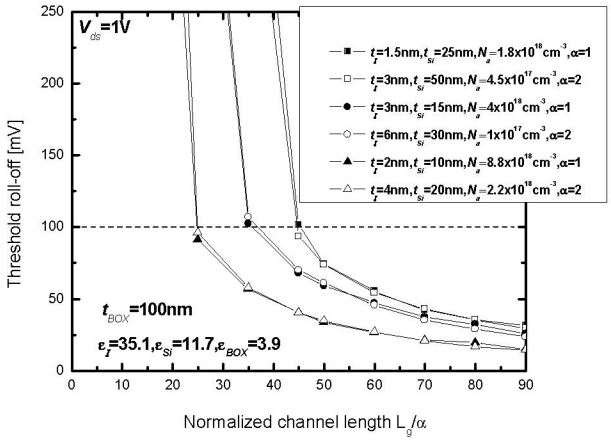


Fig. 5. General scaling in doped FDSOI MOSFETs.

In the generalized scaling rule of bulk MOSFETs, both the gate dielectric thickness and the gate-controlled depletion width in silicon must be reduced in proportional to channel length. To determine the scaling rules of doped SOI MOSFETs, extensive 2-D numeric simulations are carried out by drift-diffusion model in DESSIS. The short-channel scaling of doped SOI devices depends only on the silicon-film thickness, gate dielectric thickness, the corresponding permittivities, and body doping concentration, as shown in Fig. 5. For given channel doping N_a, dielectrics ε_I and ε_{Si}, the L_{min} is scaled down by a factor of α if both t_I and t_{Si} are scaled down by the same factor α but N_a is scaled up by a factor of α^2.

III. Realxed t_{Si} Design Space in Doped FDSOI

Since the scaling principles of doped FDSOI are governed by the body doping, silicon film and gate dielectric thickness, constant L_{min}=45nm contours are plotted in a N_a-t_{Si} plane for ε_I =3.9, 11.7, and 35.1 in Fig. 6. The partially-/fully-depleted SOI boundary is obtained by the depletion width equation for bulk MOSFETs in [7] and is valid for long channel SOI MOSFET. For short channel SOI MOSFET, however, the silicon film thickness can be further relaxed with a given off current level and the body is still fully-depleted because the charge sharing occurs in source/drain region. In Fig. 6, each L_{min} contour is composed of different combinations of N_a, t_I, and t_{Si} that yield a 100mV high-drain threshold rolloff at a given channel length of 45nm. The simulation results in Fig. 6 can be generalized to other values of L_{min} by scaling all t_I, t_{Si}, and L_{min} by a common factor of α but α^2 for N_a, as demonstrated in Fig. 5. High-κ insulators allow thicker t_I for given N_a, t_{Si}, and L_{min}. For extremely thin high-κ gate dielectrics, the design space of silicon film thickness can be relaxed most by doping body toward partially-/fully-depleted SOI boundary. For EOT=0.5nm, the short-channel effect of ε_I =35.1 case is worsened by the 2-D effect in thick gate dielectric and has narrower t_{Si} design space than ε_I =3.9. With high-κ dielectrics, the L_{min} of undoped FDSOI is limited to ~5t_{Si} [1]. The L_{min} limitation can be further improved to ~2t_{Si} with body doping and is same as the~2W_{dm} limitation in bulk MOSFETs [7].

Body doping also improves subthreshold slope in FDSOI MOSFETs. It is indicated in Fig. 7 that the subthreshold slope of doped FDSOI devices is inverse proportional to body doping concentration and silicon film thickness. When the silicon body of a SOI device remains fully-depleted, the corresponding subthreshold slope decreases with higher doping and thicker t_{Si}. Considering any L_{min} contour in Fig. 6, the best subthreshold slope solution of FDSOI MOSFETs occurs when the silicon body is doped nearly partially-depleted. Furthermore, doping helps to reduce the threshold variation when the silicon film thickness is scaled down to 5nm and below. For undoped ultrathin SOI MOSFETs, threshold voltage increases with decreasing silicon film thickness due to quantum confinement of carriers and varies dramatically after t_{Si} < 5nm. For doped body SOI MOSFETs design, however, threshold voltage depends on both body doping level and silicon film thickness. One can design doped SOI with an acceptable *SCE* by a moderately doped thin silicon body or a highly doped thick silicon body without large threshold voltage variation. Whereas body doping can mitigate 2-D effect, it has deleterious effect on carrier mobility due to impurity scattering. The mobility degradation needs to be taken into consideration as the trade-off.

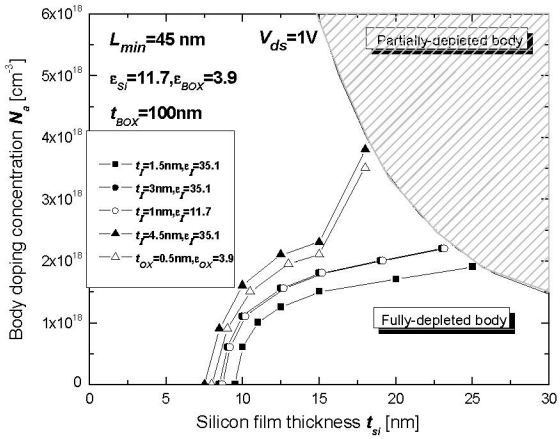


Fig. 6. Constant minimum channel length (L_{min}=45nm) contours for doped FDSOI with three different gate dielectrics.

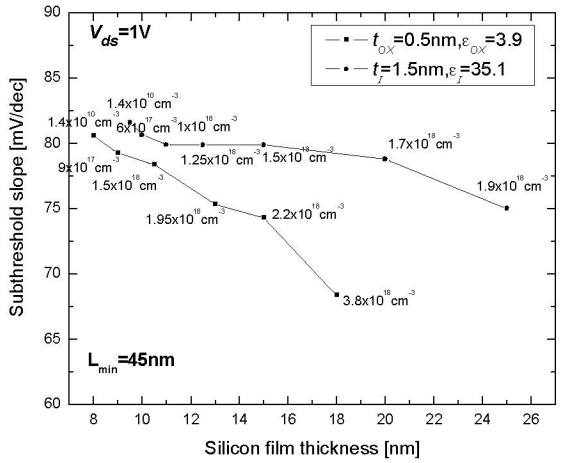


Fig. 7. Subthreshold slopes for L_{min} contours with t_{ox}=0.5nm and t_I=1.5nm in Fig. 6.

IV. FDSOI Design for 45nm TN

The possibility of doped FDSOI MOSFET design for 45nm technology node is also investigated in this paper. Fig. 8 shows the t_{Si} design space with different gate dielectrics in

doped FDSOI with N+ poly gate. Each data point is obtained by solving Poisson equation and 1-D Schrödinger equation in DESSIS to ensure that the threshold voltage of corresponding device is ~ 0.3V. According to the ITRS gate dielectric thickness requirement [8], the effective oxide thickness of high-κ dielectric is 0.7nm and a physically thick gate dielectric design is needed. However, 2-D effect emerges in thick gate dielectrics, worsens short-channel effect and leads to a narrower t_{Si} design space. It is indicated in Fig. 8 that with gate insulator thickness scaled down to its tunneling limit, the *silicon film thickness* can be relaxed further even with increasing dielectric constant. According to the solution of Schrödinger equation, the tunneling distance is inverse proportional to square root of barrier height of the gate material. Therefore, the tunneling limit thickness is simply assessed by the following equation:

$$\alpha_{high-k} \approx \sqrt{\phi_{B,oxide} / \phi_{B,high-k}} \qquad (1)$$

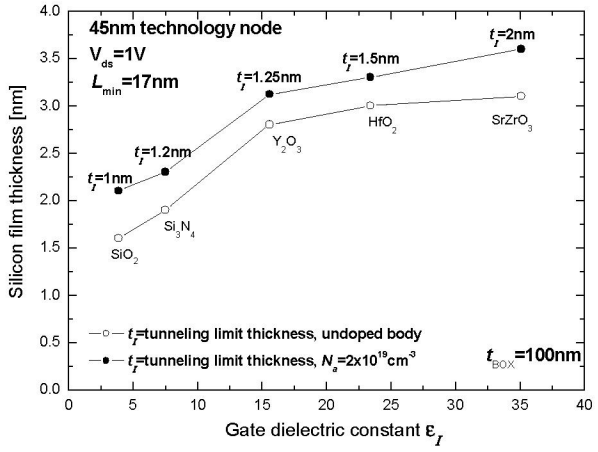


Fig. 8. Design space of doped FDSOI MOSFETs with gate oxide and high-κ gate insulators for 45nm technology node.

Since the minimum gate oxide thickness for high performance operation is ~1nm, the tunneling limit of high-κ gate dielectrics can be simply assessed by (1) with α_{oxide}=1nm, e.g., α_{HfO2}≈1.5nm. Body doping in ultrathin silicon film shows limited improvement due to quantum effect, and threshold voltage considerations [1]. It also has the trade-off for lower carrier mobility caused by impurity scattering [9], [10]. Scaling down high-κ gate dielectrics to their tunneling limits [11] will allow thicker t_{Si} in FDSOI design for 45nm technology node.

V. Conclusion

Through extensive numerical simulations, we demonstrated that the scaling principle of doped FDSOI MOSFETs is independent of buried oxide thickness and similar to bulk MOSFETs scaling. The design space of silicon film thickness requirement can be relaxed most when the doped body is nearly partially-depleted. With high-κ dielectrics, the L_{min} is limited by ~$2t_{Si}$, which is same as the L_{min} limitation in bulk MOSFETs. However, quantum effect and threshold considerations impose a limit on body doping in sub-20nm FDSOI MOSFETs.

Acknowledgment

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