3-Dimensional Analysis on the GIDL Current of Body-tied Triple Gate FinFET

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Abstract *–Triple gate FinFET is emerging as a promising candidate for the future CMOS device structures because of its immunity to short-channel effect. However, the suppression of GIDL is a significant challenge for its application.*

In this paper, we discuss the characteristics of GIDL on FinFET and extensively analyze the influence of the device technology on GIDL. The analysis is expected to give guidelines to the future development of triple gate FinFET.

1. INTRODUCTION

As the channel length of the CMOS is scaling down towards 10nm, the suppression of short channel effect has become more important. In this respect, FinFET becomes the most attractive device structure due to its superior channel controllability and high performance characteristics over the conventional transistor [1]. Especially, body-tied triple gate FinFET has advantages in heat dissipation, wafer cost, and defect density compared to SOI FinFET [2]. However, it is considered that GIDL is deteriorated in a FinFET structure [3]. In particular, the leakage current has a prominent impact on memory cell application where FinFET is considered as the most suitable device structure.

In this work, the characteristics of GIDL on body-tied triple-gate FinFET have been investigated and the conditions to minimize GIDL are proposed using 3D device simulation.

2. Leakage Characteristics of FinFET

As the device scales, the level of channel doping has been increased to reduce the short channel effects. Therefore, the electric field of the junction has been considerably increased; thus, junction leakage is a major component of off-state leakage current.

In contrast, FinFET shows GIDL-dominant characteristics in several respects. Firstly, a thin body device such as FinFET shows very low threshold voltage(~0V) with n-type gate (Fig. 1). Thus the application of p-type gate is necessary in order to increase the threshold voltage. This results in enhanced BTBT as shown in Fig 2. Secondly, there is field crowing effect induced by triple gate around the fin. In addition, the junction leakage is reduced by the application of low body doping which makes the GIDL a major leakage mechanism in FinFET. Our preliminary simulation, reflecting the scaling trend, reveals that GIDL would be more severe with the further scaling (Fig 3). Consequently, the biggest obstacle in the FinFET application and future scaling is the impact of GIDL, which should be kept low with the advanced structures and process optimization.

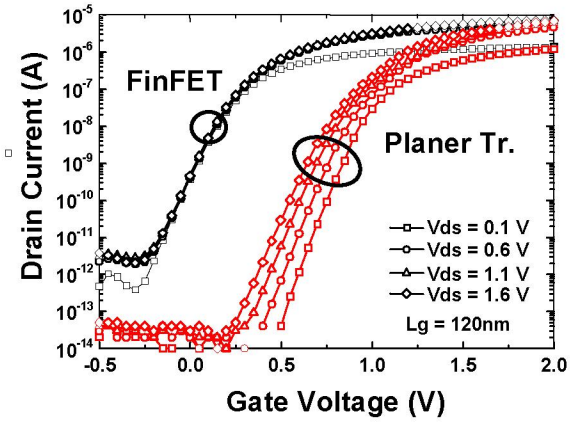


Fig. 1. Comparison of measured Id-Vg characteristics between triple gate FinFET and planaer transistor. SCE is improved with FinFET, however, threshold voltage drop is severe with the same n-type gate.

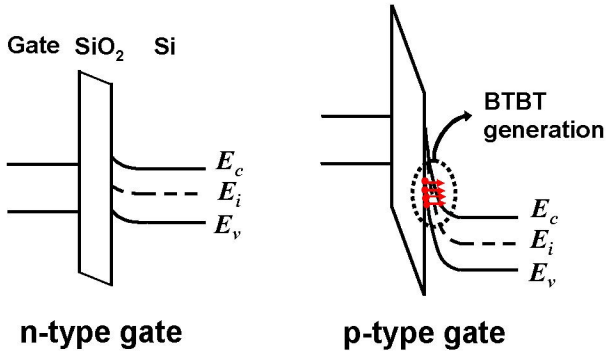
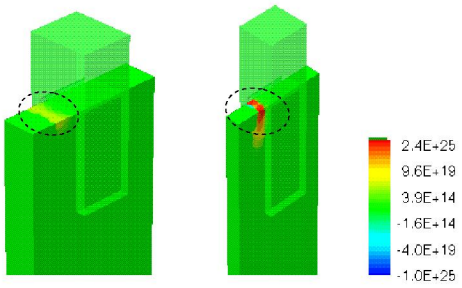


Fig. 2. Energy band diagrams for n-type and p-type gate applications. BTBT is enhanced with the p-type gate at the same negative gate bias due to the built-in potential difference.



3. Comparison of measured Id-Vg characteristics between triple gate FinFET and planaer transistor. SCE is improved with FinFET, however, threshold voltage drop is severe with the same n-type gate.

3. Device Simulation for GIDL Estimation

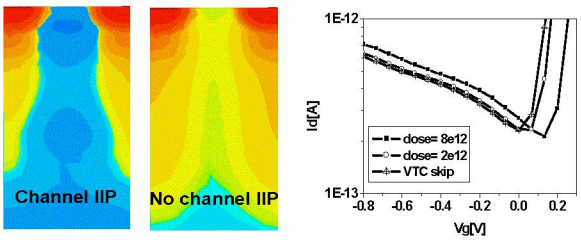
To evaluate the GIDL, we used HySyPros [4] for the process simulation and DESSIS [5] for the device simulation of 3D FinFET. Trap-assisted tunneling / band-to-band tunneling model are applied for the GIDL analysis.

In this study, channel implantation(IIP), source/drain IIP, doping level of the source/drain contact, fin thickness, gate length / spacer and SEG(Selective Epitaxal Growth) are investigated to analyze the influence on GIDL.

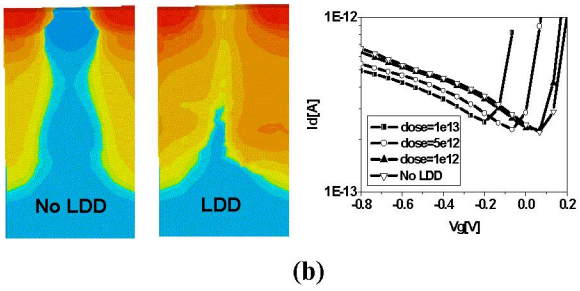
4. IMPACT ON GIDL IMPROVEMENT

A. Implantation Engineering

Fig. 4 shows the doping concentration and GIDL current according to the channel IIP and source/drain IIP. The GIDL current can be reduced to some degree by decreasing junction electric field with low channel doping and application of source/drain IIP. However, as shown in Fig. 4, the omission of channel IIP and irrelevant source/drain IIP can increase the short-channel effect(SCE) such as threshold voltage drop and DIBL. Therefore, the doping level should be selected carefully using device simulation regarding the channel and source/drain IIP. Fig. 5 shows the BTBT profile in terms of source/drain contact concentration. The characteristics of GIDL and SCE have been improved at the same time as gate/drain overlap region decreases by lightly doped source/drain contact. Therefore, the doping concentration of contact should be minimized if it does not degrade the performance severely.



(a)



(b)

Fig. 4. The reduction of channel IIP and application of source/drain IIP is effective for the GIDL reduction. However, SCE can be enhanced by these implantation engineering. (a) Doping profile and GIDL current as a function of channel IIP. (b) Doping profile and GIDL current as a function of source/drain IIP.

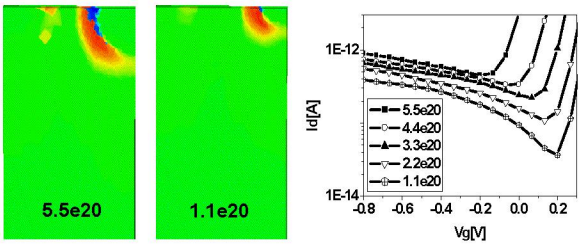
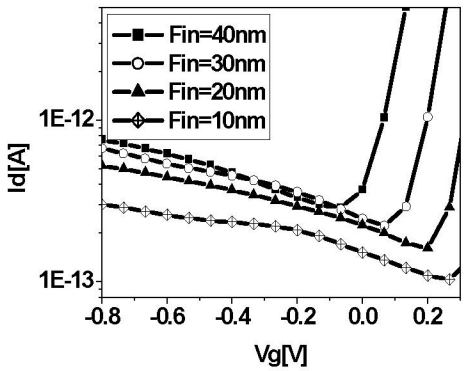


Fig. 5. The reduction of source/drain contact concentration can suppress GIDL and SCE at the same time. Appropriate trade-off between performance and GIDL is important for the selection of the doping level.

B. Structure Engineering

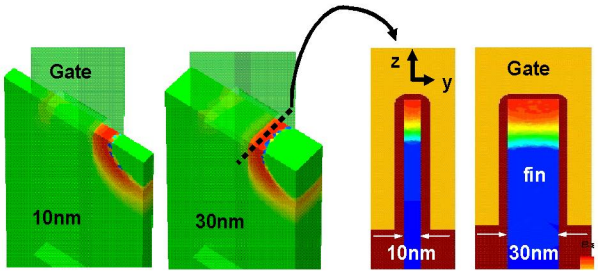
Fig.6 shows that GIDL is decreasing with the thinner fin thickness. Earlier 2D simulation on a double gate transistor reports that GIDL decreases in the thinner fin thickness due to the reduction of transverse electric field [6]. In our 3D simulation of triple gate FinFET also reveals that transverse electric field(y-axis) can be decreased. However, electric fields of other directions, which also contribute to GIDL, are not decreased. Fig. 6(c) shows that BTBT is generated at the center of fin as well as the surface. This indicates that the reduction of GIDL in the thinner fin is attributed to the reduction of GIDL generation region.



(a)

Fin thickness	10nm	20nm	30nm
y E-field [V/cm]	2.99e5	5.48e5	5.63e5
Total E-field [V/cm]	2.13e6	2.07e6	1.94e6

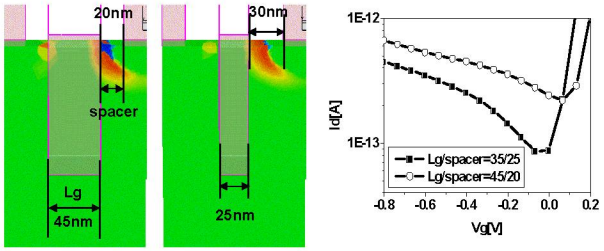
(b)



(c)

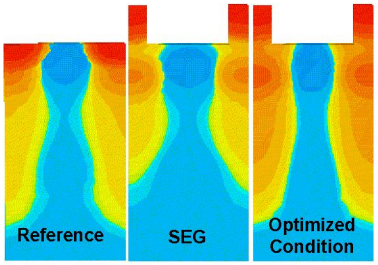
Fig. 6. (a) GIDL decreases as the fin thickness reduces. (b) Transverse electric field(y-axis) has been decreased, but, the other electric fields does not decrease in thinner fin. (c) GIDL is decreased as the BTBT generation region reduces.

In Fig. 7 the spacer thickness is increased and gate length is decreased to ensure the contact open size. The result shows that GIDL can be improved when the gate length decreases and the spacer thickness increases. This is owing to the reduction of overlap region between gate and drain. To maximize the reduction of the overlap region, we applied the SEG as source and drain contacts. The generation region of the BTBT moves to drain size and GIDL is reduced by more than 1 order. In this study, the application of SEG is the most effective way to suppress GIDL. However, the degradation of performance need to be improved. (Fig. 8)

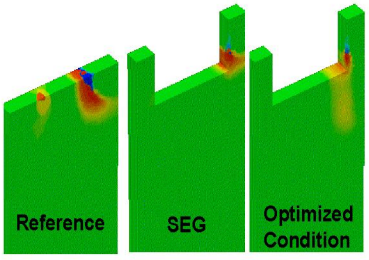


(a) (b)

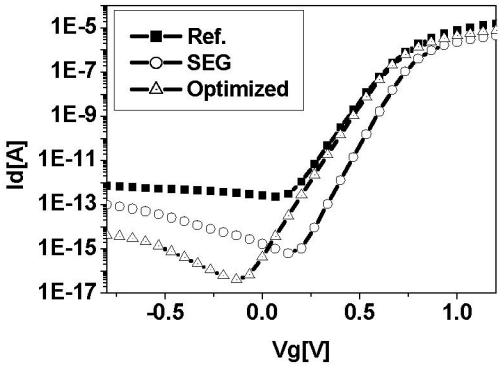
Fig. 7. Decreased gate length and increased spacer thickness can decrease the overlap region between gate and drain. Therefore, electric field and GIDL generation region can be reduced. (a) shows BTBT generation rate and (b) shows Id-Vg characteristics.



(a)



(b)



(c)

Fig. 8. Implementation of SEG process and IIP optimization can reduce GIDL by more than 3 orders. (a) doping profile, (b) BTBT generation rate, and (c) Id-Vg characteristics.

Table. 1. Comparison of electrical characteristics.

Item	Vth @Id1e-08	Ion	DIBL	SW	GIDL @Vg-0.4
No_SEG	0.529	3.0e-05	99	80	9.1e-13
SEG	0.654	8.86e-06	21	72	3.49e-14
Optimized Condition	**0.545**	**1.51e-05**	**74**	**82**	**7.87e-16**

5. OPTIMIZATION OF PROCESS AND STRUCTURE

On the basis of earlier analysis of process and structure dependency on GIDL, we have optimized the triple gate FinFET technology. Effective factors such as SEG,

increase of spacer thickness, lightly doped contact, and source/drain IIP are applied. With the application of source/drain IIP, the lateral electric field is reduced and the performance deterioration caused by the SEG is restored to some degree (Fig. 8). As shown in table1, GIDL is reduced more than 3 orders, which falls in the range of practical application. In the process of optimization, several factors such as the threshold voltage, on-current, off-state leakage should be considered at the same time. By virtue of 3D device simulation, we can find the optimal process and structure conditions which can be utilized to the application of triple gate FinFET.

6. CONCLUSIONS

The characteristics of GIDL on body-tied triple gate FinFET have been investigated using 3D device simulation. In order to suppress GIDL, lightly doped source/drain contact, reduced fin thickness, increased spacer thickness, and SEG process are preferable. Particularly, when effective conditions are optimized with the SEG process, the GIDL can be improved by more than 3 orders, which make it possible to apply the FinFET in low-power and memory cell application.

7. REFERENCES

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