Simulation of Multiple Gate FinFET Device Gate Capacitance and Performance with Gate Length and Pitch Scaling

Hui Zhao[1], Naveen Agrawal[1], Ramos Javier[2], Subhash C. Rustagi[3], M. Jurczak[2], Yee-Chia Yeo[1], Ganesh S. Samudra[1],
[1] Silicon Nano Device Laboratory (SNDL), ECE Department, National University of Singapore, Singapore. Email: eleshanr@nus.edu.sg
[2] IMEC, Kapeldreef75, Heverlee, Belgium
[3] Institute of Microelectronics, Singapore Science Park II, 2 Science Park Road, Singapore

***Abstract*— In this work, we simulate silicon-on-insulator (SOI) multiple gate FinFET (MuGFET) with the design targeting for the ITRS 2004 specifications for NMOSFET. A detailed fully 3D simulation and analysis of the parasitic capacitances is performed for the first time to study the impact of scaling and pitch spacing. Unlike planar devices, FinFET scaling does not always result in a straightforward performance improvement due to the current crowding effect and series resistance.**

Keywords-Multi-gate; FinFET; capacitance; scaling; 3D simulation

I. INTRODUCTION

MuGFET devices are suitable in sub-32 nm technology due to their excellent immunity to short channel effects and negligible junction capacitance which significantly reduces circuit delay [1]. However, in sub-100nm technologies, the effective capacitances do not reduce as predicted by the ITRS [2] because the parasitic capacitances do not scale as effectively. It was even reported in literature that when device is scaled beyond 18nm gate length, parasitic capacitances start dominating the effective capacitance [3]. To fully capture the scaling properties, one has to take the non-planar nature of the device geometry into account. As shown in the C_{gs} plot in Fig. 1, 2D simulation clearly overestimate the capacitance by ignoring the underlying bottom oxide layer and assuming that the device extends infinitely in the z-direction. In this work, full 3D device structure and doping profiles are incorporated for capacitance calculation. State-of-the-art process and device numerical simulator Taurus™ is used for forming the structure [4] and for capacitance extraction. The device prototype was then benchmarked with fabricated device from IMEC. With the use of calibrated and realistic physical device models, this work offers useful insights into the scaling properties of sub-100nm MuGFET device. In addition, the effect of fin pitch for multi fin device is also studied.

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II. 3D PROCESS SIMULATION AND DEVICE BENCHMARKING

A. 3D Process Simulation

A 3D process simulation was performed in Taurus™ emulating the full fabrication process. Key physical effects such as angle implantation, implantation damage, spike annealing, transient diffusion of dopants and defects are included [4]. Fig. 2 shows the MuGFET structure simulated by Taurus™. Two Arsenic implantations and one Phosphorous implantation were used for the source/drain doping and LDD formation [5]. Fig. 3 shows the 2D cut through middle of fin and source/drain, plotting As and P doping profile.

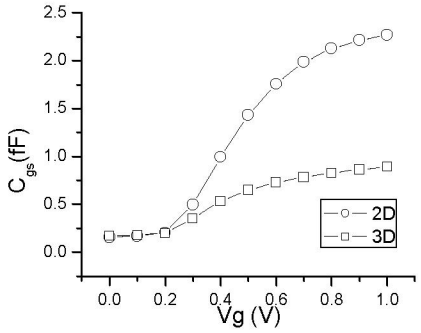


Fig.1: 2D model over predict the gate-source capacitance

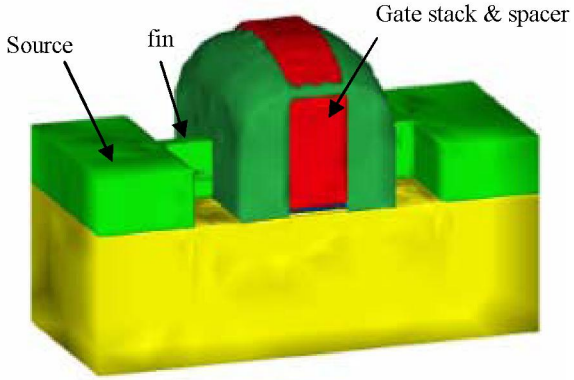
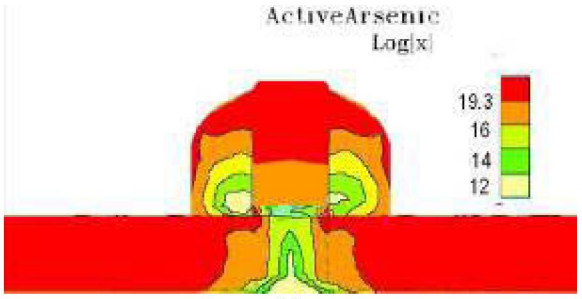
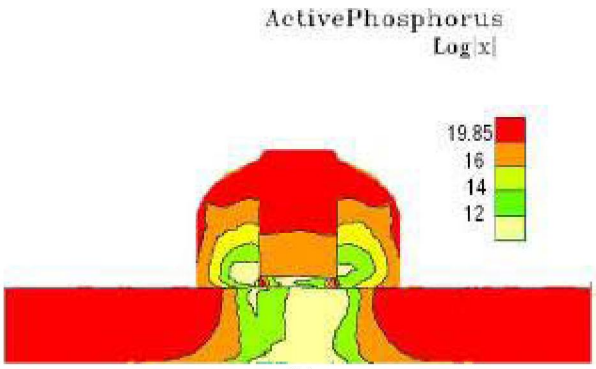


Fig.2: MuGFET structure simulated by Taurus 3D

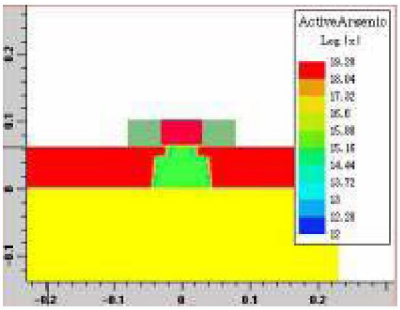


(a)

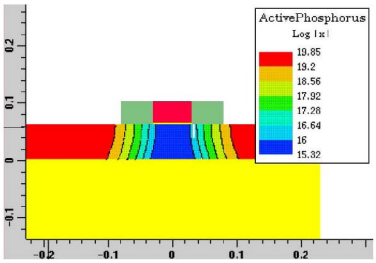


(b)

Fig.3: Active (a) As profile and (b) P profile plotted on 2D cut from process simulation



(a)



(b)

Fig.4: Active (a) As (b) P profile plotted on 2D cut at the fin center using Gaussian fitting

B. Bechmarking with Measurment Data

It is not possible to use an iterative process simulation to fit measurement data due to the formidable CPU time. Instead, the doping profile was fitted using a linear combination of Gaussians while maintaining the simulated structure. This method reproduces the profile with reasonable accuracy in agreement with 3D simulated structure in the regime with doping above 10^{15} cm^{-3} while simulation efficiency and convergence were greatly improved. The extracted doping profile and the fitted Gaussian profile are shown in Fig. 4.

The Gaussian doping and gate stack parameters were fine tuned based on experimental results and measurements. A novel gate stack was used in the device [7]. The work function and dielectric thickness was extracted by matching the gate capacitance of a sample fabricated device. An excellent fit was achieved by having 4 nm high-k dielectric and 4.75 eV work function for the gate (Fig. 5). The doping profile was then fine-tuned iteratively by fitting the simulated drain and gate electrical characteristics with experiment results. The device simulation included quantum effect, advanced mobility and recombination models [6]. Simulated and measured I_d-V_g curves are shown in Fig. 6.

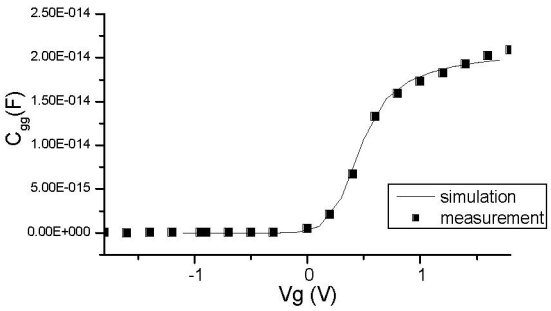


Fig.5: Gate work function and dielectric thickness fitting using C-V measurement data

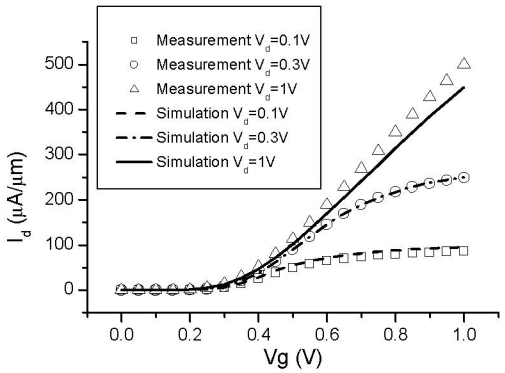


Fig. 6: Calibrated device gate characteristic
Blue: fabricated MuGFET, green: device physical model

III. RESULTS AND DISCUSSION

A. Inversion Charge Distibution Extraction

The inversion charge distribution for two devices of different gate lengths (L_g) and fin widths (T_{fin}) are plotted in Fig. 7 at different gate biases. Volume inversion with a single charge centroid at center of fin occurs for gate bias up to 0.5 V. As the gate voltage increases further, the centroid starts to split into two and moves towards the each of the fin sidewall surface

while the inversion charge density at the fin center remains relatively stable at a saturation value. It is clear that for fin width down to 8 nm the volume inversion indeed contributed to the superior turn-on performance in sub-threshold regime as described in the literature [8] but not after strong inversion. The plot also shows that the device with a thinner fin in which gate coupling is stronger has higher inversion charge density in strong inversion and its charge peaks are further from channel surface. This will also have a positive effect on current drive due to less surface roughness scattering.

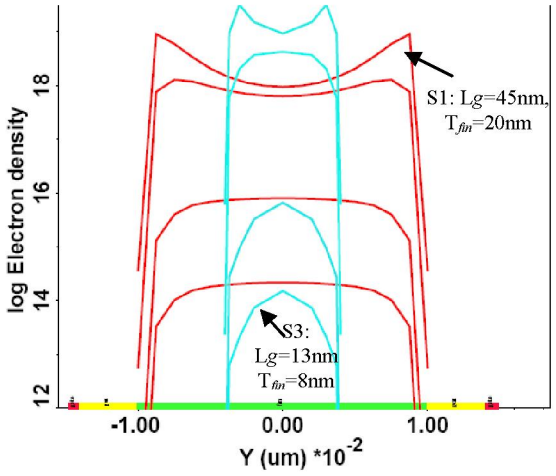


Fig.7: Electron density plotted along fin cross section at Vg=0.1, 0.2, 0.5, 0.9v
S1: Lg=45nm, T_{fin}=20nm *S2*: Lg=13nm, T_{fin}=8nm (y-axis is along the channel width)

B. Scaling Properties of MuGFETs

The calibrated device is scaled based on ITRS projections. The device specifications are described in Table 1.

The capacitance was extracted using AC device simulation. Fig 8 plots the C_{gs} and C_{gd} (in fF/um). Increase of capacitance due to T_{ox} reduction is only seen for device with fin width larger than 10 nm. This is predictable since volume inversion is more prominent in very thin channel and the charge peaks are further moved inside the fin. However, this advantage of smaller capacitance does not result in better speed because of the significantly larger series resistance. This is reflected by the CV/I curve in Fig 9 which shows the fastest device is in fact S2 with gate length of 35 nm (L_{eff}≈25 nm). We can conclude that aggressive scaling of a multiple gate device may not result in much incentive in terms of current and delay though the reduced capacitance can be useful for some applications.

Table 1: Scaled device detail

	Printed Lg (nm)	High-k Dielectric Thickness (nm)	Fin Length (nm)	Fin Width (nm)	Fin Height (nm)
Calibrated Device S	60	*4*	*260*	20	60
Scaled Device S1	45	*3*	*200*	15	45
Scaled Device S2	35	*2.5*	*180*	13	40
Scaled Device S3	25	*2*	*120*	10	30
Scaled Device S4	18	*2*	*100*	8	25

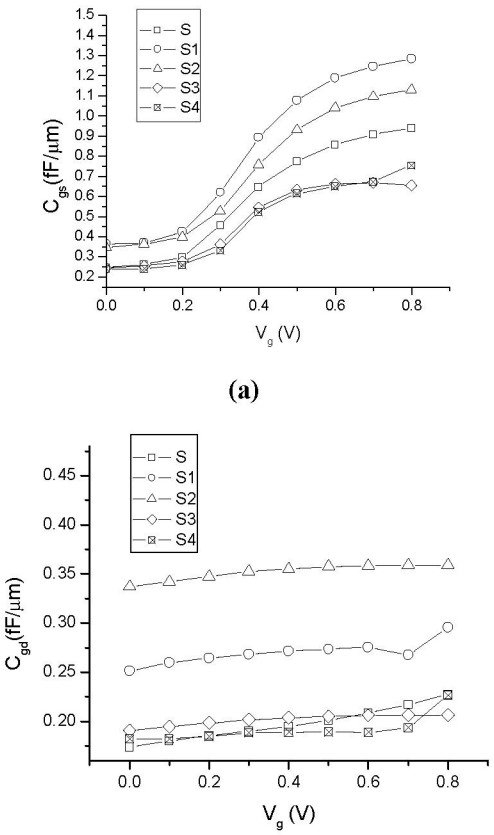


Fig.8: (a) C_{gs} (b) C_{gd} as a function of V_g for various scaled single fin device at V_d=0.8V

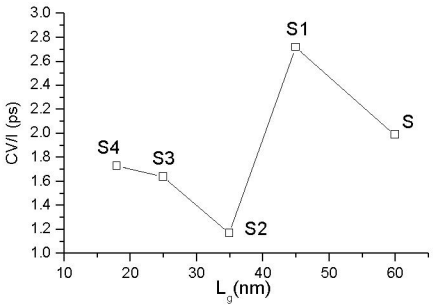


Fig.9: Estimated delay for scaled single fin device of various gate length (V_d=0.8V)

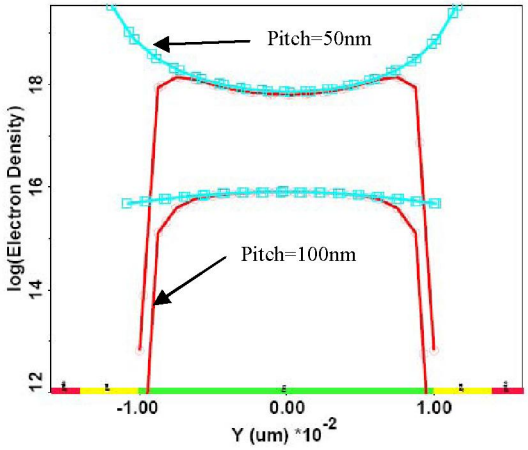
C. Pitch Effect of Multi-fin MuGFET

Due to aspect ratio constraint, the current drive of single fin is often too small for circuit application, thus multi-fin structure is more useful and practical. However, putting conducting channels in close proximity produces stronger fringing field affecting capacitance and channel charge distribution. These effects need to be carefully studied.

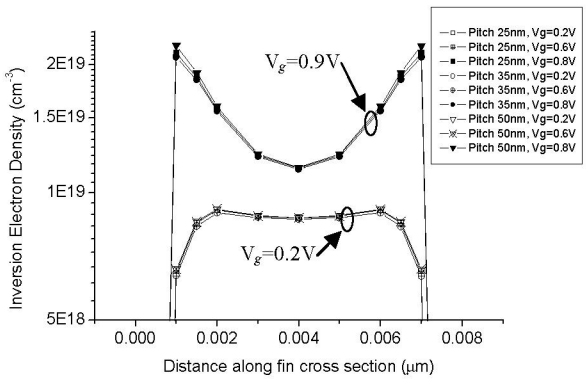
In the case of a wider fin width device, we found that as the fins are placed closer to each other the channel charge distribution is changed. Charge peaks actually shift from inside

the fin towards the fin surface and the number of inversion carriers available in the channel increases as shown in Fig. 10 (a). This shifting of electron peaks signals the formation of a larger gate field and reduction of dielectric EOT which both result in higher C_{gs} and C_{gd}. This trend can be clearly observed in Fig. 11 (a). Saturation current is found to increase by about 6%. As plotted in Fig. 12, over all normalized delay time is increased by ~25% as the pitch is reduced to less than 100nm as comparing with that of a single fin (approximately represent the case of infinite pitch).

However, devices of very thin fin width exhibit characteristic which is opposite to the above described (both C_{gd} and C_{gs}). In a multi-fin structure of W_{fin}=8nm, the channel inversion charge is found to be independent of pitch as shown in Fig. 10 (b). In this case, the change in capacitance is dominated by the strong fringing field from gate to source and drain. Due to the larger source/drain region required for higher pitch device, both C_{gs} and C_{gd} are larger as shown in Fig. 11 (b).

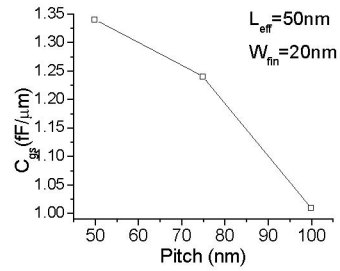


(a)

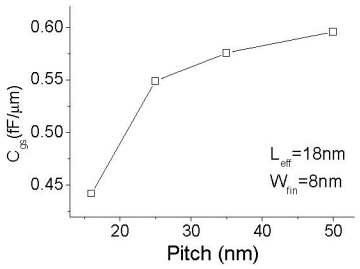


(b)

Fig.10: Electron distribution in the channel for (a) multi fin MuGFET with 20nm fin width and 100nm and 50nm pitch at V_g = 0.2 & 0.9V. (b) Multi fin MuGFET with 8nm fin width and 50nm, 35nm, and 25nm pitch at V_g=0.2, 0.6, 0.8V. The devices have L_{eff}=18nm, L_{fin}=80nm and W_{fin}=8nm.



(a)



(b)

Fig.11: Saturation C_{gs} against pitch for MuGFET with (a) fin width of 20nm (b) fin width of 8nm (both simulated at V_g=V_d=0.8V)

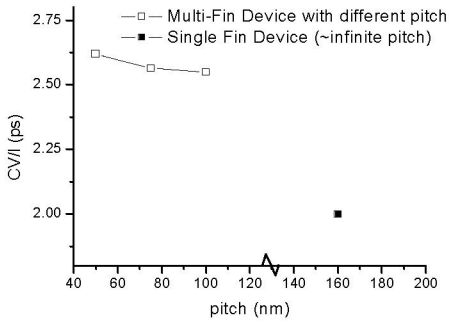


Fig.12: Estimated delay for multi-fin MuGFET with different fin pitch (V_g=0.8v) W_{fin}=20nm, L_g=60nm

IV. Conclusion

AC analysis in 3D device simulations shows increase in gate capacitance when fin pitch decreases for wide fin (~20nm) and increase of capacitance in device with narrower and shorter fin. The delay performance, however, is relatively uniform once the pitch is below 100nm. On the other hand, there is no monotonic trend for C_{gs}/C_{gd} of a single fin device on scaling.

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