Device Performance and Package Induced Self Heating Effects At Cryogenic Temperatures

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***Abstract*— As electronics that can work in space find wider applications, the modeling of devices that can efficiently operate under extreme conditions has been gaining great importance. Thus, we present a methodology for determining device performance details at cryogenic temperatures in conjunction with chip and package details. Using our technique that takes into account package thermal resistances and generated heat, we obtain possible temperature operating conditions for a device used in space applications. Moreover, to enable device operation at higher temperatures that would result in higher transconductances and operating speeds, we also offer methods for initial temperature boosting using heat kick-start circuits.**

Keywords: Cryogenic temperatures, self-heating, device modeling, chip modeling.

I. INTRODUCTION

Electronics for space applications should be designed for extreme temperature conditions ranging from the very low temperature of 2.7K, due to cosmic microwave background, to one-to-two hundred Kelvins for orbiting satellites [1]. Thus, to guarantee good device and circuit operation in these conditions, designers need to know how well the devices will perform at these temperatures, and what their final temperature will be after their initial turn-on. In this work, we provide a methodology that answers these two questions.

Since prohibitively costly external heaters that can pull temperature values to desired levels are less desirable in terms of power management, self-regulating circuits and chips need to be designed. This necessitates knowledge of device performance details including heat generation, and heat conduction from the device to the ambient. Specifically, calculation of device performance details provides heat generated by a device for given boundary temperature values. To find device boundary temperature values, we solve for heat conduction from that device to ambient. Therefore, to aid device and chip designs that can work in low space temperatures, we present a methodology for determining device performance details at cryogenic temperatures in conjunction with chip and package heat transfer details.

After the device is first turned on, it will reach an operating temperature value when heat generated is equal to heat conducted to outside. This may occur at more than one temperature value, opening possibilities for device operation at higher more efficient temperatures. However, having the device operate at the high temperature value might require additional circuitry that provides initial warming. Here, we also offer a design for such a microheater that can be used to provide initial device heating. This microheater can be used until the device is pulled into a region where it can reach a high steady state temperature, and thus regulate itself.

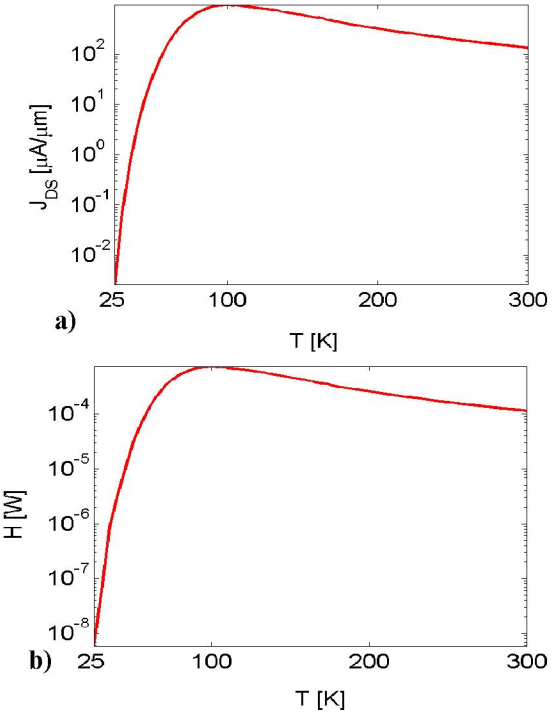

Figure 1. Calculated **a)** current density and **b)** heat generated of a 0.13μm N-MOSFET. (V_{GS}= V_{DS}=0.7V)

II. DEVICE PERFORMANCE AND MIXED-MODE THERMAL MODELS

A. Device Performance Model

To obtain device performance details shown in Fig. 1, we solve the coupled semiconductor equations including the Poisson equation, electron and hole current equations, and the heat flow equation. We list these equations below in the aforementioned order:

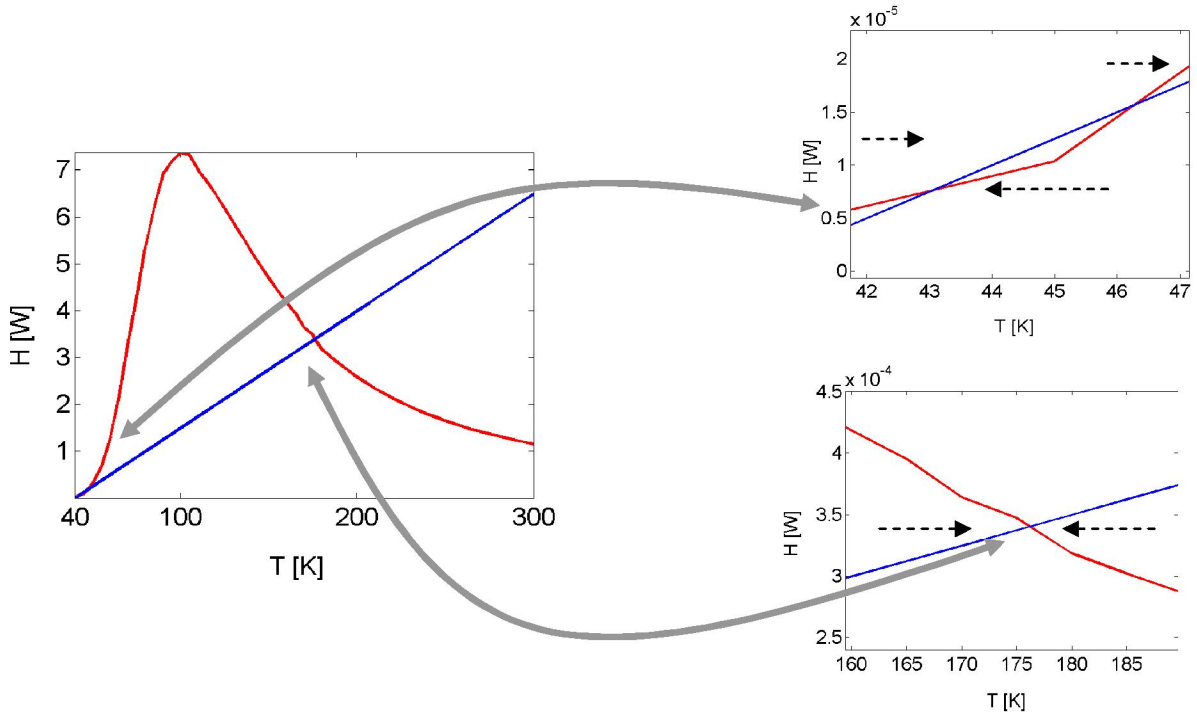

Figure 2. Heat generated by a device and the resistive linear thermal current. Intersections (zoomed in on the right) are operating temperature conditions. (T_A=40°K, R_c=4x10^5 K/W).

$$\nabla^2\phi = -\frac{q}{\varepsilon}\left(p - n + D\right) \tag{1}$$

$$\frac{\partial n}{\partial t} = \nabla.\left(-n\mu_n\nabla\phi + \mu_n V_{TH}\nabla n\right) + GR_n \tag{2}$$

$$\frac{\partial p}{\partial t} = \nabla.\left(p\mu_p\nabla\phi + \mu_p V_{TH}\nabla p\right) + GR_p \tag{3}$$

$$C\frac{\partial T}{\partial t} = \nabla.\left(\kappa\nabla T\right) + H \tag{4}$$

Above, H is Joule heating at each mesh point, and therefore has units of W/cm^3. The integral of H over the device volume gives the total heat generated by that device. In addition, we explicitly change the values of mobility, $\mu(T)$, intrinsic carrier concentration, $n_o(T)$, net ionized dopant concentration, $D(T)$, saturation velocity, $v_{sat}(T)$, thermal voltage, $V_{TH}(T)$, bandgap of silicon, $E_g(T)$, and the thermal diffusion constant, $\kappa(T)$ according to the device operating temperature and lattice temperature [2-4].

$$\mu(T) = \mu(T_o)\left(\frac{T}{T_o}\right)^{-2.5} \tag{5}$$

$$n_o(T) = n_o(T_o)\left(\frac{T}{T_o}\right)^{1.5} e^{\left(-E_g(T)/2kT\right)\left(1-\left(\frac{T}{T_o}\right)\frac{E_g(T_o)}{E_g(T)}\right)} \tag{6}$$

$$D(T) = \frac{N_d}{1+\frac{g_d n(x,T)}{N_C e^{-E_D/kT}}} - \frac{N_a}{1+\frac{g_a p(x,T)}{N_V e^{-E_A/kT}}} \tag{7}$$

$$v_{sat}(T) = v_{sat}(T_o)\left(\frac{1+e^{-T/2T_o}}{1+e^{-1/2}}\right) \tag{8}$$

$$V_{TH}(T) = V_{TH}(T_o)\left(\frac{T}{T_o}\right) \tag{9}$$

$$E_g(T) = E_g(T_o)\left(1 - 2.4\text{x}10^{-4}(T - T_o)\right) \tag{10}$$

$$\kappa(T) = \kappa(T_o)\left(\frac{T}{T_o}\right)^{-4/3} \tag{11}$$

Since incomplete ionization given in (7) greatly affects device performance at cryogenic temperatures, we here explain parameters used to compute its value. Specifically, N_C and N_V are the effective densities of state at the conduction and valence band edges. Also, E_A and E_D are the energy differences between the acceptor and donor levels, and the valence and conduction bands, respectively. In our study, we take them as both equal to 45meV. Furthermore, the net ionized dopant concentration is related to the electron $n(x,y,T)$ and hole $p(x,y,T)$ concentrations, and the net acceptor N_a and donor N_d levels (ionized and unionized together). Above, g_d and g_a,

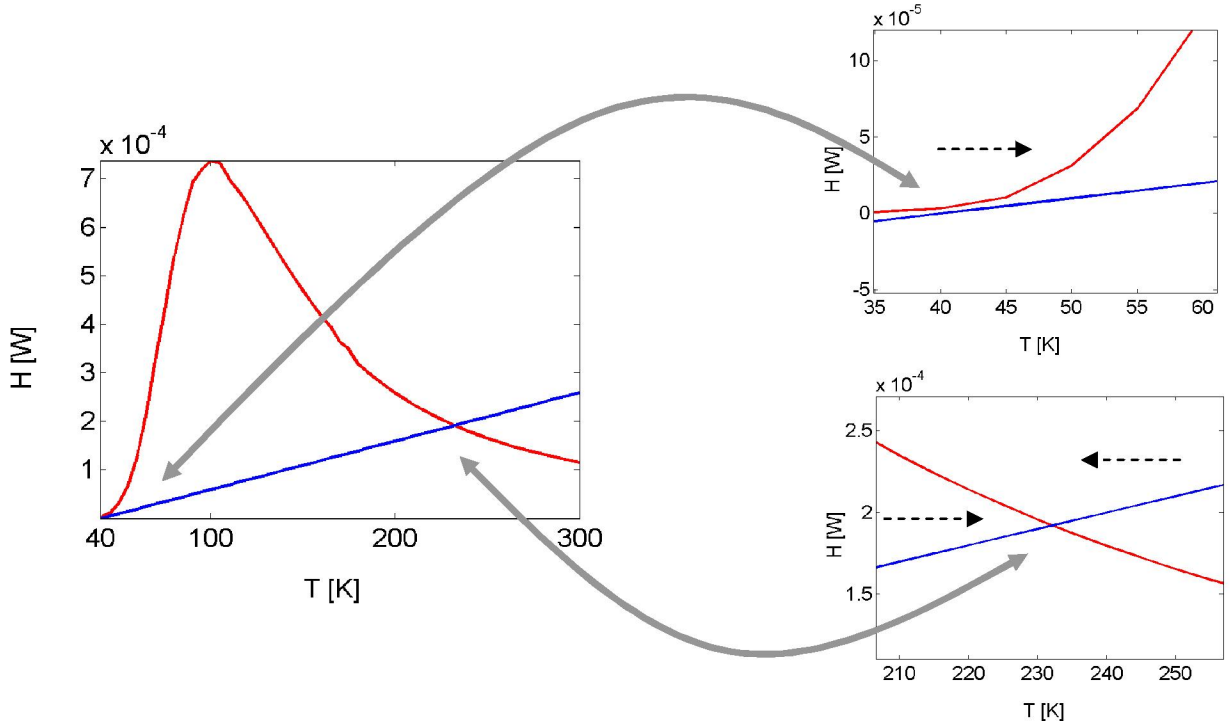

Figure 3. Heat generated by a device and the resistive linear thermal current. Intersections (zoomed in on the right) are operating temperature conditions. (T_A=40°K, R_c=1x10^6 K/W)

which are fitting parameters for the donors and acceptors, are 2 and 4, respectively.

Our analyses indicate that around room temperature down to approximately 100 degrees Kelvin, device performance is mostly affected through changes in carrier mobility, saturation velocity and built-in boundary potentials. As temperature increases from 100°K, mobility and saturation velocity decrease, resulting in lower current values. However, change in built-in boundary potentials results in effective threshold voltage lowering as temperature rises, which increases current. At cryogenic temperatures from 100°K down to 20°K, device performance degrades due to incomplete ionization and low intrinsic carrier concentration. Freeze-out of dopants especially at the source and drain terminals adversely affects drive currents, which leads to dramatic current drops as temperature decreases, as shown in Fig. 1.

Our goal is to find out how much power must be added externally to achieve acceptable device performance and to see if unaided power dissipation in the circuit can be sufficient to create sustained device operation.

B. Mixed-Mode Device-Chip Model

We determine device performance including device Joule heating figures for given boundary temperature values. However, we need to solve a lumped thermal equation for that device to calculate a boundary value for given device Joule heating. Therefore, we iterate between the device and chip levels to find self-consistent device heating and device temperature values. This temperature operating point is where heat generated is equal to heat conducted to outside via chip and package.

To obtain effects of chip and package on device temperature, we first calculate a value for the equivalent thermal resistance between a device and the ambient. It has been shown that one appropriate value for that resistance is 4x10^5 K/W [2]. Then, we solve self-consistently for the generated heat and thermal current through that resistance using the electrical analogy derived in [2].

$$\Sigma H = \frac{T - T_A}{R_C} \tag{12}$$

Here, ΣH is the heat generated by the device, which is equivalent to the integrated Joule heating over the device volume; T is the device temperature; T_A is the ambient temperature; R_C is the Thevenin equivalent thermal resistance seen from that node including chip and package. Left-hand-side of (12) is the source term, which is the total heat generated by a device. Right-hand-side of (12) shows how much heat can be conducted to outside. When heat generated, or the source term, is equal to the resistive heat flow, we have a steady state operating temperature point.

III. Simulation Results

We first find temperature versus heat generated curve of a 0.13μm N-MOSFET at V_{GS}= V_{DS}=0.7V to be used in (12). This

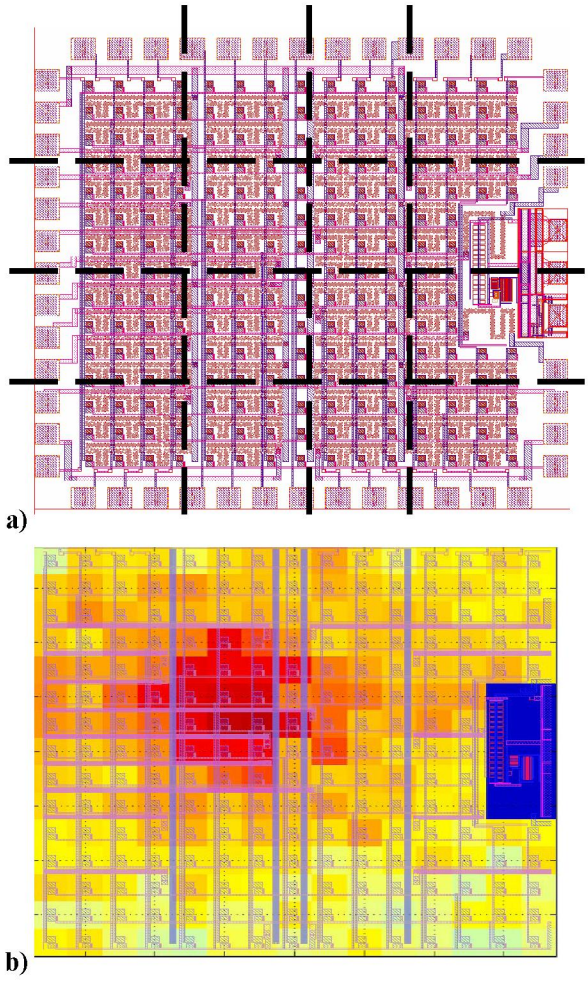

Figure 4. **a)** Our fabricated 2.2mm by 2.2mm chip with 4x4 differential microheater blocks, shown with dashed lines. **b)** Induced temperatures by turning the second row-second column resistor block on. Darker middle region is about seven degrees warmer than the lighter regions.

requires coupled solution of (1) to (4) using the parameters with temperature dependencies given in (5) to (11). We next calculate the heat flow on R_C=4x10^5 K/W for T_A=40°K, which is the approximate ambient temperature for our satellite application. Then, we determine the temperature operating conditions graphically, as shown in Fig. 2. It shows that we have three intersections at about 43°K, 46°K and 175°K. Moreover, 43°K and 175°K are stable operating temperature points because generated heat is higher than heat transferred to outside when device temperature is lower than these values, and vice versa if it is lower. If the temperature is lower than these operating points, then the device will keep generating more heat than the chip can conduct outside, which will result in temperature increase. Once the temperature is higher than these values, then the heat conduction, which is at a higher rate than heat generation, via the chip and package will keep the temperature from increasing further. If we do not use additional circuitry, a device, initially sitting at ambient temperature, will be at 43°K. Therefore, if we want the circuits to operate at the higher stable operating point of 175°K, a temperature boosting circuit to push the initial device temperature higher than the unstable operating point of 46°K is needed. In that case, the device will be at self-regulated 175°K, with higher drive currents.

In Fig. 3, we graphically solve (12); however, R_C is 1x10^6 K/W, which is higher compared to the previous case. It shows that for a higher Thevenin equivalent resistance, we do not need a heat kick-start circuit. Likewise, for a lower Thevenin equivalent resistance, we have one operating point, which is close to the ambient. In this case, even if a heat kick-start circuit is utilized, the operating temperature will not increase that much above the ambient value.

In Fig. 4a, we show the differential microheater and temperature sensors we had fabricated through MOSIS, which is a fabrication service [5]. It contains sixteen heater blocks separated by the dashed lines shown in Fig. 4a. By turning a specific block on, we provide temperature boosting for a device in a specific location. Figure 4b shows the effects of such differential heating. We turned the second column-second row poly resistor block on. (First column-first row block is at the upper left corner.) We then measured the temperature using the diode temperature sensors, and next plot the thermal map in Fig. 4b, where all temperatures were recorded and mapped except for the dark area on the right. The recorded temperatures under the block that was on is approximately seven degrees warmer than the lighter far corners. In addition, we have non-uniformity in our temperature due to non-uniformity of the medium that conducts heat. The inhomogeneous distribution of metal and polysilicon lines above the substrate causes the slight bends in isotherms.

In summary, we provide means to calculate device performance at cryogenic temperatures. Also, we determine package induced self-heating effects for that device. Additionally, we include differential microheater circuits for temperature boosting applications.

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