Electron Transport at Technologically Significant Stepped 4H-SiC/SiO_2 Interfaces

G. Pennington, S. Potbhare, J. M. McGarrity, and N. Goldsman
Dept. of Electrical and Computer Eng.,
University of Maryland
College Park, MD 20742, U.S.A.
(garyp, neil)@glue.umd.edu

A. Lelis
U.S. Army Research Laboratory
Adelphi, MD 20783, U.S.A.

C. Ashman
HPTi, Reston, VA 20910, U.S.A.

***Abstract*—The impact of interface steps on electron transport in 4H-SiC MOSFETs is investigated. Steps are found to cause a large increase in roughness scattering leading to anisotropy in the low-field mobility. An increase in phonon scattering, due to variations in the channel depth, is also predicted. Monte Carlo transport simulations show that interface steps lead to degradation of the high-field phonon-limited mobility. Results are important considering the technological significance of 4H-SiC in high temperature, high power electronics.**

Keywords- SiC; interface steps; electron transport; roughness scattering; phonon scattering; Monte Carlo simulation

I. INTRODUCTION

Silicon Carbide (SiC) is a material with significant applications in high power, high temperature electronics. The 4H polytype is of particular interest due to its large band gap and large saturation velocity. Epitaxial growth of device-quality 4H-SiC is typically achieved by step-flow growth, with the surface offset from the (0001) plane by 8° towards the [1120] direction. This creates a nanostep morphology along the surface. These nanosteps, shown in Fig. 1, often consist of the bunching of multiple single Si-C bilayer steps [1]. Also, larger macrosteps may also occur in 4H-SiC as a result of surface reconstruction or significant step bunching [2].

When compared to a typical Si surface roughened by island growth, a stepped surface can lead to an increased roughness along the step train (x in Fig. 1). This leads to an anisotropic interface roughness scattering rate, with increased backscattering along x. Also, by varying the channel depth, interface roughness in a MOSFET will increase the carrier-phonon scattering rate. The effect would be enhanced in the presence of interface steps. As SiC is targeted for high temperature applications, phonon related effects are very important.

In this work, we consider the characteristics of electron transport in the presence of stepped morphologies at the SiC/SiO_2 interface. We consider interface roughness resulting from both nano and macrostep distributions and compare with a typical Si/SiO_2 interface roughness. This investigation is important since little is currently know of the effects of interface steps on the transport properties of lateral SiC MOSFETs.

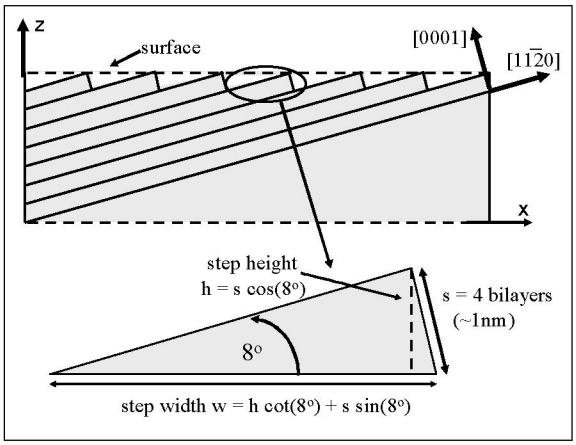

Figure 1: Nanostep Geometry

II. 4H-SIC SURFACE MORPHOLGY

Stepped surface morphologies in 4H-SiC result from 1) step-flow growth and 2) surface reconstructions. The first process produces a distribution of nanosteps, one to eight Si-C bilayers (0.25 to 2 nm) in height, along the surface. Fig. 1 shows a surface of 4 bilayer steps, but a distribution of step heights will generally occur. Typically, most nanosteps in the distribution are comprised of either 4 or 2 bilayers on the Si terminated face [1]. This distribution of nanosteps is labeled as 4-2 throughout this work. For comparison, we also consider a non-uniform nanostep distribution with equal likelihood of one through eight bilayer steps. The 4-2 and non-uniform nanostep distributions are shown in Fig. 2.

In addition to nanosteps, larger surface steps are often observed in 4H-SiC [2]. These steps are typically referred to as macrosteps although they may still have nanoscale dimensions. Macrosteps are likely the result of surface reconstructions or nanostep bunching, and formation is sensitive to processing conditions and implantation [2]. We consider an experimental distribution of Si-face macrosteps shown in Fig. 2.

Here we investigate and compare electron transport in the presence of 4H-SiC/SiO_2 interface variations in accord with

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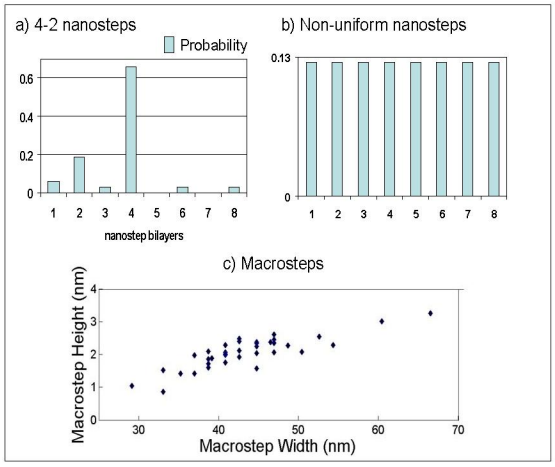

Figure 2: Step Distributions ref. [1] and [2]

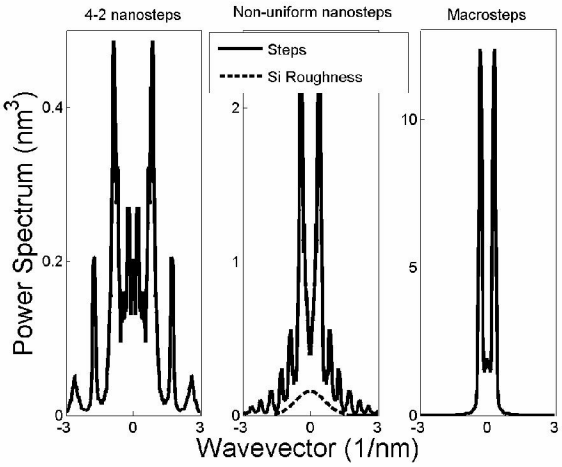

Figure 3: 1-D power spectra

the surface step distributions in Fig. 2. As shown in Fig. 1, steps propagate along x, the [1120] direction. Variations will also occur along y, the [1100] direction, as a result of step meandering, step splicing, and other processes. Since a comparison with a Si/SiO_2 interface is informative, surface variations along y are generated using a typical correlation length observed in Si (L_y=2.2nm). With step heights $\Delta(x)$ calculated from the distributions in Fig. 2, the 2-dimensional 4H-SiC/SiO_2 interface power spectrum is therefore given by

$$S(\bar{q}) = L_y \exp\left(-q_y^2 L_y^2 / 4\right) \int \exp(iq_x x)\left[\sum_{x'} \Delta(x')\Delta(x'-x)\right] dx \quad (1)$$

as a function of wavevector q=(q_x,q_y). The integral term is S_x, the 1-dimension power spectrum along the step train. S_x for each step distribution is shown in Fig. 3. The macrostep power spectrum has a larger central peak when compared to the nanosteps since the steps are larger. However, the greater uniformity of the nanosteps allows for a broader spectrum with many side peaks. For a comparison with the roughness of Si, a power spectrum is included using an exponential roughness with parameters (L_y, Δ_{Si}=0.2nm). The surface steps produce a significantly larger and broader spectrum. As we investigate carrier transport in the presence of interface steps, a comparison will be made with the isotropic roughness of a typical Si surface.

III. Interface Roughness Scattering

The scattering rate due to interface steps in a 4H-SiC MOSFETs is determined using Fermi's Golden Rule. Using methods previously developed for an isotropic roughness [3], the elastic scattering rate is

$$\Gamma(\bar{k}) = \frac{m^* F_s^2}{\pi\hbar^3} \int \frac{q^2}{(q-q_s)^2} S(\bar{q}) d\theta \quad (2)$$

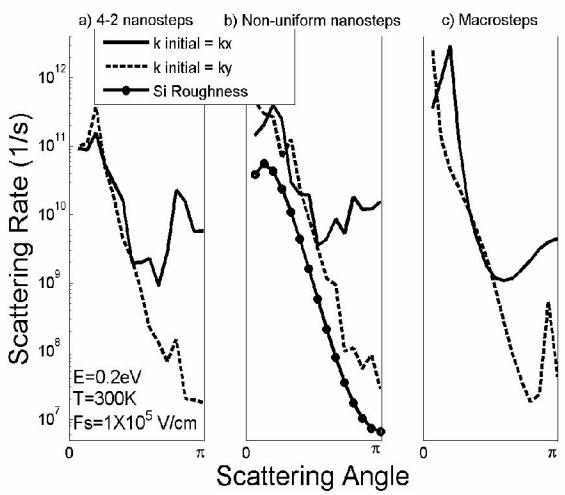

Figure 4: Scattering rate Γ vs. angle θ

This represents scattering from an initial state with 2 dimensional momentum ħk to a final state ħ(k±q). The scattering angle is θ. Also, F_s, m*, and q_s are the effective perpendicular surface field, effective mass, and screening wavevector [4] respectively. To investigate transport anisotropy resulting from interface steps, band structure anisotropy is not considered and m*=0.4m_e, where m_e is the electron mass. Scattering will depend on the interface morphology through the power spectra S given in (1).

In Fig. 4 the scattering rate in (2) is examined as a function of scattering angle. Here we consider a carrier energy of 0.2eV with F_s=1X10^5 V/cm at room temperature. The direction of initial carrier momentum k is specified either along the step train (x) or along the step edges (y). Considering distributions of interface nanosteps and macrosteps, in each case backscattering is enhanced when k is initially along x. Here the power spectrum S(k_x=2k) is large allowing for significant backscattering. When the isotropic Si power spectrum is used,

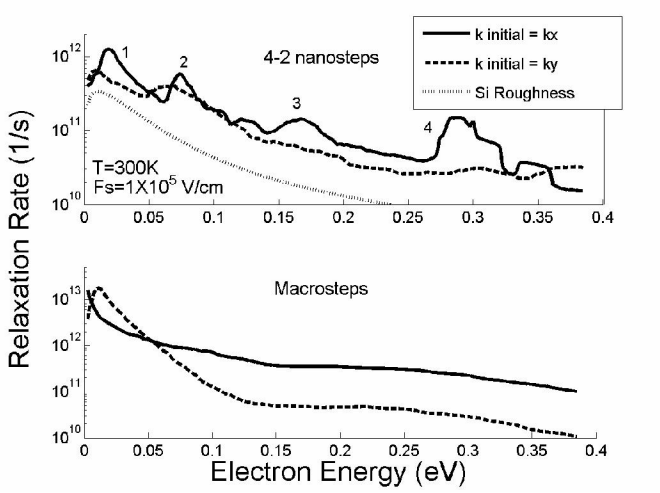

Figure 5: Momentum relaxation rate

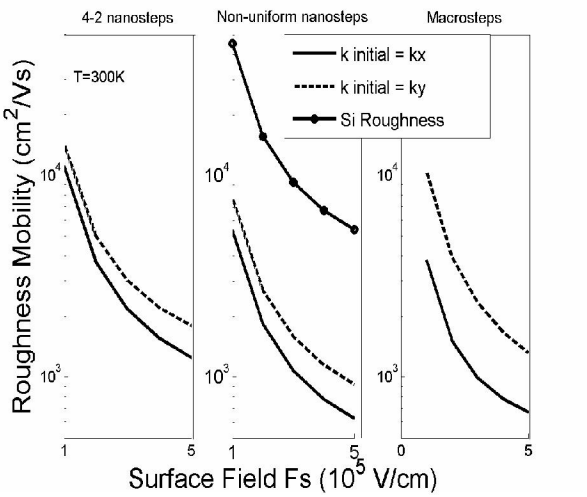

Figure 6: Low-field Roughness mobility

weak backscattering occurs. Backscattering is important since it increases momentum relaxation leading to mobility degradation.

Further insight is gained by considering the momentum relaxation rate (including a factor of 1-cos(θ) in the integrand of (2)). When the initial carrier momentum is along x, peaks in the momentum relaxation rate are observed corresponding to strong backscattering when the carrier energy is in resonance with the nanostep width. The effect can be seen when a large majority of steps are similar, as in the case of the 4-2 distribution. The 4 resonance peaks in Fig. 5 occur when the electron energy is a multiple of $\hbar^2\pi^2/2m^*w^2$, where the nanostep width is w=7.2nm for 4 bilayers steps. These resonance peaks are not observed when the initial carrier momentum is along y. Also, a comparison with the silicon power spectrum indicates a larger momentum relaxation rate when nanosteps are considered. For large carrier energies (E>0.2eV), the momentum relaxation and thus mobility degradation is more than 10X larger with nanosteps.

The momentum relaxation rate for larger macrosteps is also shown in Fig. 5. No resonance peaks are observed due to the random nature of the step distribution. However, the momentum relaxation rate is found to be very large, even at large carrier energies where it is comparable with typical surface phonon scattering rates.

The momentum relaxation rate can be used to determine the low-field roughness mobility. Results are shown in Fig. 6. As expected, steps produce transport anisotropy at the surface. Anisotropy is found to be larger when macrosteps are considered. The mobility degradation is typically a factor of 10X larger when compared to the case of an isotropic surface roughness as in silicon

IV. Interface Phonon Scattering

For carrier scattering from an initial state (k,E) to a final state (k',E'), the interface phonon scattering rate takes the typical form [4]

$$\Gamma(\vec{k}\to\vec{k}') = \frac{\pi\hbar D^2 q^2}{\rho|E'-E|} Dos(E')\left\{N(|E'-E|)+\frac{1}{2}\pm\frac{1}{2}\right\}\cdot\frac{1}{W} \qquad (3)$$

Here D is the deformation potential, ρ is the 3-dimensional mass density, and N is the phonon number density. The density of final carrier states is given by Dos(E'). The rate depends on the effective depth (W) of the MOSFET inversion channel. Here we consider the quantum limit with only one subband in the inversion layer. The wavefunction perpendicular to the interface along z is [4]

$$\Psi(z) = \sqrt{\frac{b^5}{24}} z^2 \exp\left(-bz/2\right), \qquad b \propto \frac{1}{W} \qquad (4)$$

Allowing for variations in the wavefunction due to variations in the inversion channel width $b(x,y)=b_0+\Delta r(x,y)\cdot db/dW$, the phonon scattering rate is $\Gamma+\Delta\Gamma$ where

$$\Delta\Gamma(\vec{k}\to\vec{k}') = \frac{\pi D^2 k_B T}{\hbar\rho V_p^2}\cdot Dos(E')\frac{1}{W}\left[\frac{3\int d\vec{Q}\cdot S(\vec{Q})}{8\pi^2 W^2}\right] \qquad (5)$$

Here V_p is the phonon velocity. The term in square brackets accounts for phonon scattering due to variations in the channel depth across the interface. As Γ in (3) involves only one phonon, ΔΓ may involve many phonons, with the only restriction being that the phonon bath has an energy shift of E-E'. There are many possible combinations of phonons that could be involved. Changes in the momentum of the phonon bath are not constrained since scattering is coupled to the interface morphology.

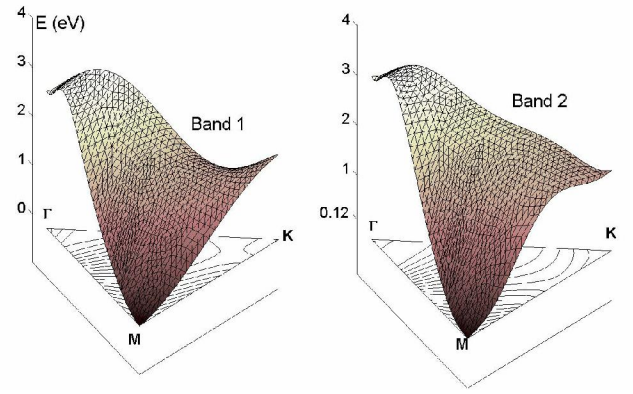

Figure 7: Irreducible wedge band structure

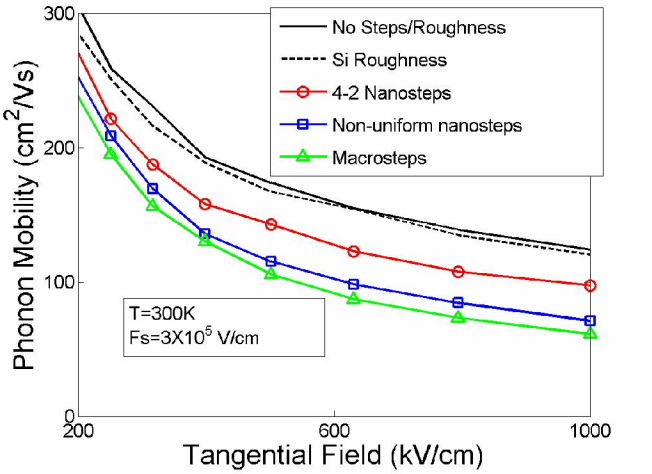

Figure 8: Surface phonon mobility at stepped interface

To determine the effects of interface steps on high-field, high temperature transport in 4H-SiC MOSFETs, we employ full-band Monte Carlo methods [5]. For the interface band structure, the first 2 bulk conduction bands are used in the (Γ,M,K) plane. This is a reasonable approximation since the bulk band structure does not vary significantly perpendicular to this plane. The band structure is determined with density functional theory using the ABINIT code [6]. Only the first subband perpendicular to the interface is considered. The band structure is determined at mesh points in the irreducible 4H-SiC wedge given in Fig. 7. Interpolation between mesh points allows calculation of E(k), k(E), Dos(E), and carrier velocities during the Monte Carlo transport simulations [5].

Results for the 4H-SiC high-field mobility limited by surface phonon scattering are shown in Fig. 8. The deformation potential is set at D=9eV and the tangential field is along y ([1100]). The mobility depends on temperature and field, here we use T=300K and F_s=3X10^5 V/cm. A significant degradation in surface phonon mobility occurs when interface steps are included. This effect increases as the steps increase in size or become non-uniform.

V. Conclusion

4H-SiC has many potentially significant technological applications in high temperature, high power electronics. Current growth methods lead to surface steps and subsequent nanosteps at the SiC/SiO_2 interface in 4H-SiC MOSFETs. Furthermore, larger macrosteps, resulting from reconstruction or step bunching, are often observed.

In this work we have investigated the impact of these steps on the electron transport properties of the SiC/SiO_2 interface. The interface morphology has been accounted for by calculation of the interface power spectrum in the presence of nano and macrosteps. The electron-step scattering rate is then developed including the spectra of various surfaces. In comparison with typical roughness parameters used for Si, results indicate a large increase in interface roughness scattering when steps are present. Steps allow enhanced momentum relaxation along the step train direction, leading to low-field transport anisotropy. Such effects have been measured experimentally [7].

We have also developed a correction to the interface phonon scattering rate which accounts for variations in the 4H-SiC MOSFET channel depth resulting from interface roughness. Although the effect is found to be weak when typical Si roughness parameters are used, results indicate a significant increase in phonon scattering when interface steps are present. Steps are predicted to degrade the high-field mobility at sufficiently high gate voltages. This result is likely to have important implications in MOSFETs operating at high bias.

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