A semi-analytical model for the subthreshold behavior of SOI FinFLASH structures

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***Abstract*— In this paper we present an original semi-analytical model for the subthreshold electrical behavior of complex 3D structures as the SOI FinFLASH devices. This physically-based model, which does not need any fitting parameter, solves the Poisson equation for a fin covered by trapped charges in the active dielectrics. The analytical results are compared with fully 3D numerical simulations and a good agreement is obtained down to fins with very small feature sizes (order of tens of nm). This model can be efficiently used to gain information on important cell electrical behaviors as the threshold voltage shift ΔV_{th} and the subthreshold slope factor S.**

I. Introduction

The FinFLASH device in trigate ($W \approx H$, see Fig. 1) or double-gate ($H \gg W$) configuration is currently investigated as one of the most promising solutions to replace conventional planar FLASH structures beyond the 32 nm technology node[1]-[2]. The main advantages of the FinFLASH device are its compact layout, moreover fully compatible with future generations of multi-gate CMOS, and its excellent electrical performance due to the enhanced coupling between the gate and the active channel. In this frame, it is today of utmost importance to provide a simple approach which allows us to describe the most important electrical parameters of the memory operation without appealing time consuming 3D numerical simulations.

In this paper we present 3D fully numerical simulations of FinFLASH devices (Fig. 2a) to substantiate our simpler analytical approach for the comprehension of the electrical behavior of such complex structures (see Fig. 2b). The comparison will be focused on the subthreshold electrostatics (Fig. 3) as well as on the electron transport (see Fig. 4 and Fig. 5). In the end we will analyze the limit of validity of our model in terms of doping level (see Fig. 7) and minimum feature sizes of the fin.

II. Model for electrostatics and transport

The bases of the physics of our model are herewith detailed. *The model solves the potential of a FinFLASH device,* Ψ_{FFLASH}, *as the sum of the potential of a FinFET fresh device,* Ψ_{FFET}, *plus the potential due to the trapped charges around the fin* $\Psi_{\mathrm{q-tot}}$. The superposition principle can be used if the impact of mobile charges is neglected, therefore the device is operated in the *subthreshold* region.

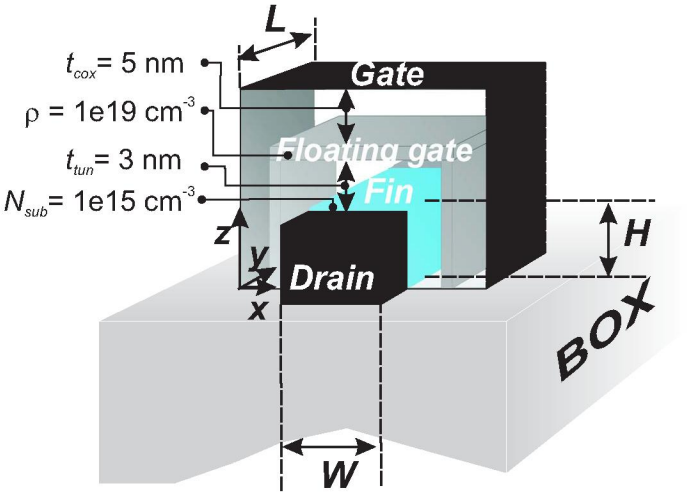


Fig. 1. Plot of the modeled SOI FinFLASH structure. Relevant features used both in the model and in 3D TCAD simulations are highlighted.

The model starts from the solution of the Laplace equation for Ψ_{FFET} in the FinFET space domain Ω (see Fig. 2b) with mixed conditions on the boundary Γ [3]. Ψ_{FFET}, indeed, is the potential distribution of a non-doped fin where mobile charges are neglected and the control oxide region is considered as an equivalent silicon region with proper thickness, in order not to treat mathematically the Si/SiO_2 interface. The source and drain are treated as perfect metals. Thus Ψ_{FFET} solves the following Laplace problem:

$$\begin{cases} \Delta\Psi_{\mathrm{FFET}} = 0 & & \text{in } \Omega \\ \psi_{tg} = V_G - V_{FB} & \psi_{rg} = V_G - V_{FB} & \\ \psi_{lg} = V_G - V_{FB} & \psi_S = V_{bi} & \text{on } \Gamma \\ \psi_D = V_{bi} + V_{DS} & d\psi_{BOX}/dz = 0 & \end{cases} \quad (1)$$

where ψ_{tg}, ψ_{rg}, ψ_{lg} are respectively the top, right and left gate potentials, ψ_{BOX} is the potential at the interface silicon/BOX, ψ_S and ψ_D are respectively the source and drain potentials (see Fig. 2b).

Then we treat separately the impact of a point trapped charge,

Ψ_q. Thus Ψ_q solves the following Poisson problem:

$$\begin{cases} \Delta\Psi_q = -\frac{q}{\epsilon_{si}}\delta(x-x_0)\delta(y-y_0)\delta(z-z_0) & \text{in } \Omega \\ \psi_{tg}=0 \quad \psi_{rg}=0 & \\ \psi_{lg}=0 \quad \psi_S=0 & \text{on } \Gamma \\ \psi_D=0 \quad d\psi_{BOX}/dz=0 & \end{cases} \tag{2}$$

where $\epsilon_{si(/ox)}$ is the silicon(/oxide) permittivity, δ is a Dirac Delta function of the coordinates of the charge x_0, y_0, z_0. We originally used the *Green's function method* to find an analytical solution to the point charge potential Ψ_q in a 3D domain [4], where the mixed boundary conditions are properly considered. In particular the Neumann condition at the BOX interface is obtained through the imposition of a fictitious charge having the same sign of the actual charge, mirrored with respect to the plane at $z=0$ (see Fig. 2b).

Thus for a charge q located at (x_0, y_0, z_0), the potential Ψ_q in (x, y, z) is described by the following Fourier series:

$$\Psi_q = \frac{-16q}{\epsilon_{si} L W_{\text{eff}} 2H_{\text{eff}}} \sum_{m,n,p}^{\infty} \frac{\sin\left(\frac{p\pi}{2}\right)\sin\left(\frac{m\pi x_0}{W_{\text{eff}}}\right)\sin\left(\frac{n\pi y_0}{L}\right)\cos\left(\frac{p\pi z_0}{2H_{\text{eff}}}\right)}{m^2/W_{\text{eff}}^2 + n^2/L^2 + p^2/4H_{\text{eff}}^2} \cdot \sin\left(\frac{m\pi x}{W_{\text{eff}}}\right)\sin\left(\frac{n\pi y}{L}\right)\cos\left(\frac{p\pi(z-H_{\text{eff}})}{2H_{\text{eff}}}\right), \tag{3}$$

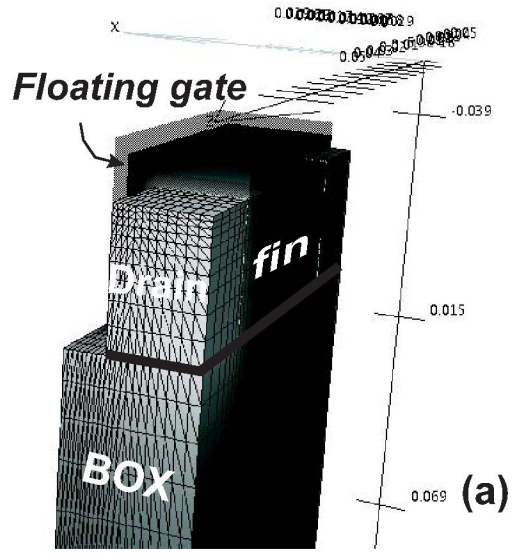
where $W_{\text{eff}} = W + 2\frac{\epsilon_{si}}{\epsilon_{ox}}(t_{tun}+t_{cox}+t_{ch})$, $H_{\text{eff}} = H + \frac{\epsilon_{si}}{\epsilon_{ox}}(t_{tun}+t_{cox}+t_{ch})$, W and H are the width and height of the fin, while t_{tun}, t_{cox}, t_{ch} are the tunneling oxide, control oxide and trapping medium thicknesses, as shown in Fig.1.

The impact of each point charge is afterwards integrated over the space domain to obtain the analytical solution for the potential of a *uniform distribution* of charges around the fin $\Psi_{q-\text{tot}}$.

Once the potential Ψ_{FFLASH} of the fin is known, the drain current is calculated through the numerical integration of the electron current density J along the dimensions of the fin, where we assumed a Boltzmann distribution for mobile charges and the Fermi energy level gradient negligible in the xz transversal plane. We obtain:

$$I_{DS} = -KT\mu n_i \frac{1-\exp(-qV_{DS}/KT)}{\int_0^L \frac{dy}{\int_0^W dx \int_0^H dz \exp(q\Psi_{\text{FFLASH}}/KT)}}, \tag{4}$$

where K is the Boltzmann constant, T is the lattice temperature, μ is the average electron mobility, n_i the intrinsic electron concentration and V_{DS} is the drain-to-source reading voltage.



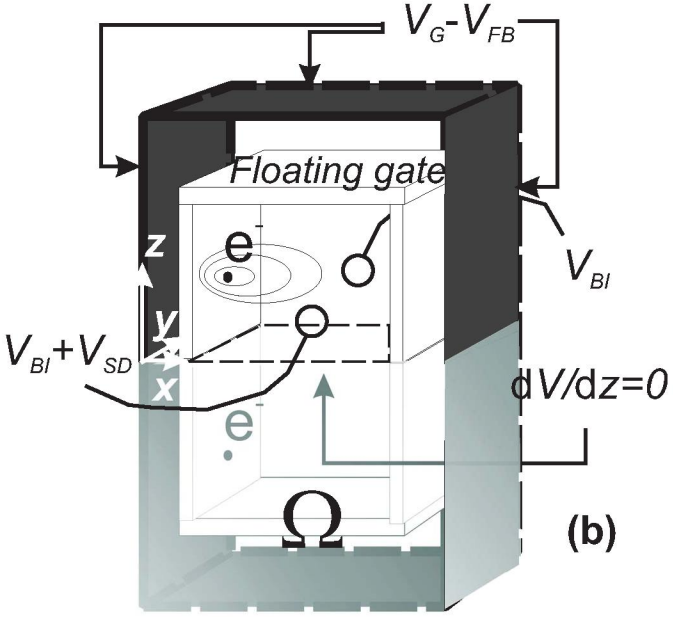


Fig. 2. **(a)** FinFLASH structure employed in 3D simulations. Only half a structure is represented and simulated because of symmetry considerations with respect to a longitudinal plane at the middle of the device. The gate stack is transparent to let appear the floating gate around the fin. **(b)** FinFLASH schematic employed for the analytical model to solve the electrostatics under weak inversion. Among the boundary conditions, it should be noted the Neumann condition ($dV/dz=0$) at the bottom side due to the presence of the thick BOX. Source and drain equivalent metallic plates are transparent to let appear the domain of analysis. The point charges are afterwards integrated to obtain the uniformly charged floating gate.

III. Numerical simulations and discussion

In order to validate our approach, we compared the results obtained by means of the analytical model with a large set of 3D TCAD simulations[5] while varying the features of the memory cell (i.e. dimensions of the fin, tunnel and top oxide thicknesses, amount of trapped charge, etc.). In Fig. 3, we show a comparison of the potential along y for a fresh and a charged cell. We see that we obtain a good agreement between the numerical and the analytical model especially capturing the minimum of the potential, which is the energy barrier peak that has to be overcome by electrons travelling towards the drain. However we note some mismatch approaching the source and drain junction. The potential around these regions is overestimated because the drain and source are represented by metallic plates (see Fig. 2b) which enforce Dirichlet boundary

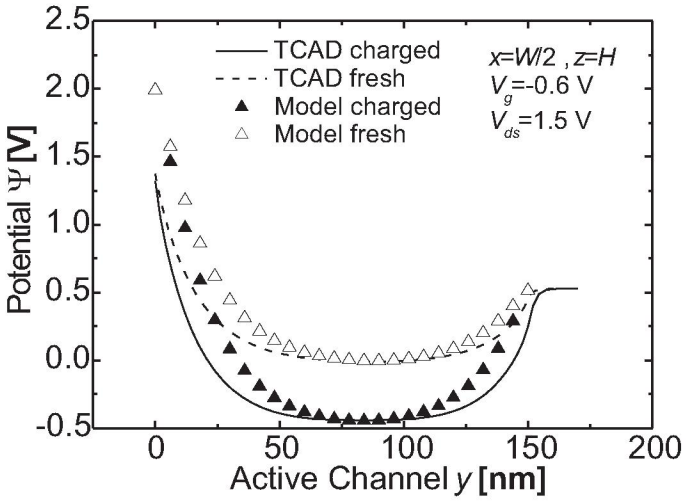


Fig. 3. Plot of the fin potential along a longitudinal cut for a fresh and charged device. A fine agreement between the TCAD and model results is apparent even for high drain-to-source voltage reading ($W = 40$ nm, $H = 30$ nm).

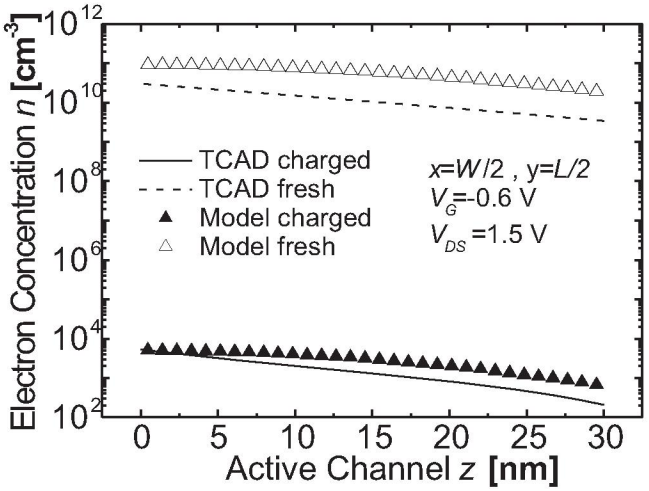


Fig. 4. Plot of the electron concentration along the fin height for a fresh and a charged device assuming $n = n_i \exp(q\Psi_{FFLASH}/KT)$, ($W = 40$ nm, $H = 30$ nm). The quasi-Fermi energy level is assumed null and this can be part of the source of error concerning the offset between the TCAD and the analytical results.

conditions not only along the extremes of the silicon fin, but also along the sides of the oxides up to the gate, where we should have preferably a Neumann boundary condition. This approximation had to be done in order to obtain an analytical solution to our problem, and the limits of validity will be discussed in section IV.

In Fig. 4 we show a comparison of the electron concentration along z. Indeed, the efficiency of our model in describing both the electrostatics, based on (3), and the transport in 3D structures, based on (4), clearly appears.

In Fig. 5 we compare the transfer characteristics I_{DS}-V_G for two different devices with $L = 150$ nm and $L = 70$ nm, and we note that the model fairly agrees with the numerical simulations even for the scaled device. We highlight the fact that we

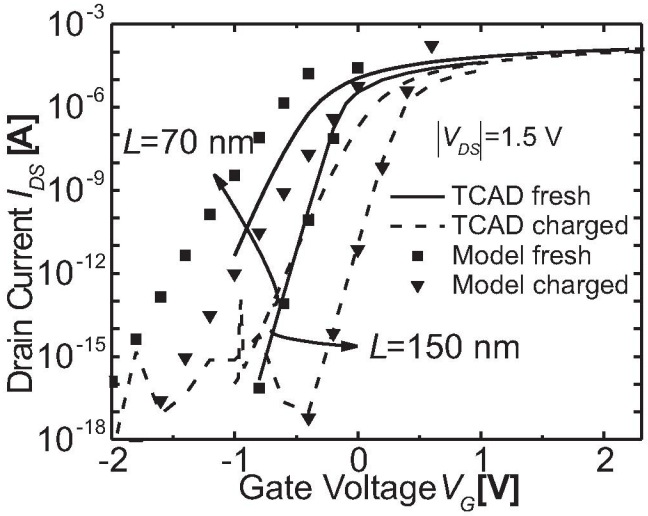


Fig. 5. Comparison between the transfer characteristics as obtained by TCAD and and by our model for a long and a short FinFLASH device ($W = 40$ nm, $H = 30$ nm). We see that for $L = 70$ nm the model looses accuracy in the V_{th} value, however still a fine ΔV_{th} and S factor are provided.

are in the worst reading condition, as we used $V_{DS} = 1.5$ V, concerning the reliability of the analytical model results.

In Fig.6 we extended the comparison of ΔV_{th} and S, the slope factor, to devices with different fin lengths and different aspect ratios, in order to analyze the typical features of a FinFLASH in the double-gate configuration (Fig. 6a) or in a trigate configuration (Fig. 6b). We notice a good agreement in the overall electrical behaviors down to $L = 50 - 100$ nm.

IV. Limits of validity

In this section we will analyze the limits of validity posed by the fin doping level and the Dirichlet boundary conditions at source/drain.

Our model is tailored for intrinsic fins, however due to the fact that the electrostatics in such structures is governed more by the geometry of the fin than by its doping level [6], we explored the validity of our approach for doped fins. In Fig. 7 we show the behavior of the programming window with respect to the fin doping level for small and large devices. Even if threshold voltages vary little with respect to fin doping (not shown in the figure), we see that the programming window remains quite constant, thus *our model can be used to well predict the threshold voltage shift even for doped fully-depleted devices.*

Concerning the Dirichlet boundary conditions at source and drain, we have to consider that in actual devices source and drain enforce a fixed voltage at the junction with the silicon fin and not over all the area up to the gate contact, as sketched in Fig. 2b. Moreover in the analytical model the oxide should be interpreted mathematically as an equivalent silicon region with suitable enlarged thickness, thus this problem put in serious challenge the model bases. This issue is even more serious for memory devices where the gate stack region is very thick with respect to fin sizes.

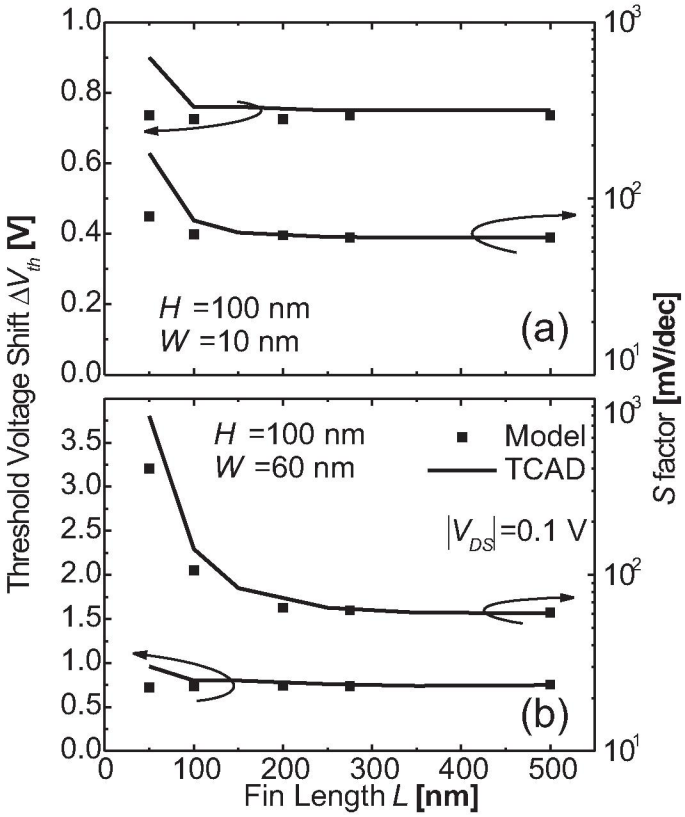


Fig. 6. Threshold voltage shift and slope factor for **(a)** a double-gate FinFLASH ($H \gg W$)and for **(b)** a trigate FinFLASH ($H \approx W$). We see that an excellent agreement is found down to $L = 100$ nm. Below this value the model suffers from excessive impact of drain and source built-in voltages on channel potential.

As evidenced in Ref. [3], we can highlight a natural decay length L_d of influence of the drain voltage on the fin electrostatics:

$$L_d = \frac{1}{\pi\sqrt{\frac{1}{W_{\text{eff}}} + \frac{1}{2H_{\text{eff}}}}} \tag{5}$$

This decay length has to be short (i.e. less than a half) with respect to the distance between the drain junction and the location of the potential minimum, in order to be sure that the error of the perfect Dirichlet boundary condition at source/drain does not propagate on the drain current calculation. Indeed the minimum of the potential govern the subthreshold current [7], and for reasonable value of the reading voltage V_{DS}, it remains around the center of the device length. Therefore we can establish as a safe value for the minimum features of the memory device with thick gate stack, what we obtain from the following criterion:

$$L_d \leq L/4, \tag{6}$$

which means, for instance, a device with features highlighted in Fig. 1 and W=40 nm, H=30 nm, L=90 nm.

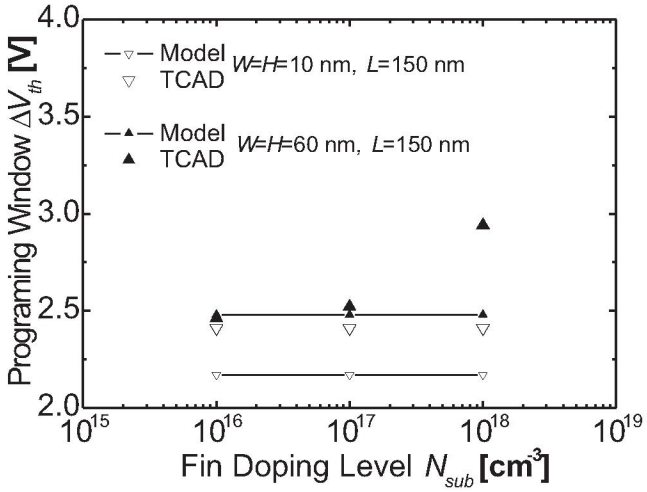


Fig. 7. Comparison between the programming windows obtained by the TCAD and by our model with different fin doping level. Both a large and a small fin device are represented, however the doping level of the fin does not impact much on the device performance at least up to the case of $W = L = 60$ nm and $N_{sub} = 10^{18}$ cm^{-3}, where we deal with a partially-depleted device.

The problem of perfect Dirichlet boundary condition at source drain is alleviated by the consideration of epitaxially raised source/drain junctions. As shown in Fig. 2a, the ideal device used for the comparison with TCAD simulation does not have raised source and drain junctions. However in actual devices the source and drain are normally raised in order to diminish access resistance, thus their geometry approaches the assumption of perfect Dirichlet boundary conditions made in our analytical model.

V. Conclusion

We have presented an original semi-analytical model that efficiently describes important electrical features of complex 3D SOI FinFLASH memory structures operating in *weak inversion*. The proposed model *does not need any fitting parameter* and shows a good agreement even for *doped fully-depleted devices*. Indeed, this model could be an effective tool to further investigate the electrical performance (i.e. multibit, multilevel, etc.) of different architectures of FinFLASH cell (i.e. SONOS, nanocrystal-based, etc.), without the need of implementing time consuming numerical simulation.

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