Impact of Wafer and Technology Selection on Liner Stress Mobility Enhancement

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Abstract – For the first time, the drain current enhancement effect of stressed contact liner applied to various wafer material is discussed in this paper. The enhancement is larger in SOI and SOQ device than in bulk MOSFET. Thinner SOI film causes more enhancement, but saturation current fluctuation sensitive to SOI thickness variation increases drastically. In case of SOS wafer, enhancement is reduced as SOS film thickness becomes thinner, because of large elastic modulus of sapphire.

I. Introduction

To keep Moore's law, mobility enhancement by uni-axial stress of liner SiN is suggested by many groups. Nfet mobility enhancement presented in 2005 conferences[1][2][3] is summarized in fig.1. In these papers, bulk, PD, FD-SOI are discussed individually, and impact of technology selection on mobility enhancement is not clear yet. Since most papers introduce several mobility enhancement approaches simultaneously, it is hard to separate liner effect from other effects.

In this paper, liner mobility enhancement of major wafers such as bulk, SOI, SOQ and SOS are compared and impact of wafer structure is clarified through simulation with stress effects. Furthermore, statistical problems arising from gate length and body thickness are discussed.

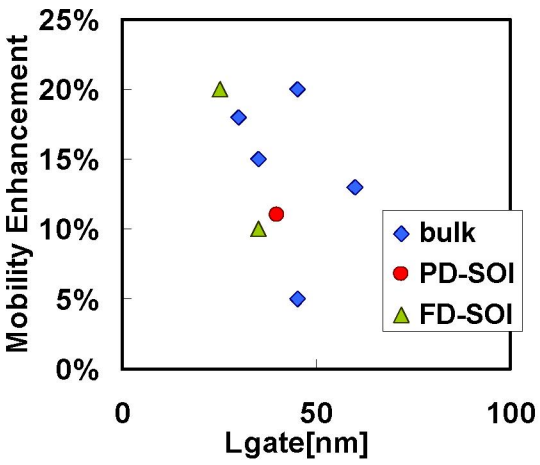


Fig 1. Mobility enhancement at various generation and various technology presented in 2005 conferences[1][2][3].

II. Simulation Method

An example of simulation structure is shown in fig.2. Simulations were performed using a three-dimensional process/device simulator ENEXSS[4]. Intrinsic stress of gate poly-Si, sidewall nitride, and liner nitride are considered as in ref.[5]. Stress arising from gate oxidation is also included.

Fig.3 shows an example of 2D stress distribution and its cross section along channel direction. In the following section, difference of stress at channel center calculated with and without liner stress are monitored, changing substrate material, thickness, and gate length.

III. Wafer Dependence

Channel stress as a function of top silicon thickness (Tsoi) is plotted for SOI, SOQ, SOS and bulk devices in fig.4. In case of SOI and SOQ wafers, stress effects are enhanced as Tsoi becomes thinner, but are reduced in case of SOS on the contrary.

SOI BOX thickness dependence is shown in fig.5. With thick BOX such as 500nm, SOI behaves identical to SOQ, and with thin BOX, identical to bulk wafer.

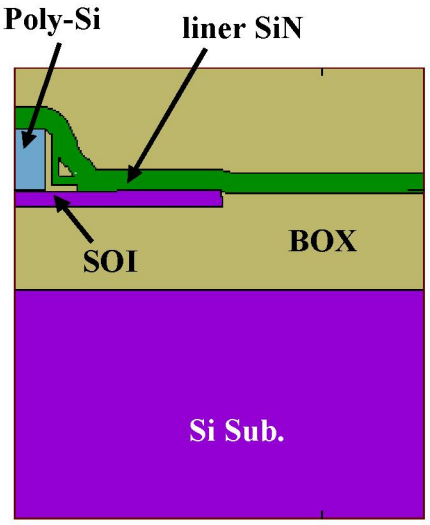
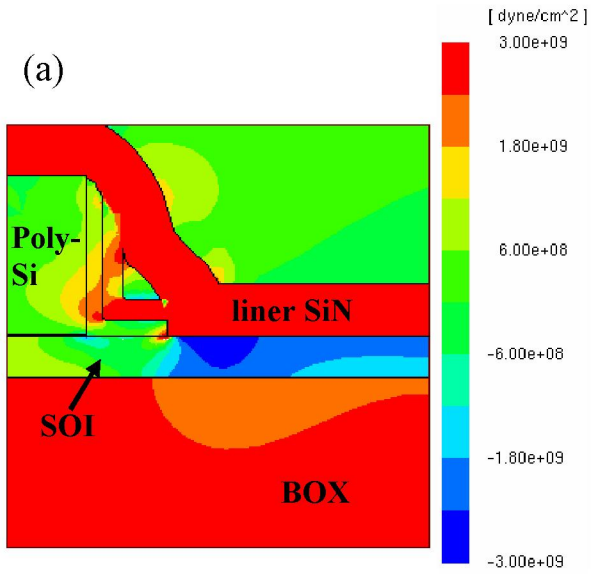


Fig 2. Simulated structure of SOI. The right half of the device is calculated. The boundary condition of the channel center is Neumann. Si Substrate is thick enough for the accuracy.



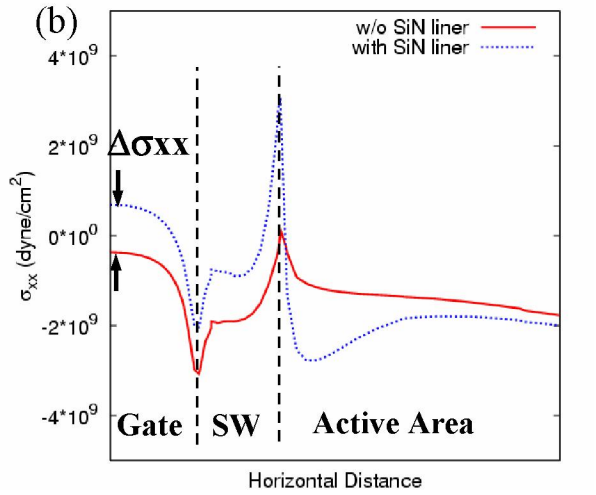


Fig 3. σxx distribution. (a) 2-dimensional profile of SOI. (b) Cross section along channel direction at silicon surface. Solid line is σxx profile without SiN liner, and dashed line is σxx profile with SiN liner. The difference of σxx at channel center is monitored as Δσxx.

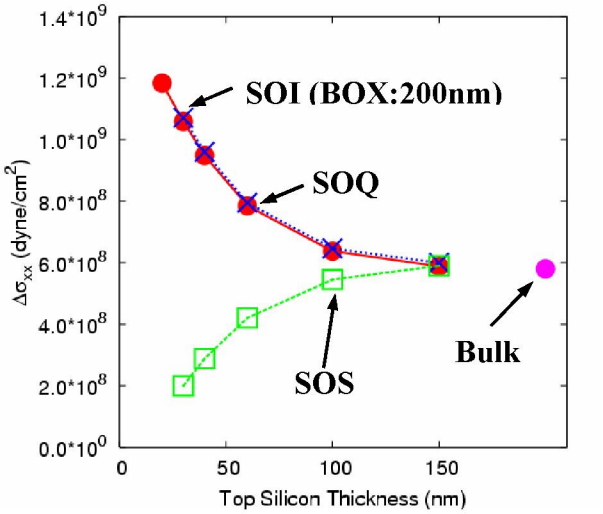


Fig 4. Impact of wafer material to Δσxx-Tsoi. SOI: solid line with filled circle. SOQ: dashed line with cross. SOS: dashed line with rectangle. BOX thickness of SOI is 200nm.

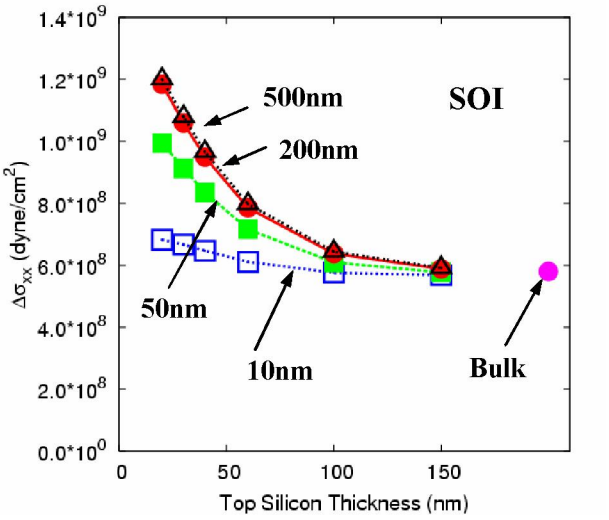


Fig 5. Impact of BOX thickness of SOI on Tsi effect to Δσxx. Stress effect enhancement along with Tsoi thickness reduction increases as BOX thickness becomes thicker.

To confirm that these results are caused mainly by mechanical characteristics of substrate materials, simple structure shown in fig.6 is simulated with only liner stress. In this simulation, left part not covered by SiN is assumed to be MOSFET channel. Horizontal distribution of Si surface stress is shown in fig.6(b) and (c).

Under the nitride layer, compressive stress is caused by nitride intrinsic stress, and this causes tensile stress in channel region not covered by nitride. In SOS case, strain caused in sapphire is small because of its large elastic modulus. As a result, tensile stress in channel region becomes smaller. Hence this effect enhances by thinner silicon thickness, mobility enhancement by stress liner diminishes in scaled-down SOS devices.

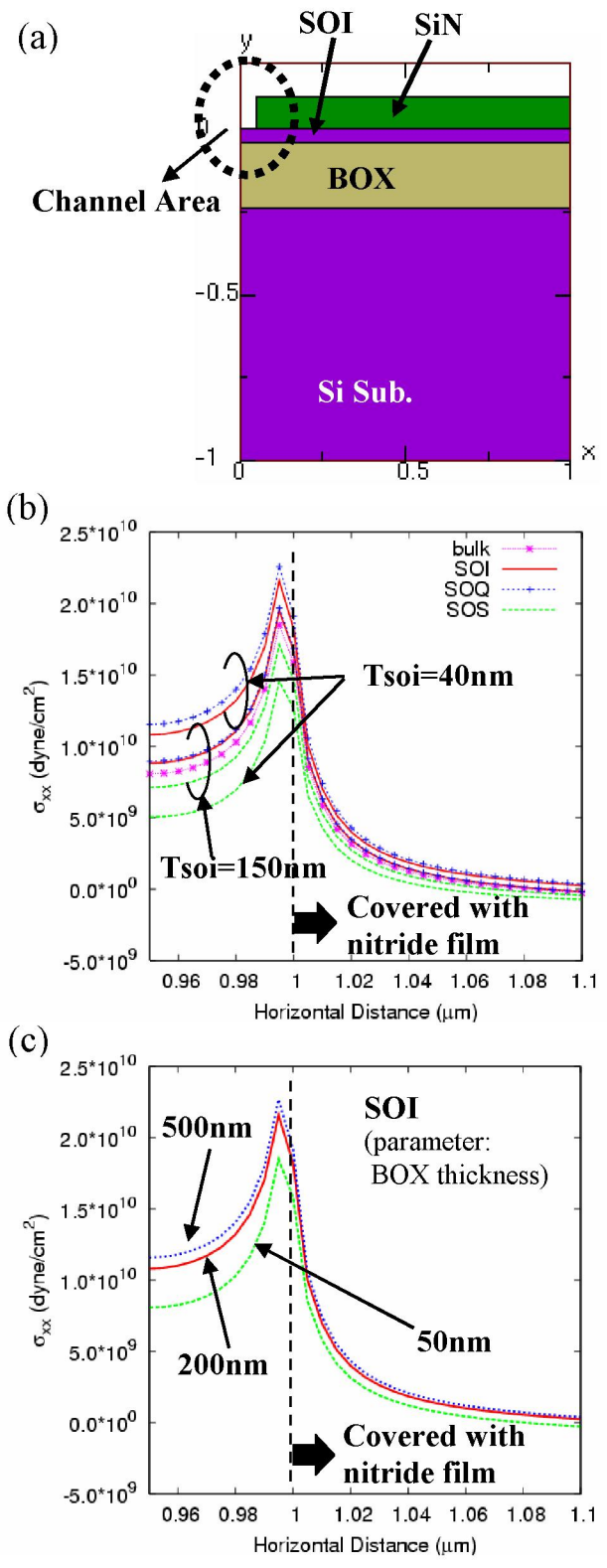


Fig 6. Stress simulation with simple structure to confirm the differences of the dependence of Tsi are caused mainly by mechanical characteristics of substrate materials (a). Cross section along channel direction at silicon surface of various wafer materials. (b) and BOX thickness of SOI. Left part not covered by SiN is assumed to be MOSFET channel area.

IV. Gate Length Dependence

To confirm scaling effects, Tsoi dependence of different gate lengths is plotted in fig.7. Because liner effects are almost similar both for 0.15um and 0.10um, gate length and body thickness has small interaction for mobility enhancement. When gate length is scaled down, SOQ takes advantage more than SOI. This means that reducing BOX thickness is not desirable for SOI scaling from the stress liner point of view.

Tsoi dependence of Drain current increase is almost same as that of σxx component of stress. SOQ and SOI have more advantage than bulk and SOS.

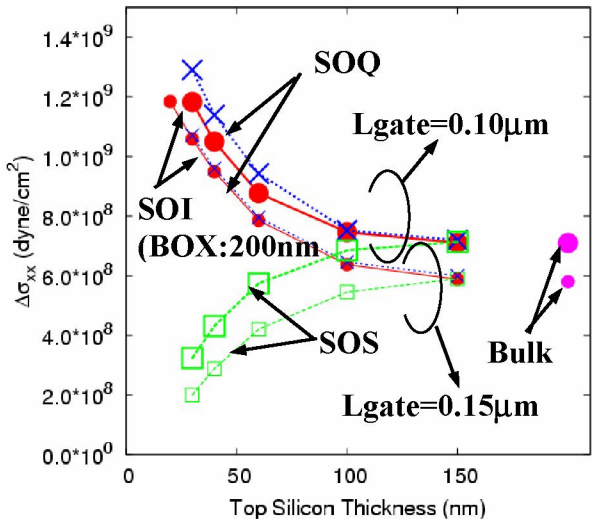


Fig 7. Impact of gate length on Tsi effect to Δσxx. SOI: solid line with filled circle. SOQ: dashed line with cross. SOS: dashed line with rectangle.

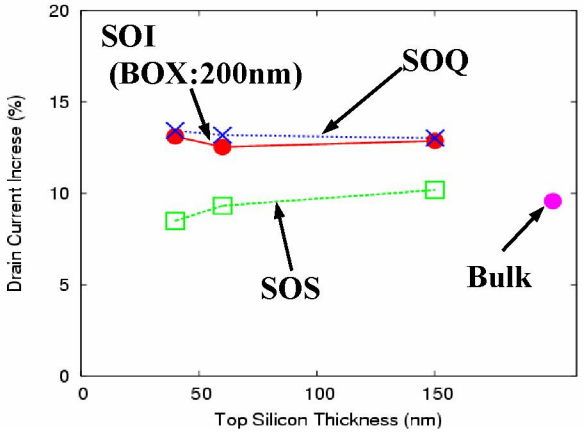


Fig 8. Drain current increase vs. Tsoi. The trends of increase are the same as Δσxx, but the enhancements are not in proportion to Δσxx because of the influence of the original stress without liner film.

V. Conclusion

Wafer structure dependence of stress liner effects are studied by simulation. When top silicon layer is scaling down, SOQ takes more advantage compared to SOI and bulk devices. In case of SOI, stress effect becomes identical to SOQ with thick BOX, and identical to bulk with thin BOX. Scaled-down SOS takes less advantage of stress liner. Gate length has small interaction on Tsoi dependence of stress effects.

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