Novel Mechanism of Neutron-Induced Multi-Cell Error in CMOS Devices Tracked Down from 3D Device Simulation

H. Yamaguchi, E. Ibe and Y. Yahagi
Production Engineering Research Laboratory
Hitachi Ltd.
Yokohama, Japan
hironaru.yamaguchi.ha@hitachi.com

S. Yamamoto, T. Akioka and H. Kameyama

Renesas Technology Co. Ltd.
Itami, Japan

Abstract— **In recent CMOS devices, multi-cell error induced by cosmic neutron, in which memory state change extends over multiple memory cells, is becoming serious. However, its mechanism has not been clarified yet because conventional analysis by device simulation has not included multiple memory cells domain. Our novel method is to create the device model including multiple memory cells and perform 3D simulation. Analyzing current transients and current distribution, we identified multi-cell error as a chain reaction as follows: (1) parasitic bipolar in "target" CMOSFET is turned on by secondary ions produced by ion strike, (2) this parasitic bipolar action causes well voltage shift, (3) lastly parasitic bipolar in adjacent CMOSFETs are turned on and thus error propagates.**

Keywords-CMOS; neutron; single event error; device simulation

I. INTRODUCTION

Along with recent scaling of CMOS devices down to sub-100nm, neutron induced soft and hard errors are becoming major concern in reliability issues. Especially, multi-cell upsets (MCUs), in which multiple memory cells show abnormal behavior by neutron strike at single memory cell, have been reported in these days. Other error modes called "power-cycle error"[1], or "firm-error"[2], etc. would be identical with MCU in their phenomenon. Fig. 1 shows some example of error bit map of MCUs. WL and BL show the directions of word-line and bit-line. Each square shows one memory cell, and black circles show memory cells in which data upsets occurred. This error is serious because it cannot essentially be corrected by usual Error Correction Code (ECC). Though some of them are supposed to be due to "known" mechanism like latch-up or "microlatch", their detailed phenomena and mechanisms have not been identified yet [3-5].

Summing up experimental data of MCU, they have the features as follows:

(1) more than 10 bits fails take place in the same p-well,

(2) errors can be recovered by some re-writing, so that they are not classified as latch-up [6].

Corresponding to these features, we applied 3D device simulation to multi-cell CMOSFETs structure models. A novel error mechanism, multi-coupled bipolar interaction (MCBI) is proposed for the MCU mode.

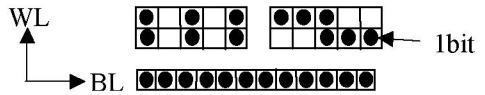


Figure 1. Error bit map of MCUs

II. METHOD

We use Davinci™ to analyze transient responses after the ion strike, applying SRH and Auger recombination models, Lombardi's surface mobility model, and impact ionization model.

In conventional method, MCU is analyzed by mixed-mode simulation in which single CMOSFET domain is modeled and coupled into circuit model substituting adjacent CMOSFETs domain [7]. But actually, as wells are continuous along bit lines and contain multiple CMOSFETs, mixed-mode simulation cannot reproduce the "true" device action. Instead, we constructed the device model including multi CMOSFETs area. Though this model needs nearly 100k nodes, the performance of recent device simulator satisfies it.

In the following sections, firstly the model for single NMOS structure is treated, and secondly the model containing 4 CMOSFETs combined structure is treated.

In both models Mg^+ ion is chosen as a candidate secondary ion from spallation reaction of silicon nuclei with terrestrial neutron.

III. RESULTS AND DISCUSSIONS

A. *Single NMOS configuration*

Fig. 2 shows the configuration of single NMOS with two ion tracks. Track A is perpendicular from the top to bottom through the NMOS node. Track B is parallel with the source-drain direction in the well. In other word, track A passes through the p-n junction between the p-well and deep-n-well, and track B does not pass through the referred p-n junction.

Fig. 3 shows the current through node for 10MeV Mg^{+} ion passing (initial charge deposition density is 123fC/mm) along track A and B, respectively. For track A, two peaks appear in the current transient at around 10ps and 1ns. In contrast, for track B, only 10ps peak appears.

Fig. 4. (a) and (b) show carrier flow for normal MOS "on" state as no ion struck, and Fig. 4(c) and (d) show carrier flow as ion passed along track A. In Fig. 4(a), electrons flow mainly near surface and in Fig. 4(c) electrons flow through p-well. Therefore, the carrier flow in Fig. 4(c) is not caused by normal MOS action but by parasitic bipolar action. Also there is vertical flow of holes from drain as shown in Fig. 4(d), which shows vertical parasitic bipolar action.

From these results, it is considered that the 1ns peak in Fig. 3 is caused by parasitic bipolar action in the p-n junction between the n+ node and the deep-n-well, though the 10ps peak is caused by parasitic bipolar action in the p-n junction between the source and drain. Bipolar gain, that is, the ratio of collected charge to deposited charge, is estimated at about 4 [8].

Fig. 5 shows the waveform of drain current I_D, source current I_S, and substrate current I_{Sub} for the two ion tracks. I_D+I_S and $I_D+I_S+I_{Sub}$ are also shown. Positive value of vertical axis shows current inflow and negative value shows outflow.

In the case of Track A, I_D+I_S is negative and I_{Sub} is positive, which shows current flow from substrate to source and drain through deep-n-well. This current direction agrees with that shown in Fig. 4(d). In addition, as $I_D+I_S+I_{Sub}$ is positive, the surplus current is considered to flow out of p-well.

In the case of Track B, I_D+I_S is positive and I_{Sub} is nearly 0, which shows almost all current flows to p-well.

Fig. 6 depicts the equivalent circuit illustrating the phenomenon above. In the case of Track A, as holes flow to ground through p-well, well potential rises by well resistance. By this, lateral and vertical parasitic NPN transistors turn on, and large current flows in device. In the case of Track B, as holes flow to p-well, only lateral parasitic NPN transistor turns on.

As shown in Fig. 5(a), the peak of I_{Sub} is delayed from the peak of I_D. It is considered that initially lateral NPN transistor corresponding to I_D peak is turned on, and next vertical NPN transistor corresponding to I_{Sub} peak is turned on.

These actions agree well with the theory of "snapback" by Beitman [9].

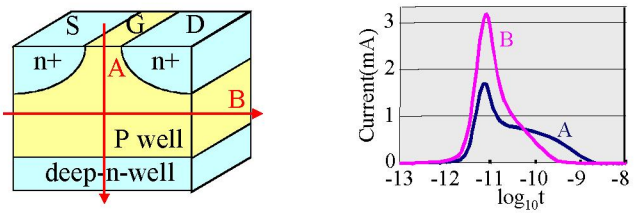


Figure 2. Single NMOS configuration *(left)*

Figure 3. Waveform of the current through node *(right)*

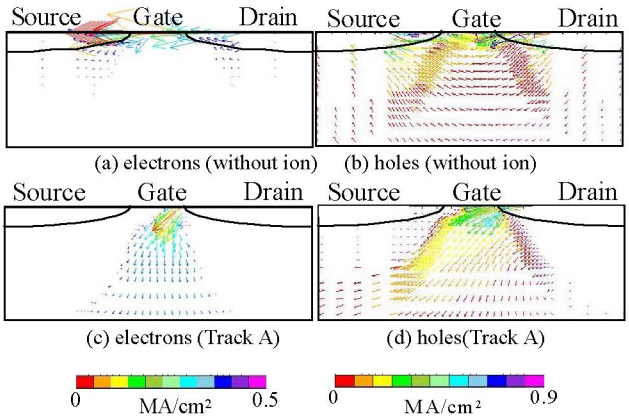


Figure 4. Carrier flow in single NMOS

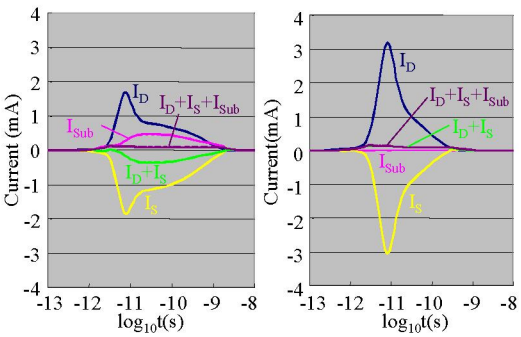


Figure 5. Waveform of the current through each electrode

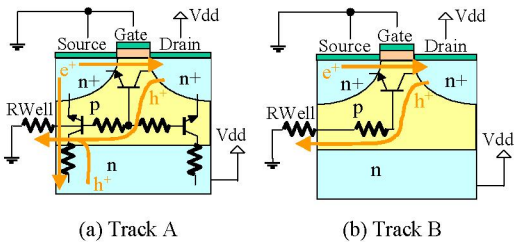


Figure 6. Scheme of snapback

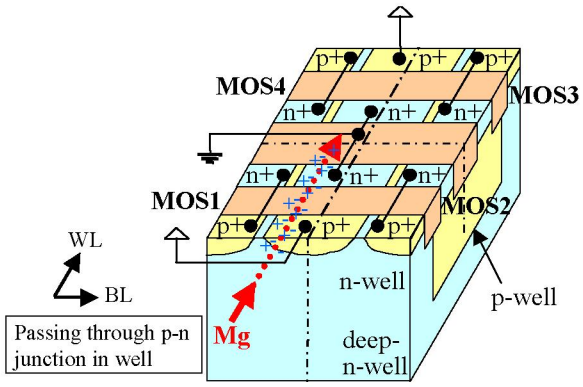


Figure 7. Four CMOSFETs configuration

B. Four CMOSFETs configuration

Fig. 7 shows the configuration containing four CMOSFET inverters MOS1 to MOS4 where a full p-well structure is placed in the center. P-well and n-well are connected to GND and Vdd respectively. Initial state is settled as each NMOS is "Off" and each PMOS is "On".

The Mg^+ ion strikes at n-well side penetrating p-n junction of MOS1 in Fig. 7 below drain node, by an analogy with the charge amplification for ion track passing through p-n junction in well as shown for single NMOS configuration.

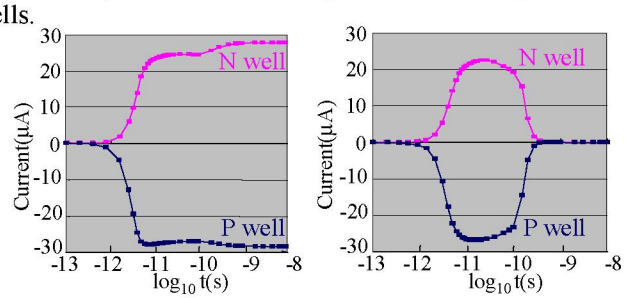
Fig. 8(a) and (b) show simulation results for the currents through n+ nodes into MOS1 to MOS4. Each figure corresponds to different ion energy. Initial charge production density is equivalent to 45fC/mm and 30fC/mm in Si, respectively.

In Fig. 8(a), initially the current into MOS1 jump at the onset of Mg^+ ion, which is considered to be equivalent to the action of I_D in Fig. 6. Then, the current into MOS2 to MOS4, which are apart from the penetration point, increases gradually to the same level as that into MOS1, eventually the current of a few milliamperes continue to flow and cause upset in all 4 bits. In contrast, as shown in Fig. 8(b), as ion energy is lower the node current in MOS1 recovers to the level of normal gate leak current, and the node currents in MOS2 to MOS4 do not increase.

Fig. 9(a) and (b) show the current through p-well from GND and through n-well from Vdd on the same condition as in Fig. 8(a) and (b). For the condition of Fig. 8(a), currents continue to flow, besides for the condition of Fig. 8(b), currents drop to normal state. This tendency agrees that of the current through n+ node into MOS1 shown in Fig. 9(a). From this, we can estimate the device action as follows — as the current into MOS1 through n+ node increases, the currents through n-well and p-well increase and eventually the currents into MOS2 to MOS4 also increase.

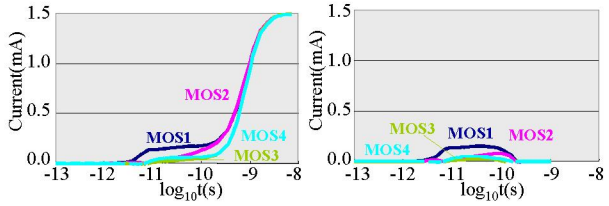
Fig. 10(a) and (b) show the carrier flows at 1ns as ion energy is 1MeV. In Fig. 10(a), electrons flow horizontally in NMOS, which is the evidence of the snapback as well as single NMOS configuration. In Fig. 10(b), there is vertical hole flow in PMOS.

From the result shown above, we depict the equivalent circuit of MCBI as shown in Fig. 11. In comparison with Fig. 5, parasitic PNP(Tr3) is formed between PMOS node and p-well through n-well. It is considered that the snapback of NMOS causes the temporal variation of n-well potential and turns on the PNP transistor. Though Fig. 11 shows single CMOSFET region, the same circuits can be applied for other CMOSFETs region because wells are common to each CMOSFET, and then error expands over multiple memory cells.



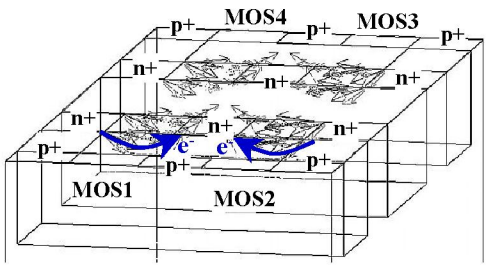
(a) Ion energy: 1MeV (b) Ion energy: 0.6MeV

Figure 8. Waveform of current through n+ node into each CMOSFET

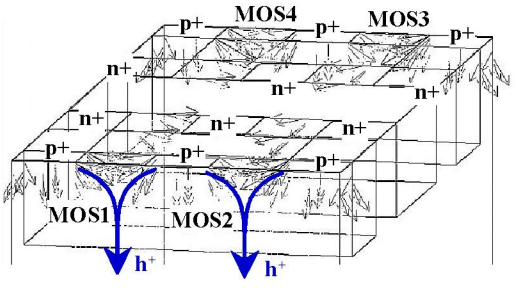


(a) Ion energy: 1MeV (b) Ion energy: 0.6MeV

Figure 9. Waveform of current through n-well and p-well



(a) Electrons



(b) holes

Figure 10. Carrier flow in four CMOSFETs configuration

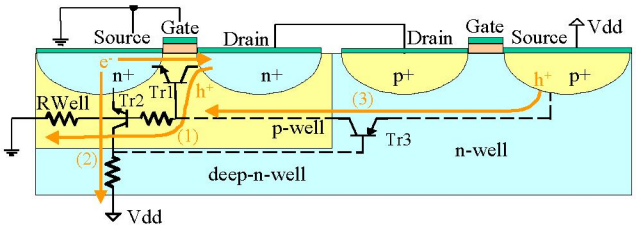


Figure 11. Scheme of MCBI

C. *Carrier flow in single NMOS* Dependence of collected charge on ion track position

Fig. 12 shows the charge collected to Node1 at 1ns for various ion energies. From Fig. 12, the threshold energy is estimated at about 650keV, where the charge deposition density is 32fC/μm.

Fig. 13 show the charge collected to the n+ node in MOS1 at 1ns for various depths of ion track where ion energy is fixed at 1MeV. It is found that collected charge depends significantly on the depth of ion track. In addition, current continues to flow after 1ns peak as ion passes through the p-n junctions between n-well and p-well.

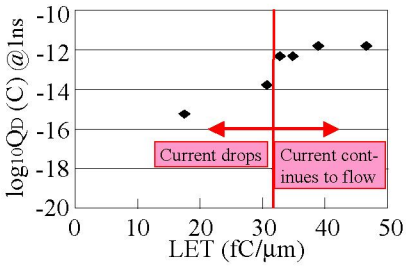


Figure 12. Collected charge at various ion energy

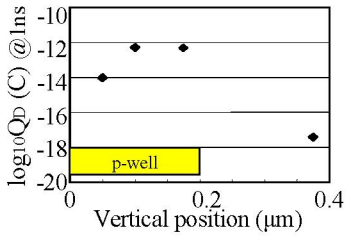


Figure 13. Collected charge at various depths of ion track

IV. Conclusions

The behavior of CMOSFET due to neutron irradiation is ana-lyzed by using 3D device simulation with single NMOS and 4 CMOSFETs configurations. In a single NMOS model, current peak due to snapback appear at the onset of ion, but does not show any stable current as shown in Fig. 5. As combining 4 CMOSFETs, it is found that snapback of single NMOS causes the variation of n-well potential and lastly causes parasitic bipolar action in adjacent CMOSFETs which keeps the increased node currents. In conclusion, we have identified the mechanism of multi-cell error as MCBI triggered by snapback of single NMOS, for the first time. This result could not gotten by mixed-mode simulation of single CMOSFET domain coupled with circuit model substituting adjacent CMOSFETs domain, but by constructing a device model containing multiple CMOSFETs domain.

V. Appendix

For reference the difference of MCBI from other errors is summarized below. Here, "power cycle" means that the DUT power is turned off and then turned on.

TABLE1. Difference between error modes

Mode	Structure	Range	I_{dd} current	How to recover
Snapback	NMOS or PMOS	<=2-10 bits on BL <=2 bits on WL	Low and stop automatically	Re-write (or re-read)
Latch-up	CMOS	>>2 bits on both WL and BL	High and continue to flow	Power cycle
MCBI	CMOS	>>2 bits on both WL and BL	Low and continue to flow depending on MCU multiplicity	Re-write

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