Monte Carlo study of remote Coulomb and remote surface roughness scattering in nanoscale Ge PMOSFETs with ultrathin high-κ dielectrics

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Abstract— **In this work we perform full-band Monte Carlo simulations of nanoscale Ge bulk PMOSFETs with ultrathin (< 2nm) effective oxide thickness high-κ dielectrics and investigate the importance of remote Coulomb and remote surface roughness scattering in these devices. For a gate overdrive, (V_g - V_t), of 1.0 V, remote scattering mechanisms seem to decrease the saturation current by as much as 15% in these devices.**

Keywords-Germanium, remote Coulomb, remote surface roughness, Monte Carlo

I. Introduction

As the channel length in CMOS (Complementary Metal-Oxide Semiconductor) devices continues to be scaled down, so must the thickness of the dielectric in order to control short channel effects. However, when the thicknesses of conventional dielectrics like SiO_2, used in Si MOSFETs are reduced below 2 nm, the gate leakage current (due to direct tunneling) becomes prohibitively high for low standby power applications. This impediment to gate oxide scaling has led to the interest in high-κ dielectrics as possible replacements for conventional (low-κ) dielectrics like SiO_2. However, the integration of high-κ dielectrics on Si is challenging, in particular, due to degradation of carrier mobility in the channel. Hence new materials, like Ge, with higher mobilities of electrons and holes than in Si are being considered. Nevertheless, the mobility degrading factors of high-κ are present for Ge channels as well and hence, to obtain the greatest benefit from device scaling it is necessary to identify these mobility degrading factors and reduce their effect on device performance to the maximum possible extent. Recently, several experimental and theoretical studies have been performed to understand the nature and strength of the mobility degrading mechanisms in thin dielectrics on Si and Ge N- and PMOSFETs [1-5]. However, to the best of our knowledge, there has been no theoretical Monte Carlo study on the performance degradation due, simultaneously, to remote Coulomb and remote surface roughness scattering in ultra-thin high-κ-on-Ge PMOSFETs. In this work we perform a full band Monte Carlo study on the effects of remote Coulomb and remote surface roughness scattering on the performance of nanoscale Ge PMOSFETs.

II. Monte Carlo Simulator

We modified our full band Monte Carlo simulation tool "Monte Carlo University of Texas" (MCUT) to study Ge channel MOSFETs with transport in the presence of phonon, ionized impurity, normal and remote surface roughness scattering, remote coulomb scattering and impact ionization. Quantum confinement in the inversion layer was taken into account in the form of a modified potential. The bandstructure and phonon scattering rates for Ge holes were calculated by the tight-binding method and from Fermi's Golden rule, respectively. The parameters in the various scattering rates were tuned to match experimental data as shown in Figs. 1 and 2.

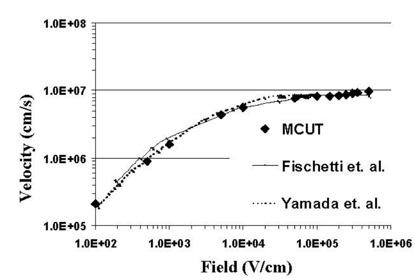

Figure 1. Velocity versus longitudinal field for unstrained Ge holes.

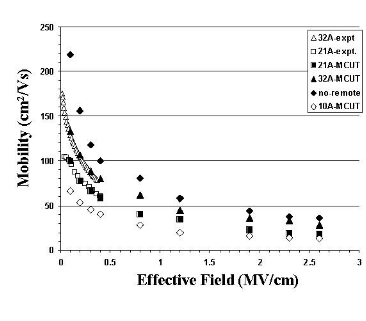

Figure 2. Mobility versus transverse effective field curves (for various oxide thicknesses) for unstrained Ge holes.

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III. DEVICE SIMULATION

The experimental mobilities were extracted from a self isolated ring Ge PMOSFET using (100) n-type Ge wafers of resistivity 0.1 ohm-cm and a self aligned MOSFET process with Tungsten as the gate material. Ultrathin HfO_2 of varying thicknesses (t_{eq} ranging from 2.1 to 3.2 nm) were deposited using UHV reactive atomic beam deposition and the effective mobility was calculated using long channel MOSFETs (100 μm) at low lateral fields using the gradual channel approximation and the mobility versus effective field data are shown in Fig. 2 for oxide thicknesses of 2.1 and 3.2 nm. Device simulations were performed with a bulk MOS structure with 50 nm gate length and 2 nm gate oxide (HfO_2) thickness. A "well-tempered" bulk n-MOSFET doping profile [6] was used and the dopant type was switched to study PMOSFETs.

IV. DISCUSSION

Fig. 3 shows the I_D vs. V_D curves for the Ge PMOSFET with and without remote scattering at V_G - V_t = -1.0 V and –0.5 V. The decrease in the saturation current due to remote scattering at V_G - V_t = -1.0 V is 15.3 % and at V_G - V_t = -0.5 V is 16.7 %. As discussed in [7], the mobility at the peak of the source channel barrier still plays an important role in determining the saturation currents of nanoscale MOSFETs. Therefore, we obtained the values of the effective field and mobility at the peak of the source channel barrier as shown in Table 1.

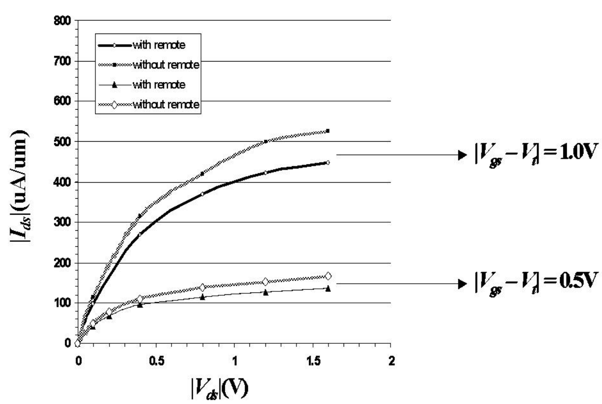

Figure 3. Comparison of drain current versus drain voltage with and without remote scattering for various gate overdrive voltages.

TABLE 1. Effective field (V/cm) and mobility (cm^2/Vs) at the peak of the source channel barrier in the notation effective field (mobility) with and without remote scattering and for various gate overdrive voltages.

Device/ scattering	50 nm single gate PMOSFET	
	$V_g - V_t$ = –1.0 V	$V_g - V_t$ = –0.5 V
With remote scattering	1.22×10^6 (32.6)	8.27×10^5 (40.2)
Without remote scattering	1.24×10^6 (59.3)	8.38×10^5 (80.23)

The values thus obtained for the mobility qualitatively correspond well with the observed values of the saturation current. For example at V_G - V_t = -1.0 V, the effective fields at the peak of the source channel barrier are 1.22 MV/cm with remote scattering and 1.24 MV/cm without remote scattering. However, the corresponding mobilities, obtained from Fig. 2 are 32.6 cm^2/Vs and 59.3 cm^2/Vs, respectively. This corresponds to a decrease of 45.0% in mobility and of 15.3% in saturation current (as shown in Fig. 3) due to remote scattering. Similar trends between mobility at the peak of the source-channel barrier and saturation current are obtained at other gate voltages for the single gate MOSFET.

Fig. 4 shows the dependence of the mobility (in the presence of remote scattering) as a function of oxide thickness at different values of the effective field.

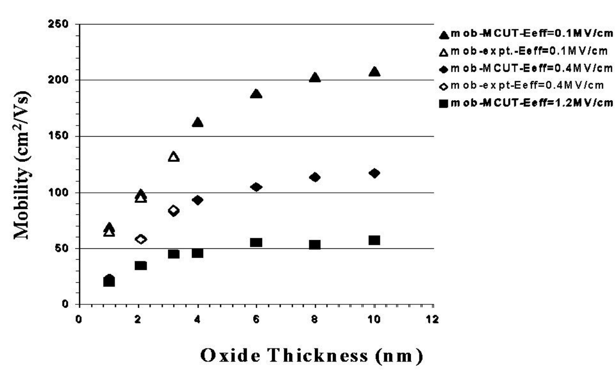

Figure 4. Mobility as a function of oxide thickness for various values of effective fields.

It is evident that, for the effective fields of ~1.2 MV/cm found in the on state in our simulations these scattering processes will remain important for $t_{eq} < \sim 3$ nm that will be encountered in such devices. This result is similar to that obtained for Si [4,8].

V. CONCLUSION

In this work we performed a full band Monte Carlo study of the effect of remote Coulomb and remote surface roughness scattering on the performance of nanoscale bulk Ge PMOSFETs. We considered transport including phonon, ionized impurity, surface roughness scattering and impact ionization, as well as remote Coulomb and remote surface roughness scattering. Carrier redistribution in real space and among energy valleys (k-space) due to quantum confinement within the inversion layer was addressed via position and valley/band-dependent quantum-corrected potentials. We showed that the experimentally obtained data on the dependence of mobility on the thickness of the high-κ dielectric can be explained by scattering due to remote surface roughness at the gate-dielectric interface and remote Coulomb scattering due to fixed charges in the dielectric. We also investigated the performance degradation of Ge PMOSFETs due to these scattering mechanisms. The decrease in drive current at $V_g - V_t = -1.0$V and $V_d = 1.2$ V is about 15 % for the single gate structure studied. Our results show that, in the regime of typical gate and drain voltages used in realistic MOSFETs, remote scattering plays an important role for oxide thicknesses below 2 nm but can be neglected above 4 nm. Consequently, we still envisage significant improvement in device performance by paying attention to processing issues such as the reduction of interface fixed and trapped charges.

REFERENCES

[1] J. Li and T.P. Ma, “Scattering of silicon inversion layer electrons by metal/oxide interface roughness, ”Journal of Applied Physics, Vol. 62, No. 10, 1987, pp. 4212-4215.

[2] S. Saito et.al., “Effects of remote-surface roughness scattering on carrier mobility in field-effect-transistors with ultrathin gate dielectrics,” Applied Physics Letters, Vol. 84, No.8, 2004, pp. 1395-1397.

[3] F. Gamiz and J. B. Roldan, “Scattering of electrons in silicon inversion layers by remote surface roughness,” Journal of Applied Physics, Vol. 94, No. 1, 2003, pp. 392-399.

[4] F. Gamiz, A. Godoy, F. Jimenez-Molinos, P. Cartujo-Cassinello, “Remote surface roughness scattering in ultrathin-oxide MOSFETs”, in ESSDERC 2003, Proceedings of the 33rd European Solid-State Device Research - ESSDERC ’03 (IEEE Cat. No. 03EX704), Piscataway, NJ, USA, IEEE, 2003, pp. 403-406.

[5] G.S. Lujan, S. Kubicek, S. De Gendt, M. Heyns, W. Magnus and K. De Meyer, “Mobility degradation in high k transistors, the role of the charge scattering”, in ESSDERC 2003, Proceedings of the 33rd European Solid-State Device Research -ESSDERC '03 (IEEE Cat. No. 03EX704), Piscataway, NJ, USA, IEEE, 2003, pp. 399-402.

[6] MIT well tempered 50 nm n-MOSFET device structure, http://www-mtl.mit.edu/Well/.

[7] M. Lundstrom, “Elementary Scattering Theory of the Silicon MOSFET,” IEEE Electron Device Letters, Vol. 18, No 7, July 1997.

[8] F. Gamiz, J. B. Roldan, J. E. Carceller, P. Cartujo,” Monte Carlo simulation of remote-Coulomb-scattering- limited mobility in metal - oxide – semiconductor transistors”, Applied Physics Letters, Vol. 82, No. 19, 12 May 2003, pp. 3251-3253.

