# A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors

Jie Deng and H.-S. Philip Wong

Center for Integrated Systems and Dept. of Electrical Engineering
Stanford, CA 94305
{jdeng, hspwong}@stanford.edu

***Abstract*—This paper presents a circuit-compatible compact model for short channel length (5nm~100nm), quasi-ballistic single wall carbon nanotube field-effect transistors (CNFETs). For the first time, a universal circuit-compatible CNFET model was implemented with HSPICE. This model includes practical device non-idealities, e.g. the quantum confinement effects in both circumferential and channel length direction, the acoustical/optical phonon scattering in channel region and the resistive source/drain, as well as the real time dynamic response with a transcapacitance array. This model is valid for CNFET for a wide diameter range and various chiralities as long as the carbon nanotube (CNT) is semiconducting.**

***Keywords: CNFET, carbon nanotube, SPICE, modeling, compact model, circuit-compatible, CMOS***

## I. INTRODUCTION

As one of the promising new devices, carbon nanotube transistor (CNFET) avoid most of the fundamental limitations for silicon devices. Efforts have been made in recent years on modeling CNT related devices, e.g. CNFET [1, 2], CNT interconnects [3, 4], to evaluate the potential performance at the device level. Very promising single device DC performance over silicon device has been demonstrated either by modeling or experimental data. However, the dynamic performance of a complete circuit system, consisting of more than one CNFETs and interconnects, differs from that of a single device. All the reported models [5, 6] to date used a single lumped gate capacitance and ideal ballistic model to evaluate the dynamic performance which results in an inaccurate prediction. To evaluate CNFET circuit performance with improved accuracy, a CNFET device model with a more complete circuit-compatible structure and including the typical device non-idealities is necessary.

## II. DEVICE MODELING

In the past few years, various CNFET structures have been demonstrated. Considering both the fabrication feasibility and device performance, enhancement mode CNFETs, with intrinsic transport channel region and doped source/drain (Fig.1a), are preferred for complementary logic design and thus are chosen to be modeled in this paper. A planar gate structure which is closer to the reality than the coaxial gate structure is used in the modeling.

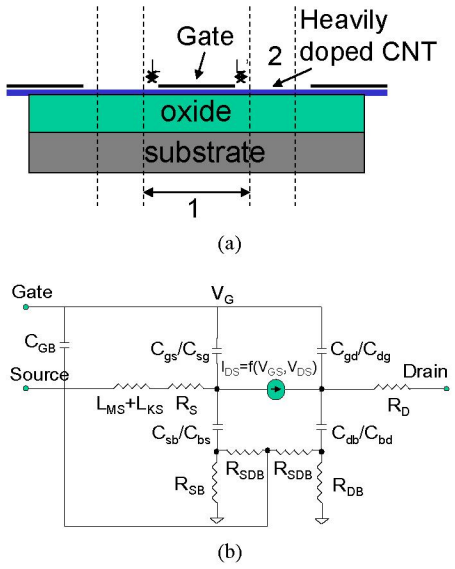



Figure 1. (a) CNFET device layout illustration. (b) Compact circuit model.

A complete compact circuit model is illustrated by fig.1b, where $C_{GB}$ is the coupling capacitance between gate and substrate, and $C_{xy}/C_{yx}$ are the trans-capacitance pairs. $L_{MS}$ is the magnetic inductance which is three orders smaller than $L_{KS}$, the quantum inductance of CNT. The quantum inductance $L_{KS}$ only kicks in with frequency higher than 5THz which is far beyond the interested frequency range for typical digital applications, thus the effects of inductance can be safely ignored in the modeling.

The device model is represented by CNT surface chemical potential, instead of the electrostatic potential. There are four Fermi levels (both input and output Fermi levels for source/drain) for each device due to the quantum contact resistance (Fig.2a). A 6-port device model, instead of the conventional 4-port FET model, is generated internally (Fig.2b). The two benefits are 1) the quantum contact resistances are automatically taken into account so that no artificial external quantum resistance needs to be added, 2)

multiple CNFETs with different quantum resistance can be easily cascaded while maintaining the superposition law required for a linear system.

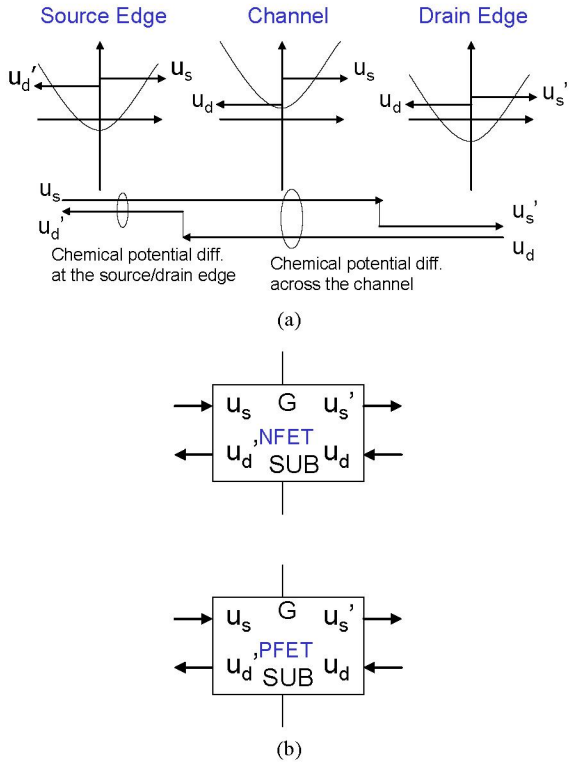



Figure 2. (a) The Fermi level profile for ballistic-transport CNFET (region 1 in Fig.1) (b) Internal 6-ports device model.

For short channel device, with the Born-von Karman boundary condition, the drain current contributed by each sub-states can be expressed as (2 is due to electron spin degeneracy)

$$J_{m,l}(V,\Delta\phi_B) = 2env_F = \frac{2e}{h} f_{FD}(E_{m,l} + eV - \Delta\phi_B)\frac{\sqrt{3}a\pi V_\pi}{L}\frac{k_l}{\sqrt{k_m^2 + k_l^2}}$$

Where L is the channel length, $f_{FD}$ is the Fermi-Dirac distribution function, and $E_{m,l}$ is the carrier energy of the substate (m, l), the quantum numbers for the transverse and longitudinal direction, respectively. V is the source / drain chemical potential. $\Delta\Phi_B$ is the channel surface potential lowering due to gate/drain bias. The source input Fermi level was chosen as the reference point. $V_\pi$ (~3.033eV) is the carbon $\pi$-$\pi$ bond energy with tight bonding model, and 'a' is the carbon atom distance.

Thus the total current contributed by all substates is given by

$$J(V_D, V_G) = \sum_{k_m^\perp}\sum_{k_l^\parallel}[T_{LR}J_{m,l}(0,\Delta\phi_B) - T_{RL}J_{m,l}(V_D,\Delta\phi_B)]$$

Where $\Delta\Phi_B$ is calculated with the charge conservation equation self-consistently

$$C_i[(V_G - V_{FB}) - \frac{(C_i + C_{sub})\Delta\phi_B}{C_i \cdot q}] = \frac{2}{L}\sum_{k_m^\perp}\sum_{k_l^\parallel}\frac{1}{1+e^{(E_{m,l}-\Delta\phi_B)/kT}} + \frac{1}{1+e^{(E_{m,l}-\Delta\phi_B+qV_D)/kT}}$$

$C_i$ is the physical coupling capacitance between gate and CNT channel, and $C_{sub}$ is the physical coupling capacitance between CNT channel and substrate. The first several subbands are doubly degenerated for all chiralities.

The transmission probability $T_{LR}$ and $T_{RL}$ equals to each other for elastic transport, but may not equal to each other for inelastic transport, e.g. the acoustic/optical phonon scattering. The acoustic phonon scattering ($l_{ap}$) and optical scattering ($l_{op}$) MFP in semiconducting CNT were normalized to the available final empty states which were assumed to be continuous to improve the runtime.

$$l_{op}(V,m,l) = \frac{\lambda_{op}D_o}{D(E_{m,l} - \hbar\Omega)[1 - f(E_{m,l} - \hbar\Omega - \Delta\phi_B + qV)]}$$

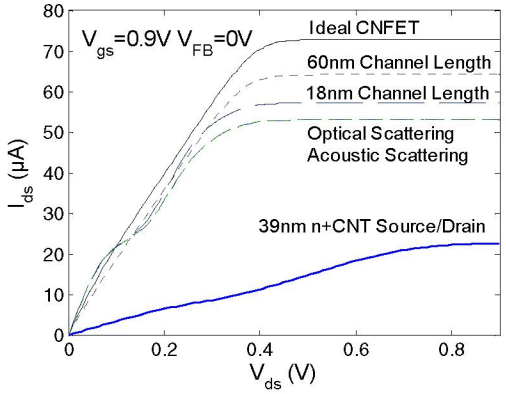
$$l_{ap}(V,m,l) = \frac{\lambda_{ap}D_o}{D(E_{m,l})[1 - f(E_{m,l} - \Delta\phi_B + qV)]}$$

Where $D(E)=D_o g(E)$ is the universal density of states (DOS) of CNT [7] which is valid for $E_{m,l} << V_\pi$, $\hbar\Omega$ (~0.16eV) is the optical phonon energy. $\lambda_{op}$ (~15nm) and $\lambda_{ap}$ (~500nm) are the optical and acoustic phonon scattering MFP in metallic CNT, respectively.

The electron accumulation effects on the drain diffusion dynamic capacitance due to phonon scattering, the impurity scattering in the doped source/drain and the band-to-band-tunneling current from drain to source are also taken into account in this compact model.

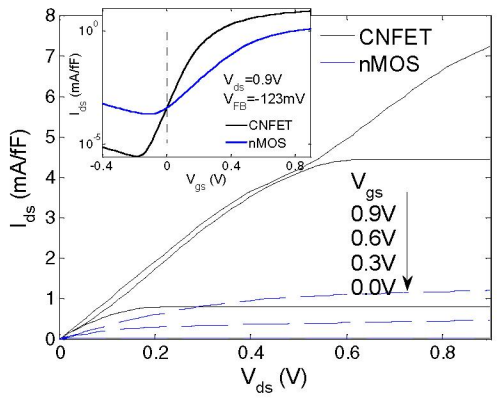
## III. Device Characteristics

To illustrate the use of this compact model, we show the device characteristics of an example CNFET. A planar gate, 4nm thick $HfO_2$, was used, and the channel length was set to be 18nm, the same as the printed channel length of 32nm node MOSFET. A (19, 0) CNT with the diameter 1.5nm was chosen to evaluate the device performance. A single power supply 0.9V was applied for high-performance application.




(a)




(b)

Figure 3. (a) Ids vs Vds with different non-idealities for (19, 0) CNFET. (b) Normalized Ids vs. Vds (Vgs) for 18nm (19, 0) CNFET and 32nm nMOS with the same off current per unit gate capacitance.

Both the drain current and transconductance are degraded by the device non-idealities (Fig.3a), especially by the reduced channel length and the resistance of doped source and drain. Significant quantum effects are observed with reducing channel length (Fig.3) due to the discrete substates populated in one by one. In terms of the on-current per unit effective gate capacitance, the 18nm (19, 0) CNFET show much better performance (6.03× for nFET and 13.7× for pFET) than 32nm node MOSFET with the similar channel length (Fig.3b) in device level, even with non-idealities (Table 1).

TABLE1. The gate effective capacitance and drain current comparison between nMOS and CNFET, in 32nm node.

| $L_{Channel}$ =18nm | Gate $C_{eff}$ | $I_{off}$ (nA/fF) | $I_{on}$ (mA/fF) | $I_{on}/I_{off}$ | CNFET/MOS |
|---|---|---|---|---|---|
| nMOS | 1.1fF/um | 383 | 1.198 | 3128 | N/A |
| nCNFET | 3.6aF/FET | 383 | 7.236 | 18863 | 6.03 |
| pMOS | 1.1fF/um | 253 | 0.5229 | 2066 | N/A |
| pCNFET | 3.6aF/FET | 253 | 7.172 | 28389 | 13.74 |

The transcapacitance pairs which are important to evaluate the circuit dynamic response are strong functions of bias conditions, and do not equal to each other except for $C_{gb}/C_{bg}$ (Fig.4, 5).

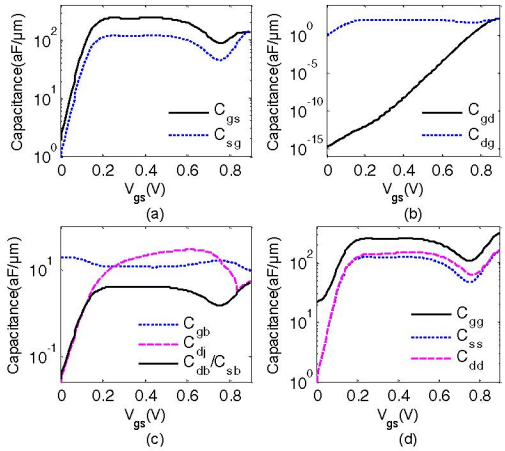



Figure 4. The transcapacitances, $C_{xy}=\partial Q_x/\partial V_y$, $C_{yx}=\partial Q_y/\partial V_x$, as a function of Vgs @ Vds=0.9V.

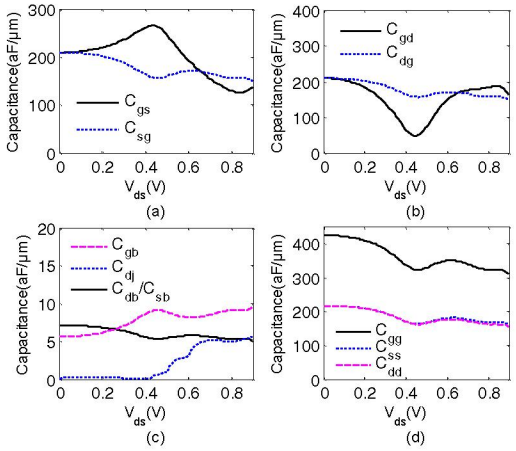



Figure 5. The transcapacitances, $C_{xy}=\partial Q_x/\partial V_y$, $C_{yx}=\partial Q_y/\partial V_x$, as a function of Vds @ Vgs=0.9V.

## IV. Circuit Performance

To evaluate the CNFET circuit performance, more non-idealities, e.g. the wiring capacitance, process induced CNT diameter variation, oxide thickness variation needs to be considered. The CNFET circuit performance highly depends on CNT diameter. Given the same off current per unit gate capacitance, due to the increasing quantum contact resistance and almost constant quantum capacitance, both the normalized on-current and inverter FO1 delay degraded with smaller CNT diameter (Fig.6).

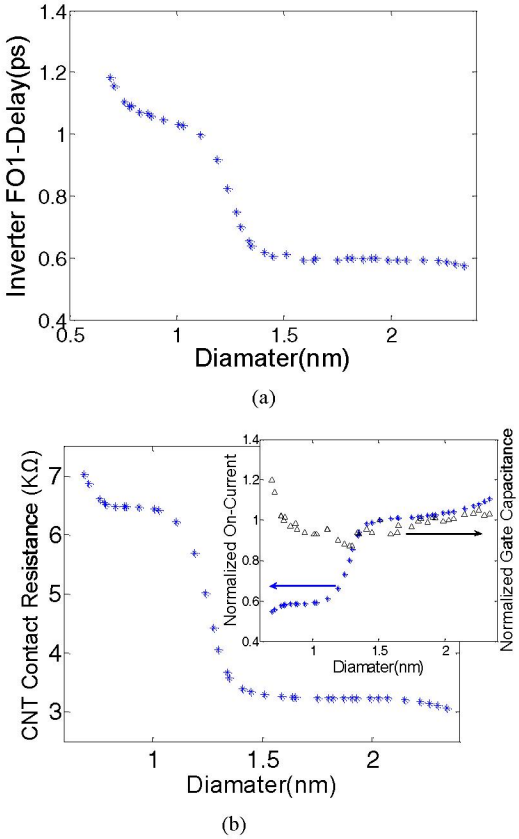



Figure 6. (a) The inverter FO1 delay vs. CNT diameter. (b) The CNT quantum contact resistance and normalized on-current vs. CNT diameter.

The circuit performance does not benefit from the aggressively scaled oxide thickness (Fig.7). For CNFET inverter without capacitive load, the FO1 delay increases abruptly with $T_{ox}$ less than 4nm due to the saturating on-current while the increasing gate capacitance of the load CNFETs. For CNFET inverter with practical wiring capacitive load (Fig.8), the circuit performance benefits from the scaled $T_{ox}$ down to 2nm (Fig.7).

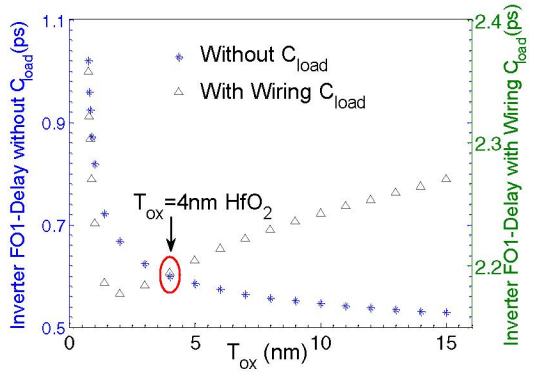



Figure 7. The inverter FO1 delay as a function of oxide thickness $T_{ox}$.

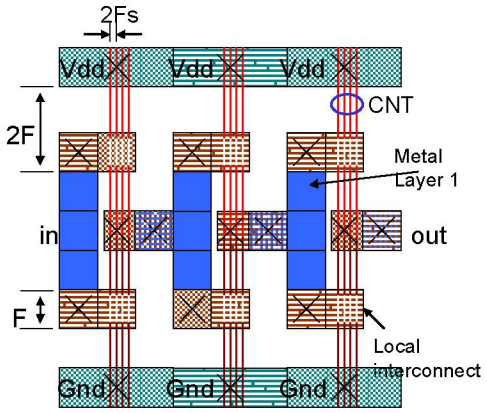



Figure 8. A sample layout for 3-stage CNFET inverter, F is the half optical lithography pitch, Fs is the half CNT pitch.

Multiple CNTs per FET (Fig.8) are allowed in our circuit model in order to evaluate the tradeoff between power and delay. For CNFET inverter without capacitive load, the FO1 delay is about 12 times smaller, matching the performance improvement in device level well, than that of 32nm CMOS inverter. With the consideration of the wiring capacitance of the random logic layout pattern, the speed enhancement was reduced to 3. The speed of CNFET inverter improves with the increasing number of CNTs per FET, and both the delay and power of CNFET inverter are dominated by the wiring capacitance because of the small quantum capacitance limited effective gate capacitance (Table 2).

TABLE 2. Inverter performance comparison between CNFET and CMOS technology (E/C=Energy/Cycle, m is the number of CNTs per FET, $C_L$ is the wiring load capacitance)

| | (19,0) CNFET, 18nm channel length | | | | | | 32nm CMOS |
|---|---|---|---|---|---|---|---|
| | m=1 | m=2 | m=4 | m=6 | m=8 | $C_L$=0 | |
| FO1 delay(ps) | 2.26 | 1.44 | 1.03 | 0.89 | 0.82 | 0.53 | 6.65 |
| E/C ($10^{-17}$J) | 6.76 | 8.82 | 13.0 | 17.3 | 21.6 | 1.99 | 54.1 |

## V. Summary

A circuit-compatible spice model for enhancement mode CNFET with real time dynamic response has been proposed and implemented. The device performance depends on CNT diameter, and aggressively scaled gate oxide doesn't benefit the performance. CNFET performance enhancement over CMOS technology in circuit level is lower than that in device level. This compact model with non-idealities is essential for and allows circuit level simulation with reasonable runtime.

## Acknowledgement

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