A compact model for Phase Change Memories

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Abstract—**In this paper we present the first inherently single-piece model describing the Phase Change Memories (PCM) electrical behavior. The model correctly reproduces for all bias and temperature conditions the behavior of both SET and RESET states, including the exponential pre-switching regime and the S-shaped negative differential resistance region. The model responds with resistance changes to different programming (SET or RESET) pulses, and retains the stored data. The proposed model provides a precious tool for the design of Non-Volatile Memory products based on the new Phase Change Memory concept.**

Keywords-Compact model;Phase Change Memory; PCM; Non-Volatile Memory; Multilevel

I. INTRODUCTION

Chalcogenide-based PCM appears to be the most promising candidate in the scenario for the next generation of Non-Volatile-Memory technologies [1]. In fact, considering the fundamental limitations that must be solved to push the floating-gate concept beyond the 32 nm technology node, PCM promises compatibility and low additional cost with respect to baseline CMOS, good scalability and improved performances in terms of writing/reading time, endurance, and bit level granularity. In order for the designers' community to fully explore the challenges and opportunities of such a promising new technology, an accurate compact model incorporating the most relevant underlying physical phenomena is strongly needed. We developed such an accurate compact model using simple C^∞ functions, which well describe the physics of the system including the electronic switching phenomena. The proposed approach is very flexible and can be easily adapted to a generic Spice-like simulator. In the following the main basic concepts of our model are presented, along with simulation results compared to the typical PCM experimental data.

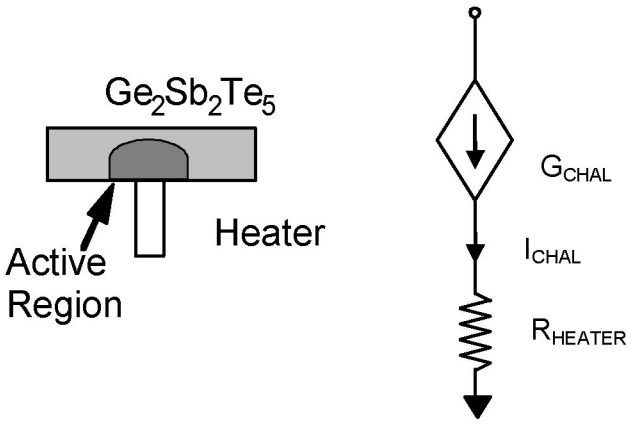

Figure 1. Schematic view of PCM cell with the equivalent circuit we

II. PCM-MACROMODEL

A. Main building block

The core of our model representing the PCM element is the Voltage-Controlled Current Source (VCCS) sketched in Fig.1. It includes an 'intelligent function' that is able to describe the electrical behavior of the chalcogenide-based resistor considering the transport mechanisms, the electronic switching and the resistance modulation as a function of the input voltage pulse. We stress that, overcoming recently proposed regional models [2], an inherently single-piece model that gives an accurate and continuous description of current and its derivatives in all device operation regions is presented for the first time. This approach is in line with the spirit of the Surface Potential models successfully developed for MOSFET devices [3]. With reference to Fig. 1, the following expression for I_1 current, as an addition of two contributions, has been introduced:

$$I_1 = I_\alpha(V_1, V_{status}) + F(I_1; I_{th}) \cdot [-I_\alpha(V_1, V_{status}) + F(V_1; V_{HOLD}) \cdot I_{ON}(V_1)] \quad (1)$$

where V_{status} is a variable that modulates the low-field resistance on the basis of a detailed analysis of the input pulse shape, I_{th} represents the threshold current for the Ovonic Threshold Switching (OTS) phenomenon to occur, and V_{HOLD} is the holding voltage (see Fig. 2). The *F(x;a)* expressions are Fermi-like smooth blending functions used to handle the I-V shape as a function of PCM state (SET or RESET) and to describe the electronic switching phenomena.

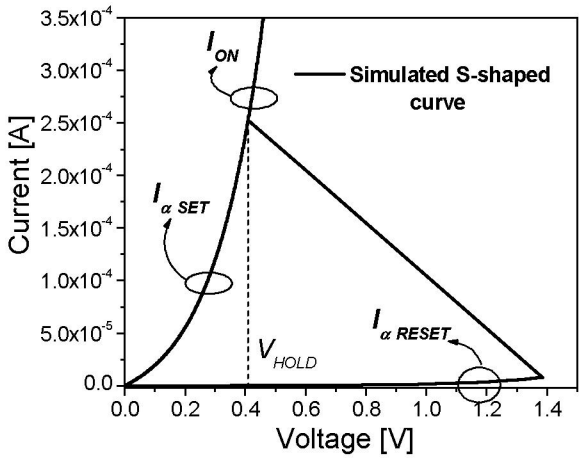

Figure 2. Typical I-V curve of a PCM element starting from the RESET state and switching to the SET one. The current contributions described by equation 1 have been reported.

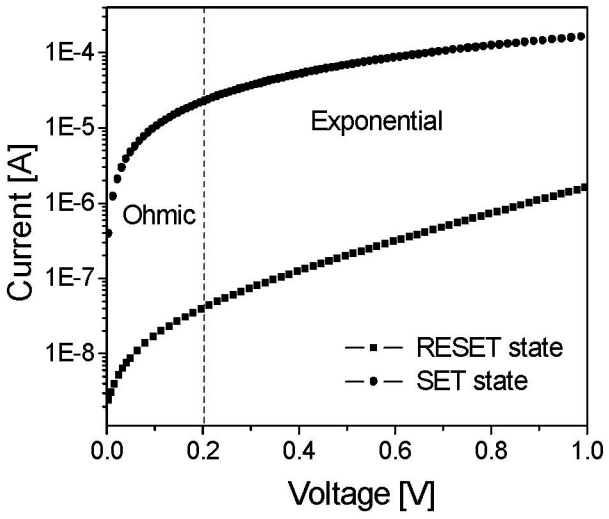

Figure 3. Simulated I-V curves of both amorphous (RESET) and crystalline (SET) states. Ohmic and exponential regions have been put in evidence.

The three branches of a complete I-V RESET-SET curve are reported in Fig. 2 with the labels of equation 1. I_α and I_{ON} currents describe the typical exponential-like trend of current of chalcogenide based resistors due to avalanche phenomena, as discussed in [4, 5], and here pictured by the following function:

$$I_\alpha(V_1, V_{status}) = \frac{1}{n_{status} \cdot R_0(V_{status}) \cdot \exp\left[\frac{E_{a,status}}{k} \cdot \left(\frac{1}{T} - \frac{1}{T_{ref}}\right)\right]} \cdot [\exp(n_{status} \cdot V_1) - 1] \quad (2)$$

that includes the activation energy parameter ($E_{a,status}$) and where n_{status} is the multiplication factor, R_0 represents the low-field resistance value, k is the Boltzmann constant, and T is the temperature. The main features pictured by these functions have been graphed in Fig. 3 and well describe both the ohmic and avalanche region. Note that the low-field resistance dependence as a function of temperature is included in equation (1) through the Arrhenius-like expression in agreement with [4].

B. *Auxiliary circuits*

According to a schematic picture, the RESET pulse provides a current amount that needs to melt the memory active region (T>600) and then rapidly switches off (t~50 ns) before crystallites could nucleate again to form a long range ordered matrix. On the contrary, the SET pulse switches off more slowly (t~150 ns) in order to provide enough time for the chalcogenide atoms to reorganize in a long-range ordered structure. Therefore, some auxiliary circuits are needed in order to allow VCCS to choose the status (SET or RESET), on the basis of the input pulse analysis, and to retain the stored data. In Fig. 4 we show the complete schematics of auxiliary circuits we exploited to reproduce the PCM electrical behavior under a SET or RESET programming pulse. In particular, we recognize schematically three blocks: the first one is an equivalent circuit describing the self-heating effect, which monitors the chalcogenide temperature and acquires the information about the occurrence of melting (if any). The second one is related to a detailed analysis of the fall down edge of the input pulse, computing the time spent in between the crystallization and melting temperatures (T_X and T_{melt}, respectively). Finally, the third one is useful to decide if the cell has been programmed in the SET or RESET state and to retain information. The flow diagram of circuits analyzing the input received pulse is pictured in Fig. 5.

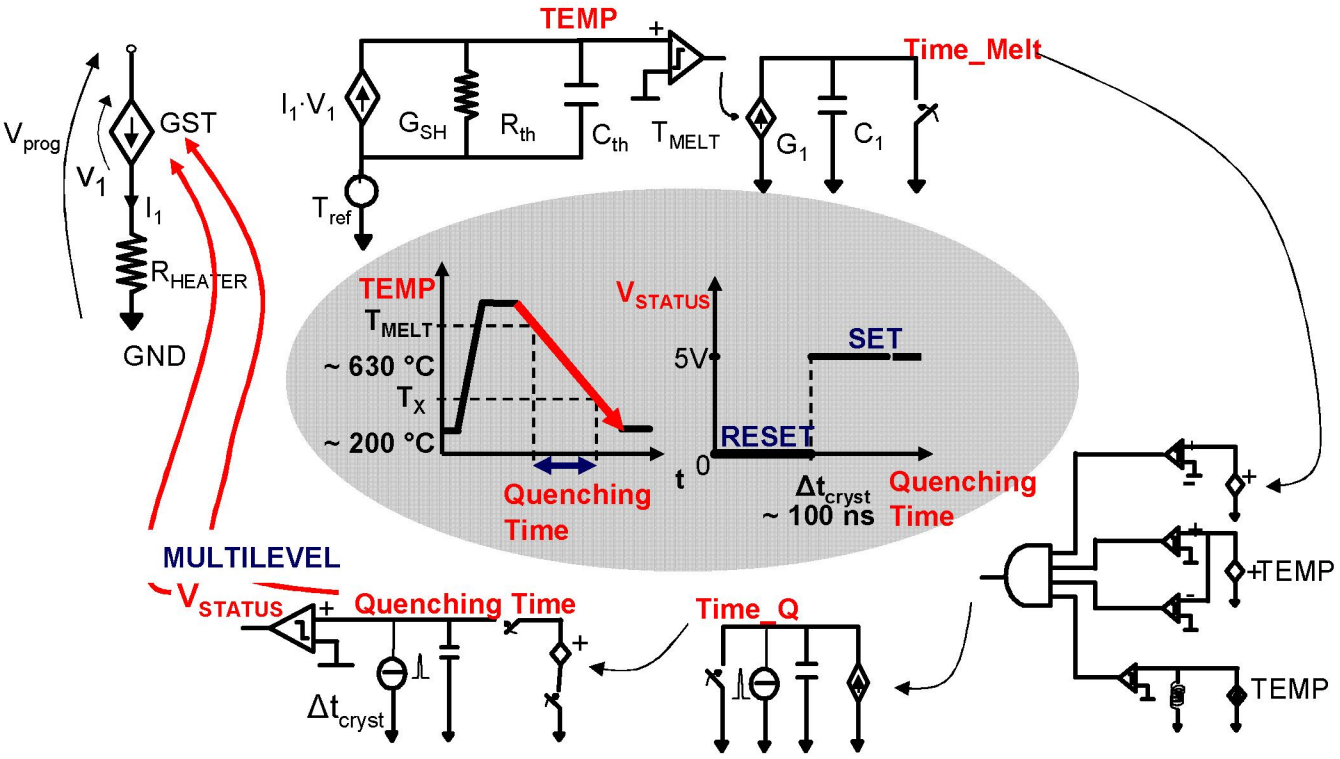

Figure 4. PCM equivalent circuit and auxiliary circuits working together to reproduce the PCM cell behavior.

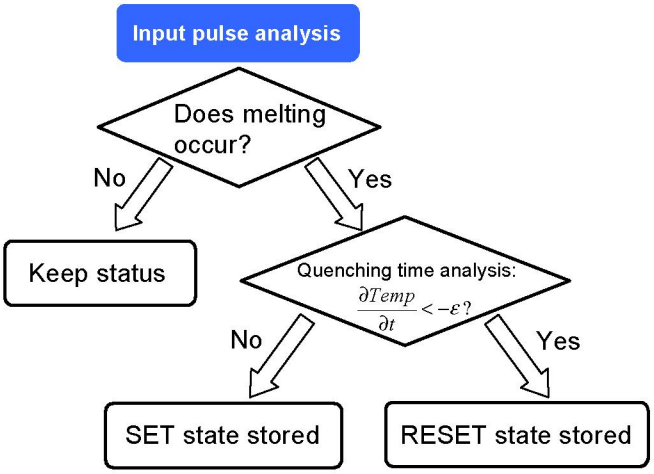

Figure 5. Schematic flow diagram of the logic followed by the auxiliary circuits to discriminate if the Phase-Change phenomenon occurs and to store data.

III. Simulation Results

In Fig. 6 we show both the temperature and status variable modification as a function of the programming and reading pulses, reported too. In particular, a sequence of four pulses has been sent: read, RESET, read, SET. As it can be observed the read pulses do not modify the cell state. On the contrary, the programming pulse with a fast falling edge provides the phase change lowering to 0 the status variable (RESET state), while the slow pulse brings again the status variable to high state, indicating the transition to SET state. In Fig. 7 the resistance as a function of the quenching time as simulated by using our model in comparison with experimental data is shown. A very good agreement can be observed. Moreover, we have also exploited the quenching time information captured by the auxiliary circuit of Fig. 4 as an analogical information discriminating the crystalline volume fraction that can be modulated by using different writing pulses. In Fig. 8 we report a simulation result obtained by applying progressively shorter pulses. This opens the possibility to employ our model also to investigate multilevel programming algorithms using the PCM technology.

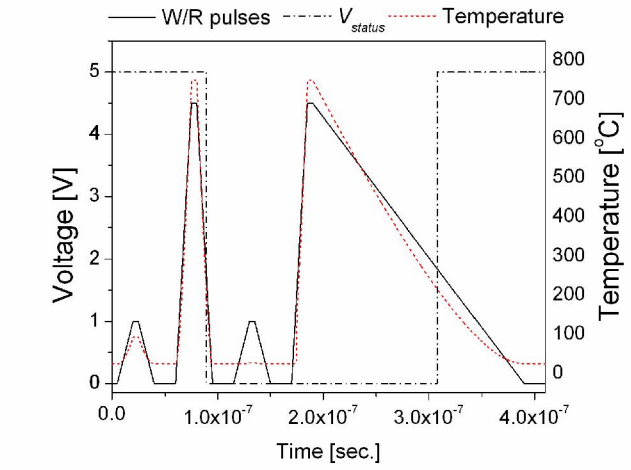

Figure 6. PCM Temperature and Status evolution during reading and writing pulse operation.

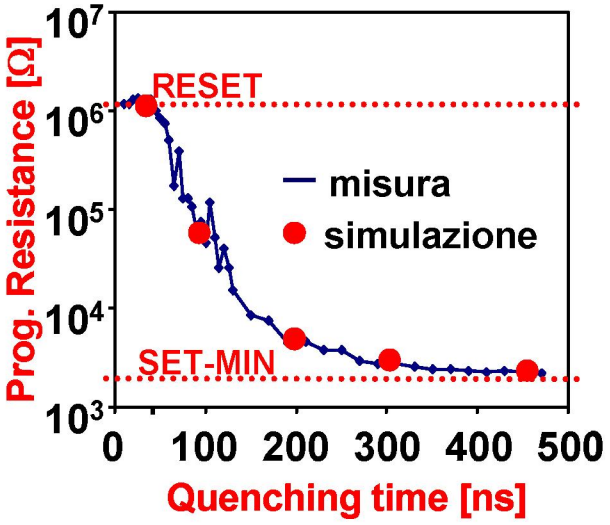

Figure 7. Low-field resistance modulation as a function of quenching time of the input pulse. Simulation points well fit experimental data.

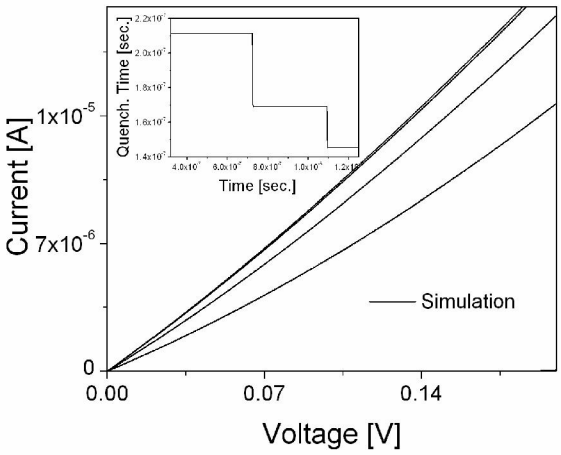

Figure 8. Example of Multi-level operation using three different writing pulses with progressively shorter quenching times as reported in the inset of Figure.

IV. Conclusions

The first single-piece model of a PCM element using only one VCCS has been presented. It provides an accurate description of all the main features of a real chalcogenide-based PCM cell with a handful of physical parameters. With the aid of auxiliary circuits monitoring the cell temperature and the time spent in the crystallization/melting temperature range, the PCM cell can choose its own final state. The logic state is finally stored. Also the multilevel design application of the model has been addressed.

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