Global Identification of Variability Factors and Its Application to the Statistical Worst-Case Model Generation

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***Abstract* - A novel methodology is presented to generate the worst-case model including extraction of its compact model parameters. This method enables physically accurate worst-case prediction in the early stage of device development concurrently. It is found through the intensive TEG analysis and TCAD simulation that correlations between process factors have a significant impact on the worst-case corner estimation. A new extraction method of compact model parameters based on error propagation analysis is developed to consider correlations between parameters.**

I. Introduction

In sub-100nm CMOS, it is a possible case that the worst-case performance does not improve, even if the typical performance does [1]. Recently it was pointed out the correlation between process factors influence the worst-case corner (Fig.1) [2]. And importance of FS/SF corners in advanced SRAM design was also pointed out [3]. Assumption of strong correlations between process factors is possible to lead to unrealistic worst-case estimation. Furthermore parameter extraction method considering correlations among compact model parameters was proposed [4].

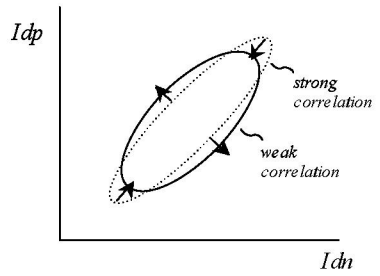


Fig.1. Impact of n-p correlation on the worst corner estimation.
FF/SS shrink, FS/SF expand.

For the short TAT development and high yield in mass production, accurate worst-case model prediction in the early stage of device development is desired. However, there are not sufficient measurement data during development phase to determine the worst-case in the statistically accurate manner. TCAD can be a strong tool to cover the shortage of data and predicting entire run-to-run/inter-wafer/intra-wafer variation in the production line. It needs only the variation data of each process step or equipment to predict the worst-case and therefore enables concurrent development.

In this work, we elucidate the significance of two "correlations" in the process of the worst-case model generation. One is the correlation between input process factors in predicting worst-case using TCAD-RSM and the other is that between compact model parameters in extraction (Fig.2).

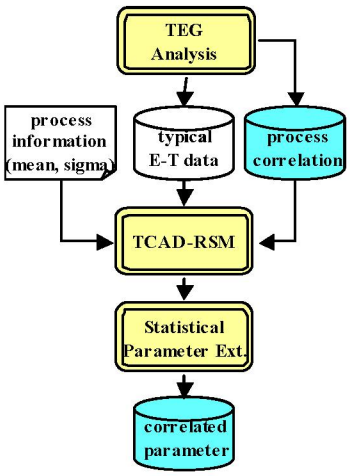


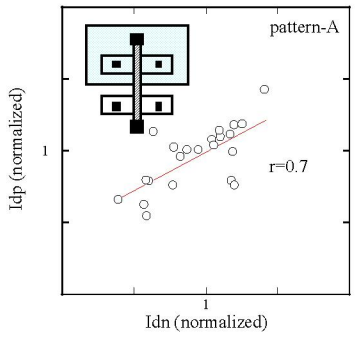
Fig.2. Overall concept and procedure of this work.

II. TEG Analysis

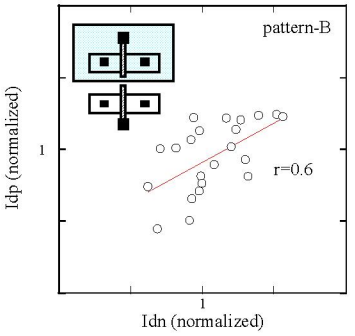
TEGs with different patterns and sizes are fabricated using *hp90*nm LSTP process to investigate not only the magnitude of variation but also the correlations among each E-T datum. All data shown here are taken from large (W_g>1μm) pattern, in which random variation and size variation (δW) can be neglected.

It is observed that FETs of pattern-A, which is a widely-used layout pattern in standard cells, have stronger I_{dn}-I_{dp} correlations than those of pattern-B (Fig.3). It is inferred that difference of L_{gn}-L_{gp} correlation after lithography and etching is a principal mechanism [2]. And it means that correlation coefficients depend on TEG layout patterns even if they are drawn with the same dimension. Therefore, variability evaluation with an actual layout pattern is necessary for precise worst-case prediction.

It is also found that there are negative correlations in V_{tn}-V_{tp} and I_{dn}-I_{dp} plots in long channel regions in contrast to positive correlations in short channel regions (Fig.4). There are two possible mechanisms for the negative correlation: one is a strong correlation between gate oxide thickness t_{ox} and fixed

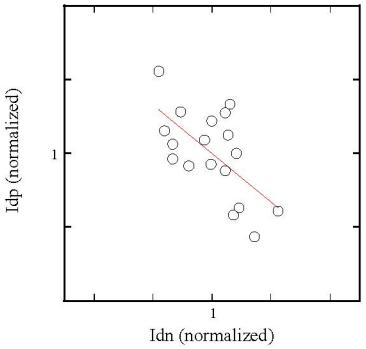


(a) pattern A : standard cell type

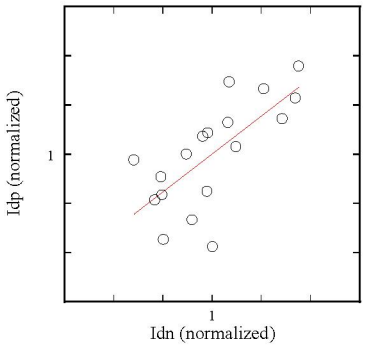


(b) pattern B : n-gate and p-gate split

Fig.3. Layout pattern dependence of I_{dn}-I_{dp} correlation (L_g=50nm).



(a)



(b)

Fig.4. Die-to-die variability and correlation between I_{dn} and I_{dp}. (a) L_g=1μm, (b) L_g=50nm

charge amount Q_f, which is related to the nitrogen profile in the oxynitride, and the other is screen oxide thickness t_{scr} fluctuation at channel implantation process. The former model proves inadequate by small correlation between EOT and V_t. On the other hand, the validity of the latter model is supported by negative correlation of C_{dep} between nFET and pFET (Fig.6). This is due to the difference of dopant species and peak depth (Fig.5).

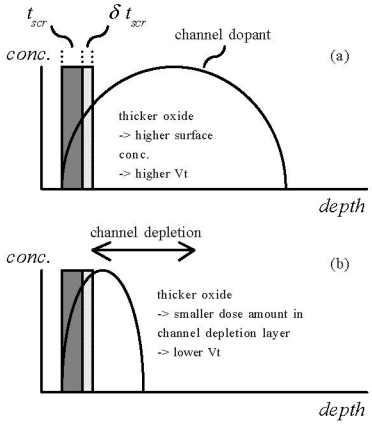


Fig.5. Illustration of V_t fluctuation due to t_{scr} fluctuation. (a) R_p > channel depl. width, (b) R_p < channel depl. width.

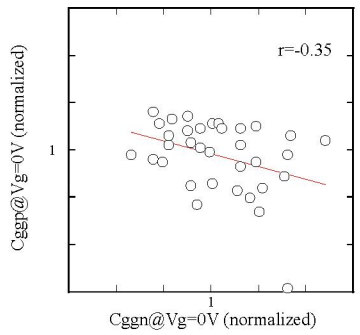


Fig.6. Correlation between C_{dep}(nFET) and C_{dep}(pFET).

III. Statistical Simulation by TCAD

Firstly, TCAD has to be well-calibrated using SIMS and E-T data of typical device. It is better to confirm the predictability of E-T data with slightly different process condition, for example, channel implantation dose or halo dose. It is found 3-stream diffusion model [5] and drift-diffusion device model with quantum mechanical correction model are satisfactory to represent electrical characteristics of our *hp90*nm devices over a wide range of device size (Fig.7). Fig.8 depicts the flow of worst-case prediction using TCAD-RSM [6]. After the sensitivity analysis, major process factors, L_g, *offset spacer*, t_{ox}, *channel dose* and t_{scr} in this work, are selected. Then, TCAD simulations are executed based upon DoE. After generating RSFs, Monte Carlo analysis is done in a few minutes.

Fig.9 shows the results of Monte Carlo simulation using TCAD-RSM considering the process correlations taken through TEG analysis. In short channel region, correlation of L_g between nFET and pFET has a significant impact, while t_{scr} has

a large impact in long channel.

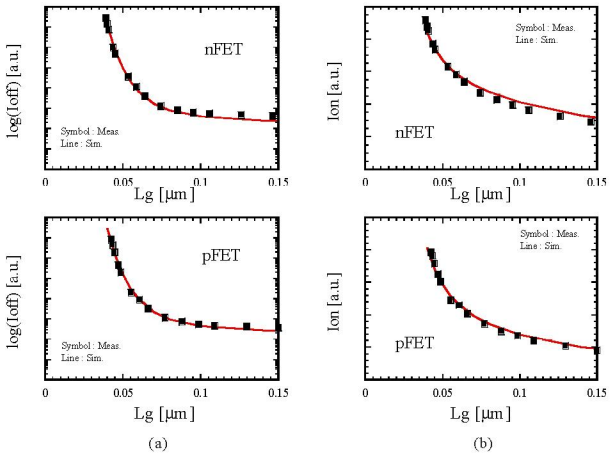


Fig.7. TCAD calibration results for Renesas *hp90*nm LSTP process.
(a) I_{off}-L_g, (b) I_{on}-L_g.

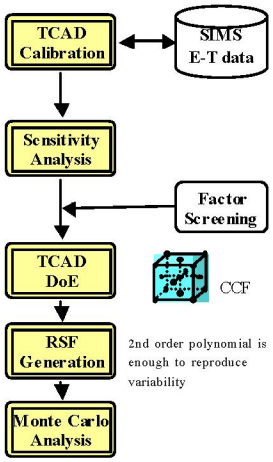


Fig.8. Flowchart of worst-case prediction by TCAD-RSM.

IV. Statistical Parameter Extraction

Compact model parameters are needed to evaluate circuit performances. However, since the parameters do not correspond one to one with process factors, that is, TCAD parameters, the correlation between the parameters have to be taken into account to represent the correlated variance of the electrical characteristics given by TCAD or Si [4].

The flowchart of a newly developed statistical compact model parameter extraction scheme is shown in Fig.10. In this scheme, the parameters are selected based on the factor loading in PCA. It is found that by using only three of BSIM4 parameters (XL, VTH0 and LPE0), statistical E-T characteristics of our hp90nm devices are well reproduced. The covariance matrix of these parameters **C**(**P**) is obtained from that of E-T data **Σ** and the parameter sensitivity matrix **A**, by applying the law of propagation of uncertainty [7]. This method has a great merit that once the parameter set of typical device and distribution of electrical properties are given, parameter variance is determined uniquely. Furthermore it is highly practical in that it does not

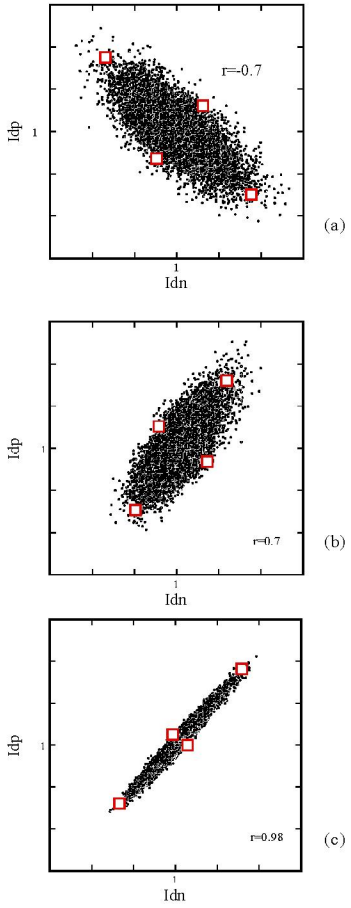


Fig.9. Predicted worst-case using TCAD-RSM.
(a) this work (L_g=1μm), (b) this work (L_g=50nm), (c) conventional approach (L_g=50nm).

need iterative calculation. Fig.11 and Fig.12 show the comparison of the statistical characteristics of measured E-T data with the results of Monte Carlo simulation using the extracted parameters. The L_g and bias dependence of the fluctuations of the measured I_{dn} and I_{dp} including their correlation agrees well with the simulated values. The t_{scr} effect mentioned above is reflected in the negative correlation between VTH0(nFET) and VTH0(pFET), and the positive correlation in short channel region is mapped into the correlation between XL(nFET) and XL(pFET), as shown in Fig.13. Thus, the statistically correlated, accurate worst-case model becomes available in circuit design environment.

V. Conclusions

A novel methodology has been proposed to generate the worst-case model parameters using TCAD and to extract its compact model in the early stage of device development. Through TEG analysis, it has been found negative correlation between I_{dn} and I_{dp} is observed in long channel region while positive in short. It has been also found correlation coefficient can be varied by device layout pattern even with the same size. And they have a great influence on the worst-case corner. TCAD-RSM was successful in reproduction and prediction of the dis-

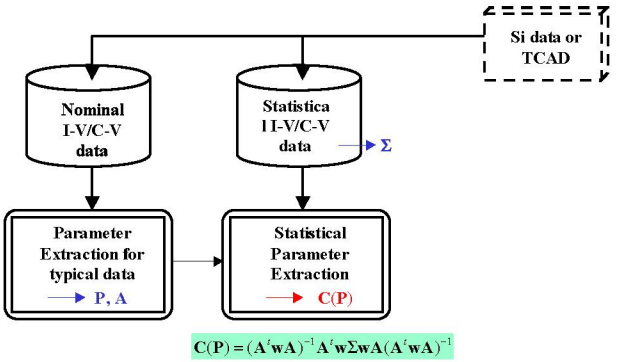


Fig.10. Flowchart of statistical parameter extraction.
P : parameter vector, A : Jacobian matrix that represents the sensitivities of compact model formula to each parameter, **Σ** : covariance matrix of E-T data, **w** : weighted function to normalize the difference of the current/capacitance which depends on the device geometry and the bias condition.

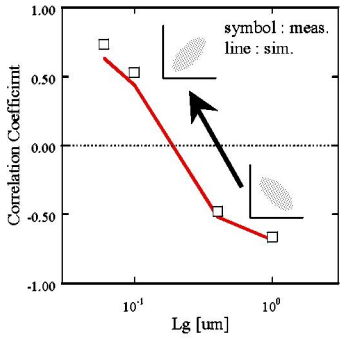
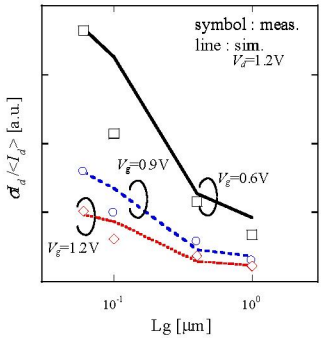
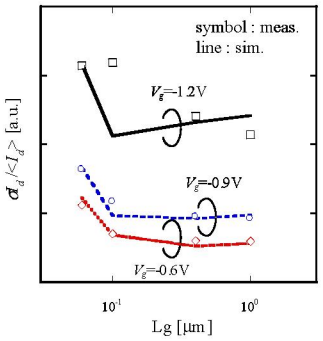


Fig.12. L_g dependence of I_{dn}-I_{dp} correlation coefficient.
Drastic shift from negative to positive during shortening L_g is well reproduced using statistically extracted parameters.

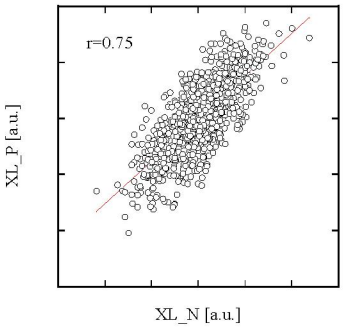


(a)



(b)

Fig.11. L_g and bias voltage dependence of σI_d. (a) nFET, (b) pFET.
Monte Carlo simulation using statistically extracted parameters reproduces the measurement data well.



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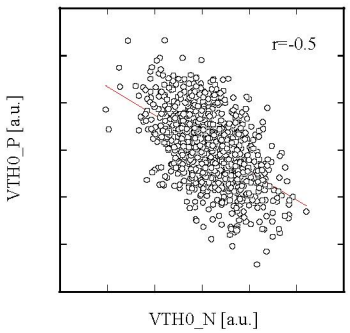

(b)

Fig.13. Correlations between extracted compact model parameters.
(a) XL, (b) VTH0

tribution of electrical properties. A new statistical parameter extraction method has been developed that is able to reflect parameter correlations and is easy to use. Only three parameters are enough to reproduce I-V fluctuations including correlations. Our total methodology enables a quite accurate evaluation of circuit performance and yield estimation before mass production.

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