Interface Barrier Abruptness and Work Function requirements for scaling Schottky Source-Drain MOS Transistors

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Abstract **-- Schottky source-drain (S/D) MOS transistor coupled with metal gate is a promising alternative to the conventional poly-Si gate and doped S/D MOSFET technology [1-2]. This paper explores through simulations the effect of metal S/D WF and the gradual change of barrier profile at the metal-semiconductor interface and in the few nanometers space around it on the n/p channel device performance. We present the S/D workfunction (WF) requirements for ultra short channel device design for the first time. Through modeling and fabrication, we also present the underlying physical explanation behind the existence of dual slope in I_d-V_g characteristics of metal S/D and Gate MOSFETs.**

Keywords – Schottky Source-Drain, TBGD, Dual Slope, Metal Gate, Metal Source/Drain

I. Introduction:

Schottky barrier (SB) source-drain(S/D) MOS transistor with metal gate (G), schematically shown in Fig. 1, is a strong candidate to replace conventional devices. This device offers several advantages over conventional MOSFET at nanometer scale such as complete elimination of the gate depletion and boron penetration problems, freedom from the requirement of ultra high doping in S/D/G regions, reduced thermal budget (thus avoiding thermal stability issues and improving compatibility with high-k dielectrics), reduced S/D series resistance and comparatively abrupt metal semiconductor junctions as we scale down to sub 50nm technology to achieve higher performance [1-4]. However, the choice of metal for the gate and the S/D may differ due to WF requirements. The gate work function (WF) requirement of metal has been extensively investigated [5]. This work gives insight and technology trend for workfunction selection for Schottky S/D regions in nanoscale n/p MOS devices. Although metal S/D-substrate interface could be comparatively abrupt, it may not be exactly a step barrier at the interface due to substantial modification of bands in a few nanometer spaces around interface. This is due to quantum mechanical effects, which are known to play a crucial role within 5nm of interface. In this light, this work presents the effect of a gradual change of the barrier modeled through Thermionic Barrier Gradient Distance (TBGD) on n/p MOS device performance. In addition to the effect of S/D and G metal WF on the device performance, we report modeling and fabrication results showing the existence of dual slope in the device I_d-V_g characteristics, along with the effect of gradual barrier change, TBGD, depicted in Fig 2. We provide important guidelines for the WF range for S/D and other device parameters requirement for nano-scale SB MOSFETs with metal gate as the gate length scales down.

II. Results and Discussion:

A. Dual slope Manifestation.

The width of the SB is spatially modulated by the gate voltage. As the barrier gets sufficiently thin, conduction occurs. The main injection mechanism is the thermionic emission through the SB at Schottky contacts. Thermionic Barrier Gradient Distance (TBGD) region A defines the interface potential distribution contributing a gradual barrier at the interface. TBGD region B is defined by charge electrostatics and is dominated by channel region dopant profile. Fig. 3 (a) shows the I_d-V_g characteristics of fabricated 4 micron gate length SB n-MOSFET with a metal S/D/G with T_{ox} 2.4 nm [6] and the Fig. 3 (b) shows I_d-V_g of simulated device with S/D WF of 4.55 eV and gate WF of 4.6 eV with channel doping of 5×10^{16} cm^{-3}. These experimental and modeling results clearly indicate the existence of dual slope in the device behavior. Physical reasons and phenomena are discussed in the following section. Fig 4 shows the substrate doping effect on the threshold voltage. For all subsequent simulations, the substrate doping is kept at 1×10^{17} cm^{-3}, as at this value, the threshold voltage and device performance with mid-gap metal gate can be achieved close to device design requirements of ITRS 2004[7].

B. Physical Modeling and WF requirements with scaling.

According to Bethe theory [8], the shape of the barrier is immaterial and the current flow depends solely on the barrier height. However, through modeling and simulation, we report the effect of gradual change in barrier height using *Taurus* simulator [9]. The Schottky Barrier Tunneling (SBT) model used augments the thermionic emission boundary condition at Schottky contacts to

include the carrier transport with this tunneling. The tunneling through SB is calculated as a distributed generation rate [10]. Fig. 5 (a) and (b) shows the I_d-V_g characteristics of simulated n-channel device with 45nm gate length with TBGD-A region transition of 0, 1, 2 nm at V_{ds} 100mV and 1V respectively with S/D WF=4.5eV, gate WF=4.6eV. This observed behavior of dual slope is mainly due to the following reasons: a) S/D WF b) Non-abruptness in interface potential distribution between metal and the semiconductor underneath – the larger the distance over which the barrier region spreads, the more prominent is the dual slope, c) Gate length of the device d) Gate Oxide Thickness T_{ox} which in effect controls the effective voltage felt by the channel and also the effective voltage appearing across the TBGD region. This dual slope behavior in I_d-V_g characteristics is seen when the S/D metal workfunction is 4.3 eV and above for the n-channel device with gate length 45 nm. Two different slopes are present before and after the device is turned *ON*. Best subthreshold swing and I_{on}/I_{off} ratio is achieved with combination of S/D metal WF≤4.3eV and metal gate WF=4.6eV for 45nm gate length, shown in Fig. 6 (a), (b). Fig 7 shows the I_d-V_d characteristics of the same device. But as the gate length is further reduced the same S/D metal WF shows splitting in I_d-V_g as seen in Fig 8. For 20nm gate length in Fig. 8 the I_d-V_g splitting starts at S/D WF≤4.2 eV. At the Metal-Semiconductor interface, the depletion width depends on built-in potential and doping of the semiconductor. The gradual change (increase) in barrier height at TBGD region *A* helps more carriers to overcome the barrier and in due course gaining momentum and thus successfully overcoming TBGD region B, thus enhancing total current and hence the dual slope is seen. This poses a limitation on process requirement of high quality interface electrically and the minimum gate length achievable. Right selection of S/D metal WF is also critical from the drive current standpoint as depicted in Fig. 6 (a) and (b). A metal with WF closer to the values where no splitting is observed shows the best device performance. Fig. 9 (a) and (b) shows the S/D metal WF requirement as the function of gate length and the possible gate length window in which it can be used for a particular technology node for n and p type SB transistors respectively. Fig 10 shows the minimum gate length achievable for a particular TBGD value.

III. Conclusion:

Metal source/drain workfunction requirement with reducing gate length and corresponding gate length processing window is provided for both n- and p- SB MOSFET. Manifestation of non-desirable dual slope in I_d-V_g characteristics is shown to be associated with TBGD and metal WF value. S/D WF ≤ 4.2 eV for n-SBMOSFET and > 4.95eV for p-SBMOSFET are suitable down to the gate length of 15nm.

References:

[1] J. R. Tucker, Chinlee Wang, P. Scott Carney, "Silicon field- effect transistor based on quantum tunneling", *Appl. Phys. Let 1994*, Vol 65, Issue 5, pp. 618-620.

[2] J. Kedzierski, P. Xuan, E.H Anderson, J. Bokor, Tsu-Jae King, Chenming Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime", *Elect. Devcie Meeting* 2000, pp. 57-60.

[3] K. Ikeda, Y. Yamashita, A. Endoh, T. Fukano, K. Hikosaka, T. Mimura, " 50-nm gate Schottky source/drain p-MOSFETs with a SiGe channel", *Elect. Device Letter 2002*, Vol 23, Issue 11, pp. 670-672.

[4] C. Wang, J. P. Snyder, J. R. Tucker, "Sub-40nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors", *Appl. Phys. Lett. 1999*, Vol. 74, Issue 8, pp. 1174-1176.

[5] D. A Buchanan, F. R. McFeely, J. J. Yurkas, "Fabrication of midgap metal gates compatible with ultrathin dielectrics", *Appl. Phys. Lett. 1998*, Vol. 73, Issue 12, pp. 1676-1678.

[6] S. Zhu et al., " Schottky-barrier S/D MOSFETs with high-k gate dielectrics and metal-gate electrode", *Elect. Device Letter 2004*, Vol-25, Issue 5, pp. 268-270.

[7] International Technology Roadmaps for Semiconductors 2004.

[8] H. A. Bethe, MIT Radiation Lab 1942, Report 43.

[9] Taurus Medici ™. Version W-2004.09, Sep 2004.

[10] MeiKei Ieong, P. M. Solomon, S. E. Laux, H.-S. P. Wong, D. Chidambarrao, *Elect. Devcie Meeting* 1998, pp. 733-736.

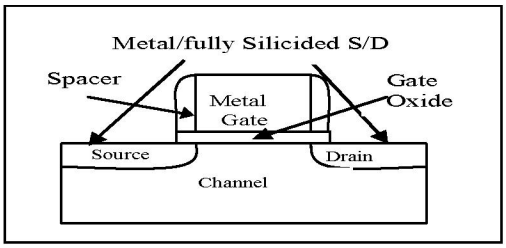

Fig.1. Schematic of Schottky Barrier MOSFET with Metal gate and Metal/fully Silicided Source/Drain

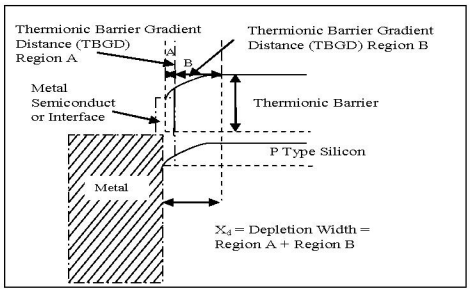

Fig.2. TBGD Region A is at Metal Semiconductor Interface of n-SBMOSFET. TBGD Region B is due to doping controlled electrostatics.

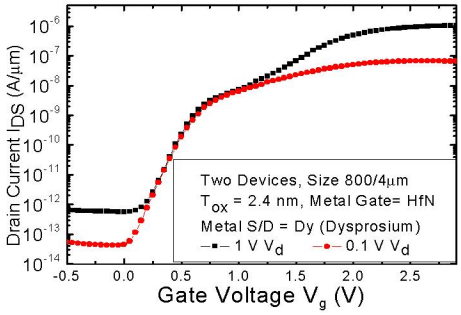

Fig.3(a). Experimental I_d-V_g characteristics of n-SBMOSFET showing dual slope. [6]

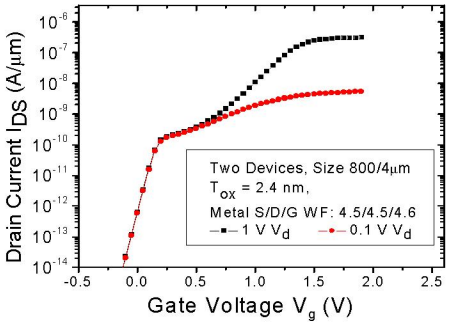

Fig.3(b). I_d-V_g Characteristics of simulated n-SBMOSFET showing two distinct slopes with very close agreement with fabricated device in Fig. 3(a).

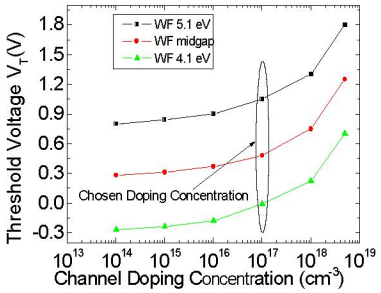

Fig.4. Threshold voltage dependence on Channel doping for nSBMOSFET with Metal gate WF of 5.1 eV, midgap and 4.1 eV for T_{ox}=2nm and Long channel length. Gate WF of 4.6 eV is chosen to give a reasonable V_T of 0.38 V.

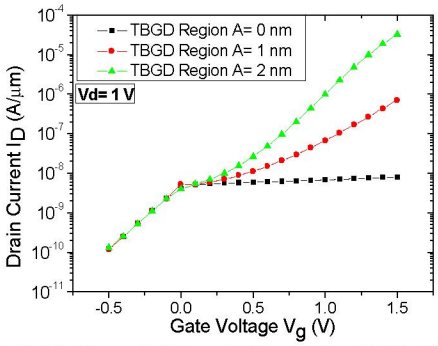

Fig.5(a). I_d-V_g Characteristics of 45nm SB n-MOS FET with V_d=1V and different TBGD distance with S/D WF = 4.5 eV and G WF= 4.6 eV.

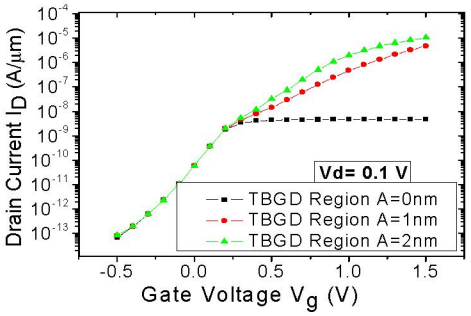

Fig.5(b). I_d-V_g Characteristics of 45nm SB n-MOS FET with V_d=0.1V and different TBGD distance with S/D WF =4.5 eV and G WF= 4.6 eV.

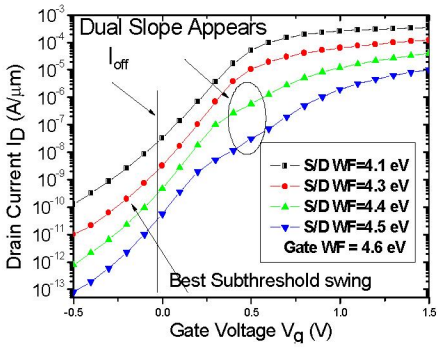

Fig.6(a). Effect of S/D WF Change on I_d-V_g Characteristics at TBGD 2nm and V_{ds}=0.1V. L_g = 45nm

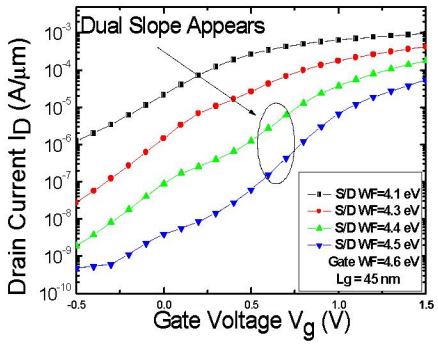

Fig.6(b). Effect of S/D WF Change on Gate Characteristics at TBGD 2nm and V_{ds}=1V.

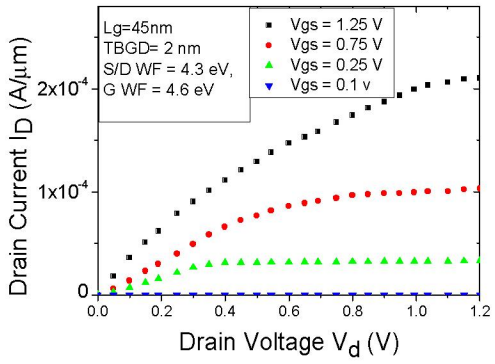

Fig.7. I_d-V_d curve of SB n-MOS FET with TBGD = 2nm. Gate Length = 45 nm

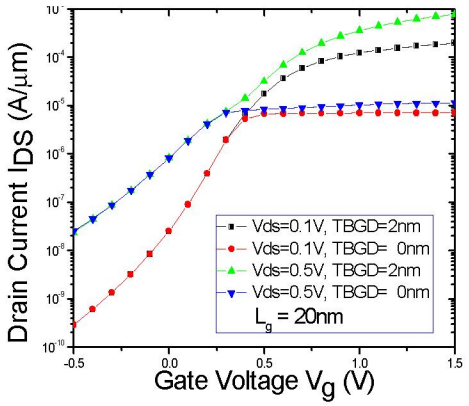

Fig.8. I_d-V_g curve of SB n-MOS FET with gate Length = 20 nm – showing significant splitting occurring even at S/D WF 4.3 eV, which in the case of 45 nm device was almost zero.

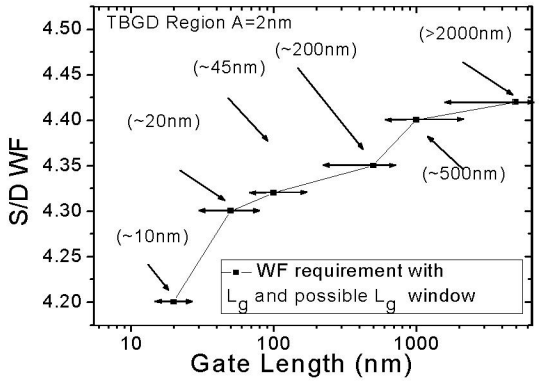

Fig.9(a). Metal S/D workfunction requirement Vs Gate length and possible process window in parenthesis () with that Source/Drain workfunction value for SB S/D n-MOS FET.

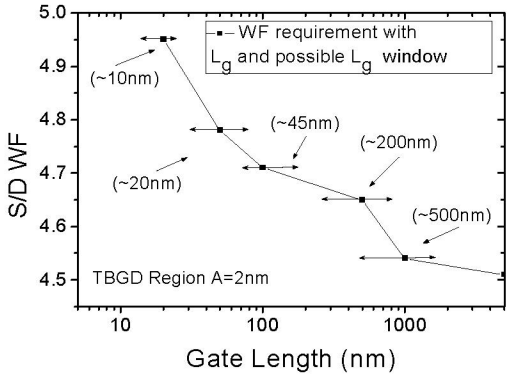

Fig.9(b). Metal S/D workfunction requirement Vs gate Length and possible gate length window in parenthesis () with that Source/Drain workfunction value for SB S/D p-MOS FET.

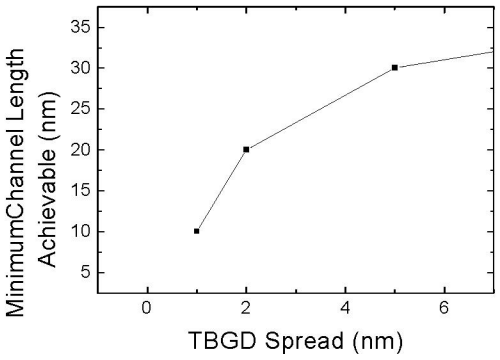

Fig.10. Minimum gate Length achievable with a given TBGD, that determines the degree of abrupt potential distribution needed.

