# Small-Signal Analysis and Modeling of Asymmetric Source/Drain Parasitic Resistances for DRAM Access Transistors in Low-Power Applications

Young Pil Kim, Matthew Ulrich, Praveen Vaidyanathan, Venkat Ananthan, Chandra Mouli, and Kunal Parekh
R&D Process Development, Micron Technology Inc., Boise ID, 83716, USA

***Abstract*— The small-signal conductance technique was extended to extract asymmetric source/drain parasitic resistances. It was also applied in order to analyze the $t_{\rm WR}$ delay of DRAM cell transistors in production and to develop a non-planar cell transistor such as Recessed Access Device (RAD) for low-power DRAM cells. Factors limiting the drive current for planar and non-planar access transistors in the low-power DRAM cells were discussed.**

## I. Introduction

Identifying the parameters that limit the drive current in planar and non-planar access transistors, like the recessed access device (RAD) [1], is crucial for highly scaled devices with long data retention time. It is challenging to meet the requirements for low-leakage and high-drive currents in low-power DRAM designs where both are yield-limiting factors in production [2]. For asymmetric source/drain (S/D) scheme, which can be used to minimize storage node junction leakage without significant reduction of the drive current of the access devices, analysis for improvement of S/D parasitic resistance is more challenging compared to the symmetric transistors. Even though considerable research has been done [3]–[6], there is no efficient method of extracting the asymmetric S/D resistances, $R_s$ and $R_d$, that can be implemented as a routine monitor for yield improvement in manufacturing.

This paper suggests an extended small-signal technique to extract $R_s$, $R_d$, and channel resistance ($R_{ch}$) separately for the asymmetric S/D. It also discusses the application of this technique to analyze $t_{\rm WR}$ (time to write data "1" or "0" into a storage cell) characteristics and identify the current limiting factor in RAD.

## II. Extension of the Small-Signal Technique

The small-signal conductance measurement technique, which directly measures conductance between the S/D nodes with a very small amplitude AC signal, is an attractive methodology since it is a compact and intuitive method compared to other techniques (*i.e.* DC conductance method [3] which requires considerable numerical calculation to solve a nonlinear system of equations). However, the conventional small-signal technique [4] can not detect the asymmetry in $R_s$ and $R_d$ because it applies zero drain to source DC bias, $V_{ds}$, to prevent the voltage drop through $R_s$ and $R_d$. The no-voltage drop gives benefits in extracting intrinsic parameters and total source/drain resistances, $R_{sd}$, but it loses asymmetry information in the conductance measurement.

Separate extraction of $R_s$ and $R_d$ needs the application of non-zero $V_{ds}$ to enable the asymmetry information to be included into the measured conductance. This leads more complex conductance equations. The measured conductance $g_{ds}$ at non-zero $V_{ds}$ in the linear region, *i.e.* $V_{ds} = 0.1V$, is expressed as,

$$\begin{aligned} g_{ds} &= \frac{1}{R_{sd} + 1/g^*_{ds}} \\ &= \frac{\beta_0 \left(V^*_{gs} - V_T - V^*_{ds}\right)}{1 + \theta \left(V^*_{gs} - V_T\right) + \beta_0 R_{sd} \left(V^*_{gs} - V_T - V^*_{ds}\right)} \end{aligned} \tag{1}$$

where $g^*_{ds}$, $\beta_0$, $\theta$, $V_T$, $V^*_{gs}$ and $V^*_{ds}$ are intrinsic channel conductance, gain constant, mobility reduction factor, threshold voltage, and internal gate and drain voltages, respectively. Here, $g^*_{ds} = \beta_0(V^*_{gs} - V_T - V^*_{ds})/(1 + \theta(V^*_{gs} - V_T))$, $V^*_{gs} = V_{gs} - I_{ds}R_s$, and $V^*_{ds} = V_{ds} - I_{ds}R_{sd}$. The schematic diagram showing experimental set-ups, applied voltages, and variable definitions were in Fig. 1.

The change of variables in the derivative of $g_{ds}$, $dg_{ds}/dV_{gs} = dg_{ds}/dV^*_{gs} \cdot dV^*_{gs}/dV_{gs} = dg_{ds}/dV^*_{gs} \cdot (1 - g_m R_s)$, simply correlates $g_{ds}/(dg_{ds}/dV_{gs})^{1/2}$ with external variables to that of internal variables after a short derivation from Eq. 1,

$$\begin{aligned} \frac{g_{ds}}{\sqrt{\frac{dg_{ds}}{dV_{gs}}}} &= \frac{g^*_{ds}}{\sqrt{\frac{dg^*_{ds}}{dV^*_{gs}}}} \left(1 - g_m R_s\right)^{-1/2} \\ &= \sqrt{\frac{\beta_0}{1 + \theta V^*_{ds}}} \left(V^*_{gs} - V_T - V^*_{ds}\right) \left(1 - g_m R_s\right)^{-1/2}. \end{aligned} \tag{2}$$

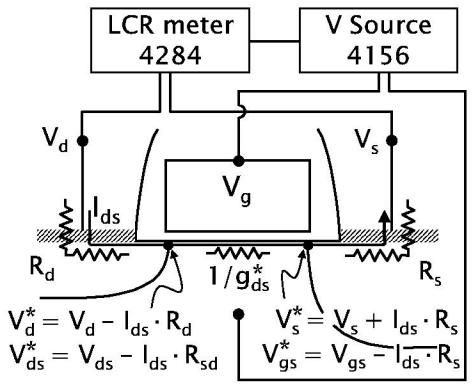


Fig. 1. Schematic of an asymmetric-access transistor of a DRAM cell and the definition of variables, including series resistances and internal and external (applied) voltages on the transistor.

 

When the $V_{ds} = 0$, Eq. 1 and Eq. 2 become,

$$g_{ds} = \frac{\beta_0 (V_{gs} - V_T)}{1 + (\theta + \beta_0 R_{sd})(V_{gs} - V_T)} \quad (3)$$

$$\frac{g_{ds}}{\sqrt{\frac{dg_{ds}}{dV_{gs}}}} = \sqrt{\beta_0} \cdot (V_{gs} - V_T) \quad (4)$$

since $V_{ds}^* = V_{ds} = 0$, $V_{gs}^* = V_{gs}$, and the transconductance $g_m = (dI_{ds}/dV_g)\,|_{V_{ds}=0} = 0$, which are the same equations as in the conventional small-signal technique [4].

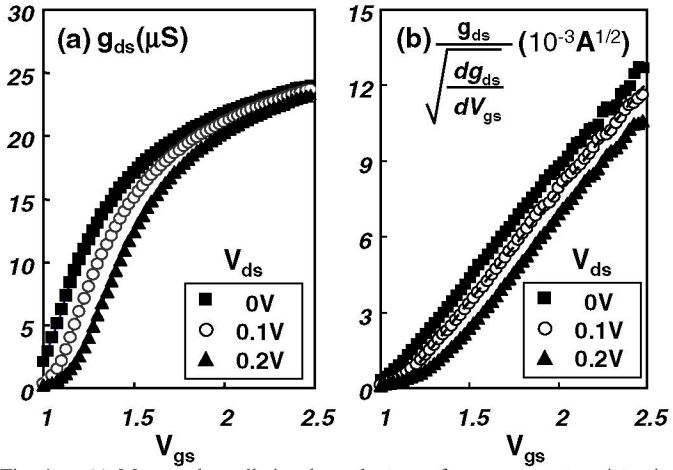


Fig. 2. (a) Measured small-signal conductance for an access transistor in a 78nm technology DRAM cell. (b) $g_{ds}/(dg_{ds}/dV_{gs})^{1/2}$ curves for a zero drain voltage and two non-zero $V_{ds}$

Measured $g_{ds}$ and $g_{ds}/(dg_{ds}/dV_{gs})^{1/2}$ are plotted in Fig. 2 (a) and (b), respectively, for an asymmetric access transistor at $V_{ds} = 0$, 0.1, and $0.2V$. The curves in Fig. 2 (b), which can be expressed by Eq. 2, have good linearity over almost the entire overdrive region up to $V_{gs} = 2.5V$ even for non-zero $V_{ds}$. This enables us to use the x-axis intersection of the curve to extract $R_s$ or $R_d$ using Eq. 1; measurement of $g_{ds}$ with $V_{ds} = 0$ is used to obtain $\beta_0$, $\theta$, $V_T$, and $R_{sd}$ through the equations in the conventional small-signal technique (Eq. 3 and Eq. 4) [4]. However, in reality, a small variation in the intersection due to measurement noise results in significant changes in $R_s$ and $R_d$. The ratio of forward and reverse measurement of $g_{ds}/(dg_{ds}/dV_{gs})^{1/2}$, $F/R$, was used to minimize the noise sensitivity.

$$F/R = \sqrt{\frac{1 + \theta V_{sd}^*}{1 + \theta V_{ds}^*}} \frac{V_{gs} - V_T - V_{ds} + I_{ds} R_d}{V_{gs} - V_T - V_{sd} + I_{sd} R_s} \sqrt{\frac{1 - g_{mr} R_d}{1 - g_{mf} R_s}}, \quad (5)$$

where $g_{mf}$ and $g_{mr}$ are transconductances measured in forward and reverse directions, respectively. As seen in Fig. 3, $F/R$ is very stable and a slowly varying function in the entire overdrive region, allowing us to use it to extract the $R_s$ and $R_d$. It should be noticed that $F/R$ has a singularity at $V_{gs} = V_T + V_{sd}^*$ which is around $1.2V$, as shown in Fig. 3. Curve fittings using $I_{ds}$ and $g_{ds}$ equations with the extracted values of $\beta_0$, $\theta$, $V_T$, $R_s$, and $R_d$ appear in the inset of Fig. 3. Here we can see good agreement between the measured data and the fitted curves, indicating the method works well in extracting the parasitic, as well as intrinsic, device parameters.

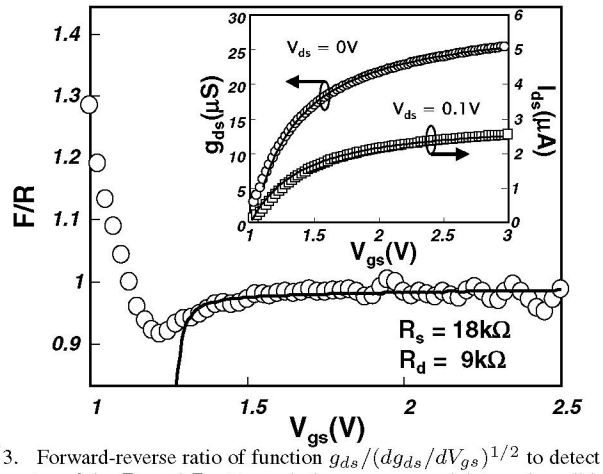


Fig. 3. Forward-reverse ratio of function $g_{ds}/(dg_{ds}/dV_{gs})^{1/2}$ to detect the asymmetry of the $R_s$ and $R_d$. Open circles are measured data and a solid line is the calculated curve from Eq. 5. Curve fittings using $g_{ds}$ and $I_{ds}$ equations with the extracted parameters are in the inset.

## III. Application for the $t_{WR}$ Analysis and RAD Development

Experimental lots of RAD and planar access devices with asymmetric S/D fabricated following the 78nm DRAM process integration sequences were used to investigate series resistance components and correlate them to $t_{WR}$. We obtained device parameters from single-access transistor test structures at 9 different sites in each wafer and correlated them to the average $t_{WR}$ characteristics of several die located in the same reticle area of the test structures. In the case of RAD, we used three different test structures that utilized different integration processes such as lightly-doped drain (LDD) implantation and contact formation schemes.

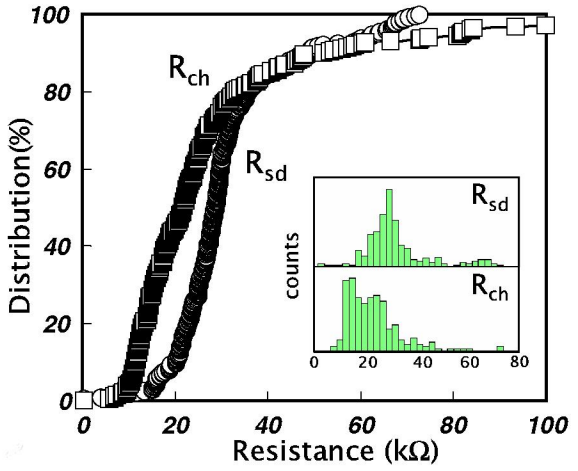


Fig. 4. Distributions of extracted $R_{sd}$ and $R_{ch}$. Differential distributions were depicted in the inset.

Fig. 4 shows cumulative and differential distributions of $R_{ch}$ and $R_{sd}$ for planar access devices (Differential distribution is

TABLE I

EXTRACTED DEVICE PARAMETERS, INCLUDING $R_s$ AND $R_d$

| $\beta_0$ $(10^{-5}A/V^2)$ | $\theta$ $(1/V)$ | $V_T$ $(V)$ | $R_s$ $(k\Omega)$ | $R_d$ $(k\Omega)$ | $R_{sd}$ $(k\Omega)$ | $R_{ch}$ $(k\Omega)$ |
|---|---|---|---|---|---|---|
| 8.71 | 0.558 | 1.03 | 18.2 | 9.01 | 27.2 | 12.0 |
| 7.53 | 0.806 | 1.12 | 14.1 | 14.8 | 28.9 | 18.4 |
| 7.72 | 0.611 | 1.06 | 18.9 | 11.4 | 30.3 | 14.5 |
| 5.20 | 0.583 | 1.12 | 8.84 | 15.1 | 23.9 | 22.2 |
| 6.71 | 0.653 | 1.14 | 14.2 | 14.5 | 28.8 | 24.5 |

shown in the inset of Fig. 4). The $R_{sd}$ is higher than $R_{ch}$, as shown in Fig. 4. It can be seen that the current drivability of the access transistor is limited by $R_{sd}$ and it could significantly influence product yields due to $t_{\mathrm{WR}}$ failure.

Table I lists the extracted parameters of access devices in 78 nm technology node. Four typical values from three different lots and the average values of 298 measurements were listed on the table. Despite the large variation of $R_s$ and $R_d$, the average values are the same even for the asymmetric S/D scheme. Spreading of current path in source (cell) junction can explain the same $R_s$ and $R_d$. Although the lower doping density in the cell junction leads to higher $R_s$, the deeper cell junction, which spreads the current path, reduces the $R_s$ and consequently results in the $R_s$ value being approximately the as same as $R_d$. The simulated $I$-$V$ curves obtained from the modeled test structures representing the cell and bit-side portions of an access transistor are shown in Fig. 5. It shows

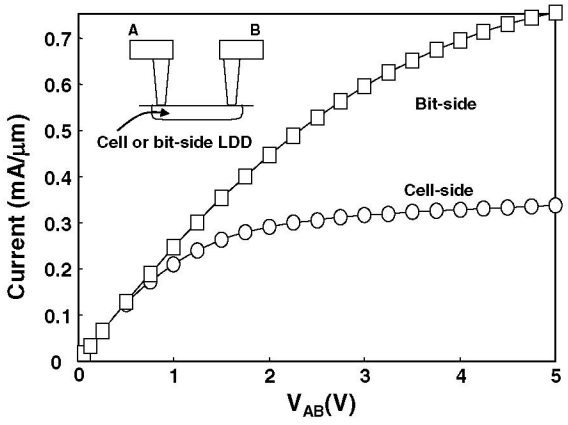


Fig. 5. Simulated I-V curves for cell and bit-side LDDs and contacts.

no resistance difference between cell and bit-sides below 1V. The large difference in the region above 2V can be attributed to the appearance of a thicker depletion layer at the LDD-substrate junction for the cell-side, which leads to a thinner conducting layer of the LDD sheet compared to the bit-side.

Fig. 6 shows the correlation between $R_{sd}$ and $t_{\mathrm{WR}}$ failures. It can be seen that the current drivability of the access transistor is limited by $R_{sd}$ and it significantly affects product yields due to the $t_{\mathrm{WR}}$ failure.

In case of RAD, it can be expected that the elongated channel, as shown in the simulated junction profile in Fig. 7,

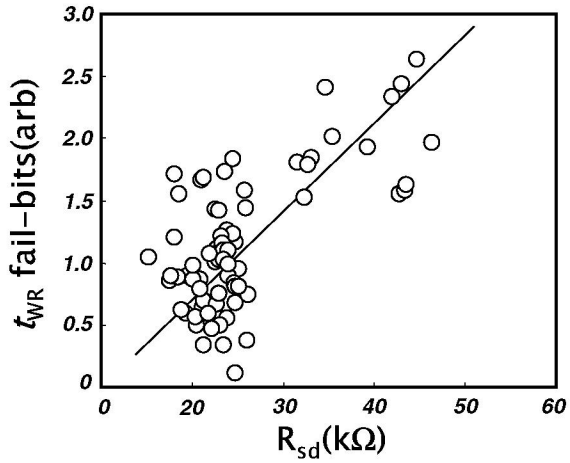


Fig. 6. Correlation between $R_{sd}$ and $t_{\mathrm{WR}}$ failure under a specific $t_{\mathrm{WR}}$ sorting condition.

results in higher $R_{ch}$ and consequently causes the severe $t_{\mathrm{WR}}$

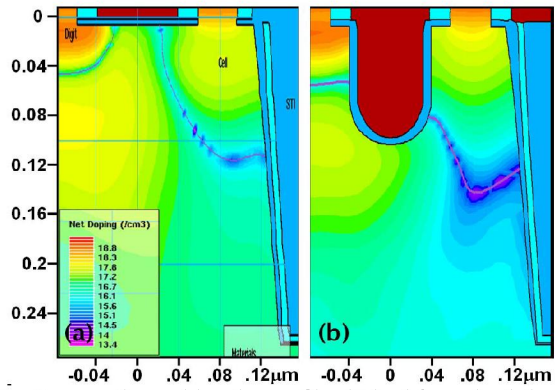


Fig. 7. Cross-section and junction profile obtained from simulation for the asymmetric access transistors: (a) planar, (b) RAD.

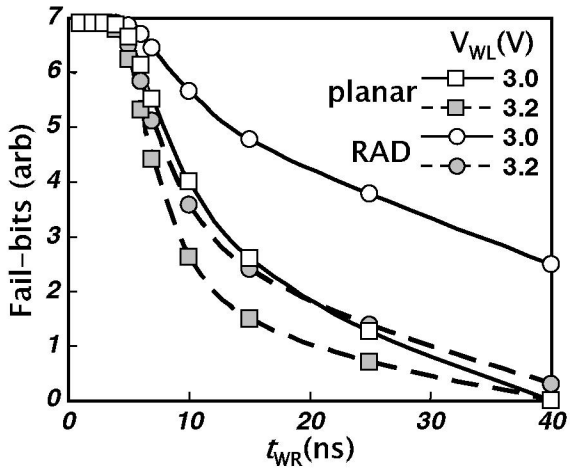


Fig. 8. Fail-bit versus $t_{\mathrm{WR}}$ trends as a function of word-line drive voltage for the DRAM cells with RAD and planar access transistors.

failures. Fig. 8 shows number of fail-bits as a function of word-line drive voltage, $V_{\mathrm{WL}}$ for RAD and planar access devices

 

under different $t_{\mathrm{WR}}$ conditions. The number of $t_{\mathrm{WR}}$ fail-bits is a strong function of $V_{\mathrm{WL}}$ for RAD compared to the planar device. This indicates that the intrinsic characteristics, $g^*_{ds}$, could act as one of the current limiting factors for RAD and its optimization along with $R_{sd}$ minimization is critical. However, the elongation of the channel length also depends on the implantation condition of the LDD formation; deeper LDD junction forms shorter channel and vice versa. Fig. 9 shows the distribution of $R_{ch}$ and $R_{sd}$ for the different RAD test structures with different processes. The lowest LDD dose sample (RAD A) shows a significant increase of $R_{ch}$ as well as $R_{sd}$ as shown in Fig. 9. This indicates that optimization of S/D junction profile is still important in the improvement of current drivability of the RAD since the junction profile mostly determines both $R_{ch}$ and $R_{sd}$. The $R_{ch}$ and the $R_{sd}$ for a well-optimized RAD has similar distributions, with slightly lower values and sharp distribution, compared to the planar devices as shown in Fig. 9.

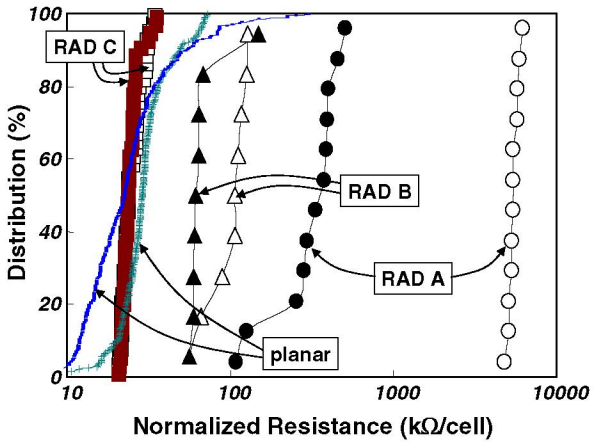


Fig. 9. Distributions of $R_{ch}$ and $R_{sd}$ for RAD test structures with different integration processes comparing to the distribution of planar cell transistors from Fig. 4. Solid symbols: $R_{ch}$; open symbols: $R_{sd}$ distributions.

## IV. Conclusion

A modified, small-signal technique for asymmetric device parameter extraction was designed and implemented to study $t_{\mathrm{WR}}$ delay in low power DRAM products and for the development of RAD. The $R_{sd}$, determined by $R_s$ and $R_d$ for asymmetric S/D, mostly limits the on-current of the access transistor and reduces yield due to $t_{\mathrm{WR}}$ delay both for RAD and planar access devices. Even though $R_{ch}$ portion is usually higher for RAD, control of the S/D junction profiles is still the most important factor in improving the current drivability since it determines both $R_{ch}$ and $R_{sd}$ for the RAD devices.

## Acknowledgment

Authors thank to Rongsheng Yang and Ravi Iyer for their helpful discussion on the simulation and the RAD integration process.

## References

[1] J. Y. Kim *et al.*, "The breakthrough in data retention time of DRAM using recess-channel-array transistor (RCAT) for 88nm feature size and beyond", *Proc. VLSI Symp.* 2003, p. 11

[2] Y. P. Kim *et al.*, "Electrical analysis of DRAM transistors for the root-cause addressing of the $t_{RDL}$ time-delay failure", *Microelectronic Reliability* vol. 43, p. 1461 (2003)

[3] C. -L. Lou *et al.*, "A novel single-device DC method for extraction of the effective mobility and source-drain resistances of fresh and hot-carrier degraded drain-engineered MOSFET's", *IEEE Trans. Electron Devices* vol. 45, p. 1371 (1998)

[4] F. C. Kong *et al.*, "Extraction of MOSFET threshold voltage, series resistance, effective channel length, and inversion layer mobility from small-signal channel conductance measurement", *IEEE Trans. Electron Devices* vol. 48, p. 2870 (2001)

[5] S. Y. Chou and D. A. Antoniadis, "Relationship between measured and intrinsic transconductances of FET's", *IEEE Trans. Electron Devices* vol. 34, p. 448 (1987)

[6] A. Cros *et al.*, "New extraction method for gate bias dependent series resistance in nanometirc double gate transistors", *Proc IEEE ICMTS Symp.* 2005, p. 69

 