Simulation of NOR-Flash Memory Cells Focusing on Narrow Channel Effects on V_{TH} Dispersion

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***Abstract*— In this paper, we present novel simulation results including threshold voltage (V_{TH}) dispersions caused by process variations for highly scaled NOR-flash memories. Fully 3-D process and device simulations are applied to calculate both of a cell (or drain) current and an F-N current with a realistic device shape. Owing to the narrow channel effects, not only the cell current but also the F-N current is found to be sensitive to the shapes of an active area and a floating gate. The dependence of the currents on the device shape is strongly related to the degradation of the V_{TH} dispersion and hence makes it difficult to miniaturize the memory cell. In addition, we propose a suitable cell structure in order to control the V_{TH} dispersion.**

***keywords*—flash memory, threshold voltage dispersion, narrow channel effect, F-N tunneling current, 3D simulation**

I. INTRODUCTION

NOR-flash memories offer random read access, electrical write and erase, and nonvolatile data storage [1]. Data is translated into a charge stored in a floating gate (FG) which modulates V_{TH} of the memory cell transistor. Hence, a fluctuation in the charge disperses the V_{TH} directly. The V_{TH} dispersion of the cell transistor is one of the most important issues, since a large V_{TH} dispersion causes a drastic reduction of the tolerance between programmed state ("0") and erased state ("1") as shown in Fig.1, which results in the unacceptable error in the read operations.

F-N tunneling of electron from FG to Si substrate is utilized in the erase operation. On the other hand, the program operation is owing to hot-electron injections to the FG. Because of the rapid saturation nature of the hot-electron current during the program operation, the V_{TH} dispersion of the programmed state is generally smaller than that of the erased state [2]. Furthermore, the V_{TH} dispersion of the erased state causes an undesirable negative V_{TH} and a narrow design window [3]. We, therefore, focus on the V_{TH} dispersion of the erased state in the present paper.

With respect to the cell transistors of the NOR-flash memories, width of an active area (AA) has been aggressively scaled down in comparison to the gate length. The narrower AA width leads to stronger narrow channel effects (NCE). We first discuss the NCE on current-voltage characteristics of the cell transistors, referring to a relation between the NCE and the dispersion of the intrinsic neutral V_{TH} (V_{THN}). Then, we investigate the dependence of the process condition on the dispersion of the erased state V_{TH} (V_{THE}), showing a suitable shape of the cell structure.

II. SIMULATION

A. Reverse Narrow Channel Effect

In Fig.2, SEM cross-sections of two types of the cell transistor fabricated with different process conditions are shown. The FG widths of both cells are almost the same, although the AA width of cell-B is narrower than that of cell-A. In order to evaluate the effect of the device shape on their characteristics, 3-D process simulator HySyProS [4] is fully utilized to reproduce precisely the actual device structure. We also have carefully dealt with the mesh generation (Fig.2 and Fig.3) to minimize numerical error in the simulation results of electrical properties.

In Fig.4, we demonstrate the simulated current-voltage characteristics of the cell transistors under charge neutrality conditions in the FG, showing the reasonable agreement with the experimental results. In addition, we have experimentally found that the V_{THN} of cell-B is lower than that of cell-A, which is consistent with the simulation results. As shown in Fig.5, we observed larger current density near the AA corner in cell-B than that in cell-A. Therefore, the lower V_{TH} in cell-B than that in cell-A (Fig.4) is attributed to the larger reverse NCE for cell-B than that for cell-A.

B. Dispersion of intrinsic neutral V_{TH}

The dispersions of the V_{THN} are calculated under charge neutrality conditions in the FG for two typical shapes of the cell transistor illustrated in Fig.6. The parameters chosen as random variables are the width of the AA (W_{AA}), the width of the FG (W_{FG}), the thickness of the tunnel oxide (T_{OX}), and the height of the FG (T_{FG}). Cells A' and B' have the same mean values of W_{AA}, T_{OX} and T_{FG}, whereas W_{FG} of cell-B' is larger than that of cell-A'. The simulation results shown in Fig.7 reveal that the dispersion of the V_{THN} depends on the device shape. Furthermore, we found that the strong NCE in cell-B'

enlarges the V_{TH} dispersion even in the charge neutrality conditions.

C. *Dispersion of erased state V_{TH}*

The erased state V_{TH} can be expressed as

$$V_{THE} = V_{THN} + \frac{\beta}{C_{CF}} Q_E \,, \tag{1}$$

where β, C_{CF} and Q_E represent capacitive coupling ratio, capacitance between the FG and the control gate, and erased state charge in the FG, respectively. Hence, the dispersion of the V_{THE} has two origins, one is the dispersion of the V_{THN} and the other is the dispersion of the Q_E. The Q_E is calculated by the following equation.

$$Q_E = Q_P - \int I_{FN}\, dt = Q_P - \int f\left(Q(t)\right) dt \tag{2}$$

The programmed state charge in the FG (Q_P) is assumed to be constant for simplicity. The F-N tunneling current (I_{FN}) is determined as a function of the intermediate state charge (Q) by means of a steady state simulation (Fig.8). In Fig.9, the calculated dispersions of the Q_E are compared for cells A' and B' which have the same mean value of the β. It is found that the dispersion of the Q_E also depends on the device shape as is the case of the V_{THN}.

We can adduce one of the reasons using the following series of analytical expressions for the I_{FN}, Q_E and Q_E dispersion.

$$I_{FN} = aE^2 \exp(-bE) \tag{3}$$

$$Q_E = \frac{bC_{CF}T_{OX}}{\beta}\left[\ln\left\{\exp\left(\frac{b}{E_0}\right) - \frac{ab\beta T_E}{C_{CF}T_{OX}}\right\}\right]^{-1} - C_{CF}V_{CG} \tag{4}$$

$$\frac{\Delta Q_E}{\Delta T_{OX}} \approx bC_{CF}\left[\ln\left\{\exp\left(\frac{b}{E_0}\right) - \frac{ab\beta T_E}{C_{CF}T_{OX}}\right\}\right]^{-1} \tag{5}$$

V_{CG}, E, E_0 and T_E represent control gate voltage, electric field in the tunnel oxide, electric field at the initial time and total erase time, respectively. From (5), it proves that larger C_{CF} deteriorates the Q_E dispersion. As previously stated, cells A' and B' have the same mean value of the β. However, the mean C_{CF} of cell-B' is 5% larger than that of cell-A' because of the larger W_{FG}. The Q_E dispersion of cell-B', consequently, should be 5% worse than that of cell-A'. This result also applies to the mean values of the Q_E. Although the tendency is well reproduced in the numerical simulations, the simulation result shows dispersion of cell-B' is 45% larger than that of cell-A'. The reason of the discrepancy will be described later.

Finally, the dispersions of the V_{THE} are simulated under charge balanced boundary conditions in the FG having Q_E calculated by (2). In Fig.10, scatter plots for cells A' and B' are shown, taking the Q_E as the x-axis and the V_{THE} as the y-axis. Obviously, the points of (Q_E, V_{THE}) concentrate around regression lines which correspond to (1). This fact implies that our simulation results are free from crucial meshing noise. Then, the V_{THE} dispersions of both cells can be found in Fig.11, showing the dispersion of cell-A' is smaller than that of cell B'.

By combining (1) and (5), an analytical expression of the V_{THE} dispersion excluding the V_{THN} dispersion is derived as follows:

$$\frac{\Delta V_{THE}}{\Delta T_{OX}} = b\beta\left[\ln\left\{\exp\left(\frac{b}{E_0}\right) - \frac{ab\beta T_E}{C_{CF}T_{OX}}\right\}\right]^{-1} \tag{6}$$

From (6), the V_{THE} dispersion is found to be a weak function of the C_{CF}, which is different from the case of the Q_E. The dispersions of cells A' and B', therefore, should be equivalent. This result conflicts with the simulation results shown in Fig.10 and Fig.11. The unexpected large V_{THE} (also previously mentioned Q_E) dispersion of cell B' is due to extra F-N conduction near the AA corner as shown in Fig.12. The extra conduction arises from the electric field concentrated near the AA corner. The total F-N current in (3) is modulated by the extra current which depends on not only T_{OX} but also W_{AA} and W_{FG}, since the effective area of the extra current increases relatively as the W_{AA} becomes smaller and the electric field near the AA corner grows as the W_{FG} becomes larger. Therefore, the F-N current of cell-B' is particularly sensitive to the device shape.

III. Cell Guidline

The simulation results reveal that some process techniques for controlling the NCE are indispensable to reduce the dispersion of the V_{THE}. The self-aligned STI process [5] is one of the most available techniques to achieve the requirement. Because the FG and AA are formed with RIE simultaneously, the FG width becomes slightly smaller than the AA width. This feature contributes to deconcentrating the electric field into the AA corner. A rounding of the AA corner is desirable to disperse the electric field further. At the same time, a bird's beak shape in the tunnel oxide should be removed, since it makes the device shape unstable.

IV. Conclusion

We have shown that the NCE modulates characteristics of the NOR-flash memory cells and hence complicates the problem of the V_{TH} dispersion, while taking advantages of the fully 3-dimensional process and device simulations. The applicability of the 3-dimensional simulation techniques is by no means limited to the NOR-flash memory cells and they are expected to become increasingly important in the near future.

References

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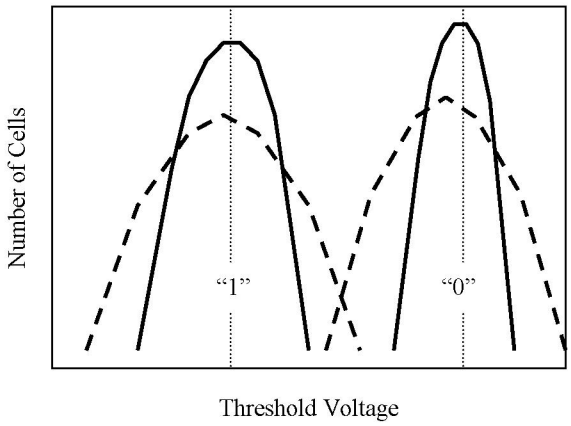
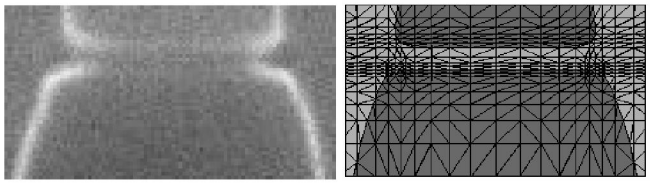
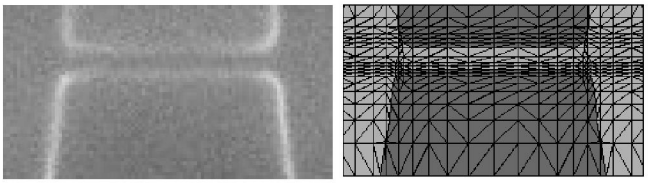


Figure 1. Schematic illustration of V_{TH} dispersion in NOR-flash memory cell. "1" and "0" represent erased and programmed states, respectively. Small dispersion (solid-lines) separates "0" state and "1" state. But there are indistinguishable cells in the case of large dispersion (dashed lines).



(A) $W_{AA}>W_{FG}$



(B) $W_{AA}=W_{FG}$

Figure 2. SEM cross-sections in word-line direction (left hand) and corresponding simulation results (right hand) of cell transistors fabricated with different process conditions. In each figure, AA and FG are found at the lower side and upper side, respectively.

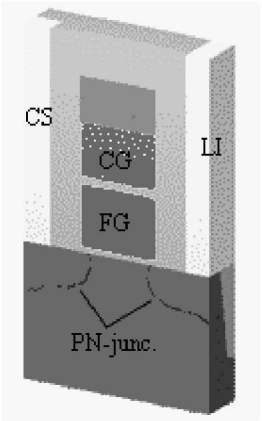


Figure 3. Bird's-eye view of cell transistor calculated by 3-D process simulator HySyProS. CS and LI denote bit-line and common source-line, respectively. Bird's beak shapes of CG and FG are reproduced through dedicated simulation of post-oxidation.

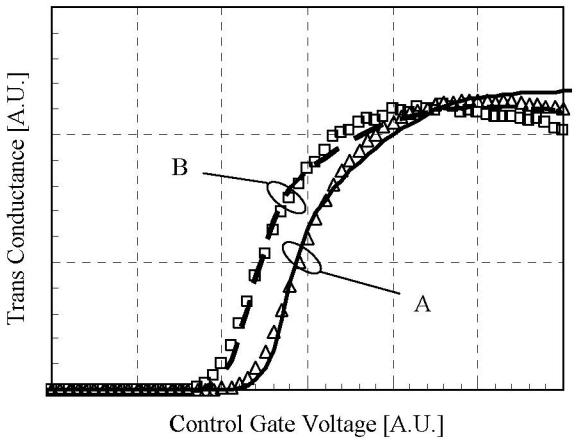
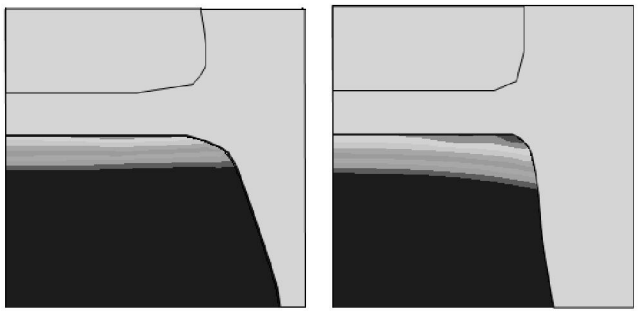
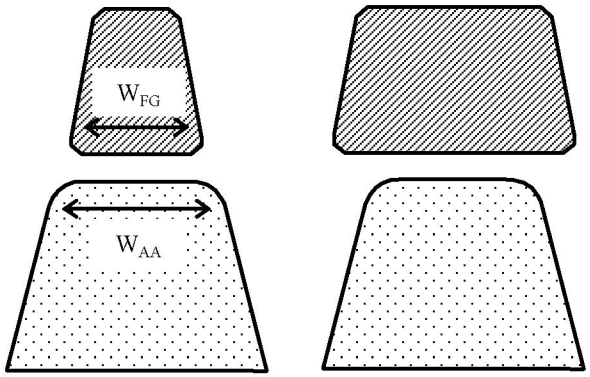


Figure 4. Comparison between measured (triangles and squares) and simulated (solid and dashed lines) I-V characteristics of cell transistors A and B shown in Fig.2.



(A) (B)

Figure 5. Simulated current densities of cell transistors A and B shown in Fig.2 on cross-sections in word-line direction., applying equivalent voltages to both FG's.



(A') $W_{AA}>W_{FG}$ (B') $W_{AA}<W_{FG}$

Figure 6. Two typical types of cross-section in word-line direction. In simulations, each device shape is simply characterized by parameters such as AA width and FG width for analyzing V_{TH} dispersion. Cells A' and B' are equivalent excluding mean FG width.

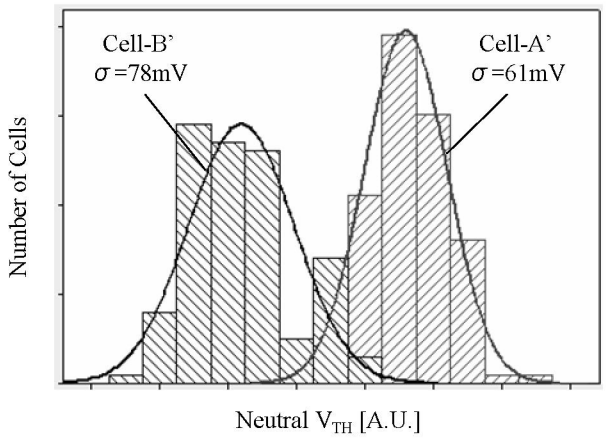


Figure 7. Simulated distributions of intrinsic neutral V_{TH} plotted from 120 sets of random variables for cell transistors A' and B' shown in Fig.6.

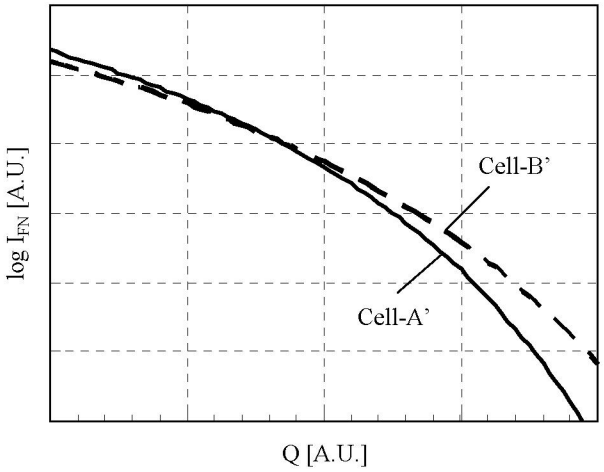


Figure 8. Example of simulated relationships between FG charge and F-N current in erase operation.

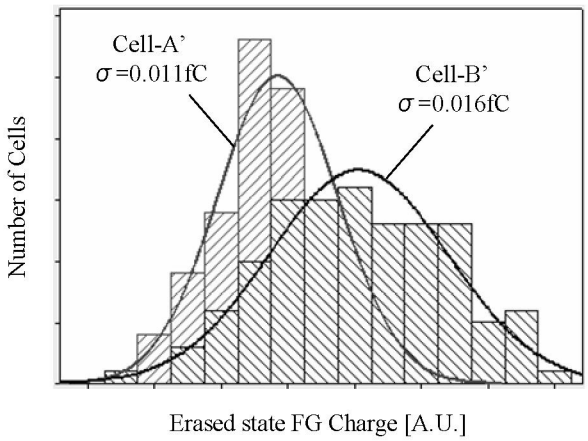


Figure 9. Simulated distributions of FG charge after 100ms erase operation.

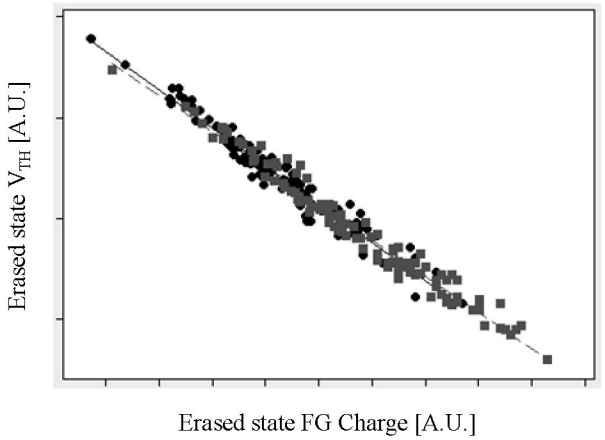


Figure 10. Simulated correlation between FG charge and V_{TH} of erased state. Circles and solid-line show calculated data points and their regression line of cell-A', respectively. Squares and dashed line shows calculated data points and their regression line of cell-B', respectively.

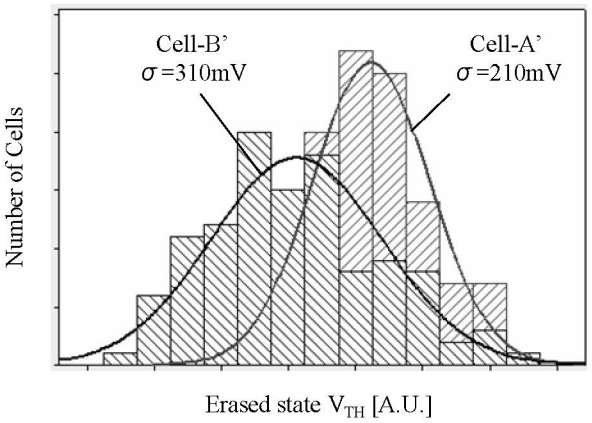


Figure 11. Simulated distributions of V_{TH} after 100ms erase operation.

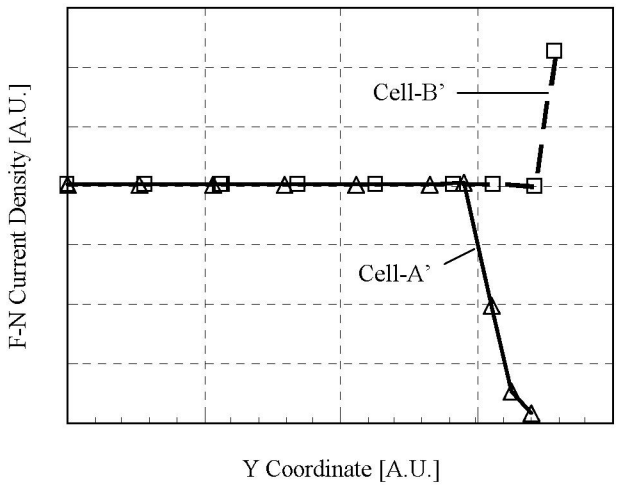


Figure 12. Simulated local F-N current density. Larger extra current flows near AA/STI boundary in cell-B'.