Multi-Layer Model for Stressor Film Deposition

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***Abstract*—Multi-layer simulation is proposed for accurate modeling of stressor film deposition. Multi-layer simulation subdivides a single deposition into a series of deposition and relaxation steps to emulate mechanical quasi-equilibrium during the physical deposition process. Only the multi-layer model is able to simultaneously match the experimental data on drive current vs. etch-stop layer stress, poly pitch, source/drain recess, and spacer stress.**

I. Introduction

Highly stressed nitride etch-stop layers (ESL) are widely used to increase deep submicron transistor performance [1]. Since transistor channel stress is difficult to measure, the ability to correctly predict stress transmittal from these films to the transistor channel is of vital importance for technology development and optimization [2]-[5].

In most commercially available process simulation tools, deposition operation is a mathematical abstraction, not a model describing the physical process. The equations of mechanics are usually solved after a material has been deposited. In many cases, this treatment is sufficient. However, certain phenomena occurring during deposition cannot be ignored, for example the evolution of stress in a conformal layer. In one typical method, stress in conformal layers is treated as a hydrostatic stress that is allowed to come to equilibrium with a free boundary at the surface of the conformal layer. The magnitude of the hydrostatic stress is determined by experimental measurement of biaxial stress on blanket (non-patterned) wafers, taking into account the Poisson effect. Our studies have clearly shown that a variety of experimental observations related to the impact of stress on transistor performance can only be explained by accounting for the quasi-equilibrium state of stress during deposition.

II. Model Description

In the proposed model, a single film deposition is subdivided into a series of deposition and "relaxation" steps to emulate mechanical equilibrium during the physical deposition process. At each step, a layer with the thickness of t/n is deposited, where t is the total film thickness and n is the number of the subdivisions. Intrinsic stress in each deposited layer is considered hydrostatic with constant magnitude. Stress relaxation occurs after the deposition of each layer.

III. Experimental and Simulation Results

The developed model was implemented in the Sentaurus Process simulator from Synopsys [6] and the ANSYS mechanical simulator [7]. Stress evolution during processing was simulated for typical transistor structures with 35nm gate length. Fig. 1 shows high resolution TEM images of such transistors with poly pitch (gate length plus distance between adjacent gates) varying from 0.26 μm to 1.04 μm. As seen, the 80nm-thick ESL films, covering the gates, are fairly conformal regardless of the pitch. Fig. 2 shows contours of lateral stress in a simulated structure after deposition of a nitride film with compressive intrinsic stress, simulated using the single and multi-layer models. In flat areas, both simulations give identical stress values in the nitride. However, stress distributions are very different near and around the gate. In the single-layer case, the conformal free surface is smooth and has fewer corners. Thus, the stress in the nitride is relatively uniform with one noted region of stress concentration located

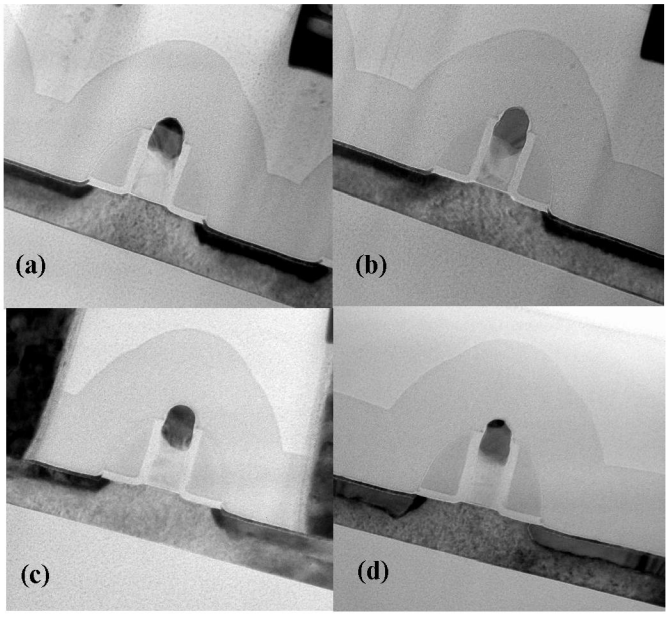

Figure 1. TEMs of 35nm gates with highly stressed ESL films as a function of gate poly pitch: (a) 0.26 μm, (b) 0.38 μm, (c) 0.63 μm, (d) 1.04 μm.

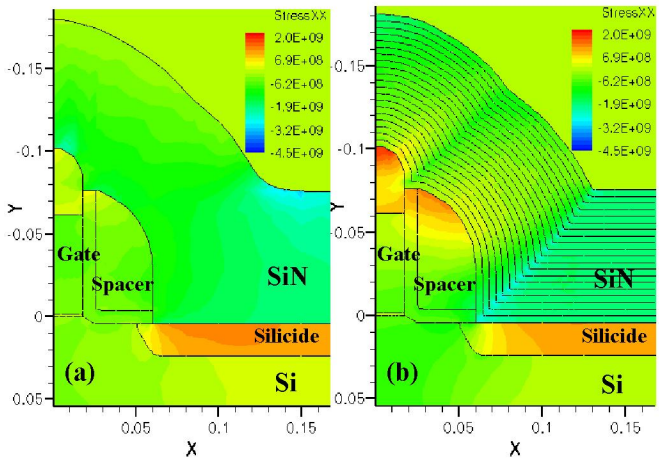

Figure 2. Contours of lateral stress (Pa) in a transistor structure simulated using (a) single-layer and (b) 20-layer deposition of 80nm nitride with compressive intrinsic stress.

at the surface of the nitride associated with the spacer/substrate corner. On the contrary, stress is much less uniform in the film simulated using the multi-step approach. The inner layers of the nitride film more closely follow the sharp contour of the gate structure, and the overall ESL shape better matches the TEM images shown in Fig. 1. Stress significantly increases in the areas where the layers sharply bend. This region of high compression extends diagonally from the film top to the spacer bottom. As a consequence, stresses in the spacer and the gate become very non-uniform as well, changing from tensile on top to compressive at the bottom, and the magnitude of compressive stress in silicon underneath the gate increases. Fig. 3 shows how simulated average stresses in the channel (lateral and vertical components) change with the number of layers. Lateral stress becomes more compressive and vertical stress becomes more tensile, both asymptotically approaching certain limits.

Channel stress simulations using the single and multi-layer models were performed for various nitride ESL films with intrinsic stress ranging from highly compressive to highly tensile. Using simulated average channel stresses as well as longitudinal and transverse piezoresistance coefficients obtained in 4-point bending experiments [8], changes in transistor drive current were calculated and compared to the measured transistor data [9]. Fig. 4 shows such a comparison. Despite drastic differences in channel stresses between the single and multi-layer deposition models, experimental drive currents could be matched with both models by changing vertical piezoresistance coefficients, which were not measured by the 4-point bending. They were considered adjustable parameters because the values reported for bulk silicon cannot be assumed to hold when there is a vertical confining field as in a MOSFET.

However, when the same piezoresistance coefficients were applied to simulations of certain geometry-related effects, experimental data could not be matched with the single-layer model, whereas the multi-layer model matched the experiments well. Fig. 5 shows simulated drive current of NMOS and PMOS transistors covered with a compressive ESL vs. poly pitch. When poly pitch decreases, the amount of ESL stressor between the gates decreases as well, and a reduction in its impact on channel stress is expected. The experimental results confirm this simple reasoning, and the multi-layer simulation matches the measured data well. At the same time, the single-layer model predicts that stress in the ESL near the gate is significantly relaxed at any pitch. As a result of this, channel stress and therefore drive current are almost independent of the poly pitch. Fig. 6 shows the dependence of transistor drive current on the recess or

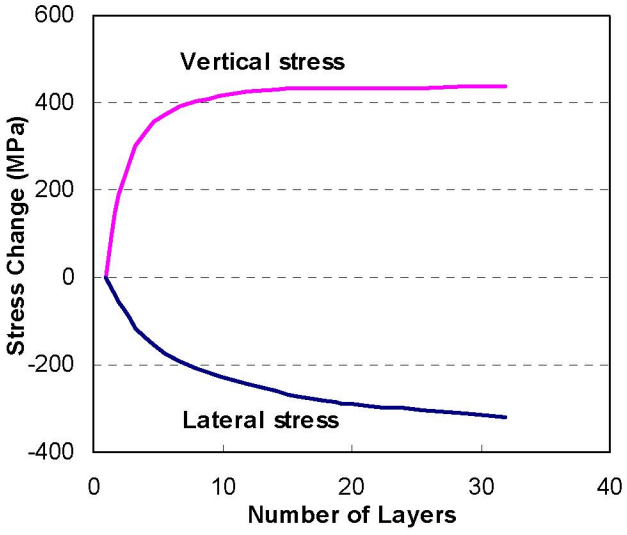

Figure 3. Simulated changes in average lateral and vertical channel stress vs. number of layers for a film with compressive intrinsic stress. Stresses were averaged along the channel at the depth of 1.5nm below silicon surface.

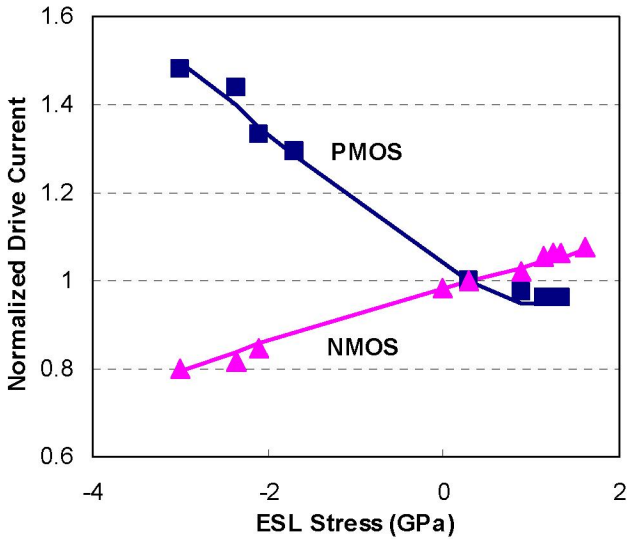

Figure 4. Normalized NMOS and PMOS drive current vs. ESL stress. Comparison of simulation (lines) to experiment (symbols).

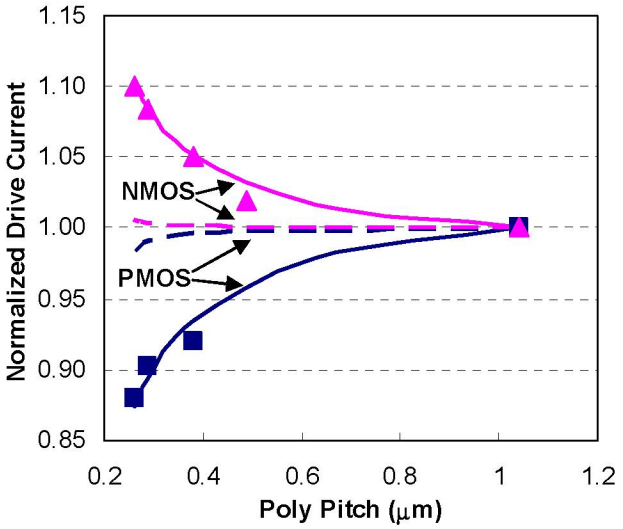

Figure 5. Experimental data (symbols), multi-layer (solid lines) and single-layer (dashed lines) simulation results on drive current vs. poly pitch for NMOS and PMOS with compressive ESL.

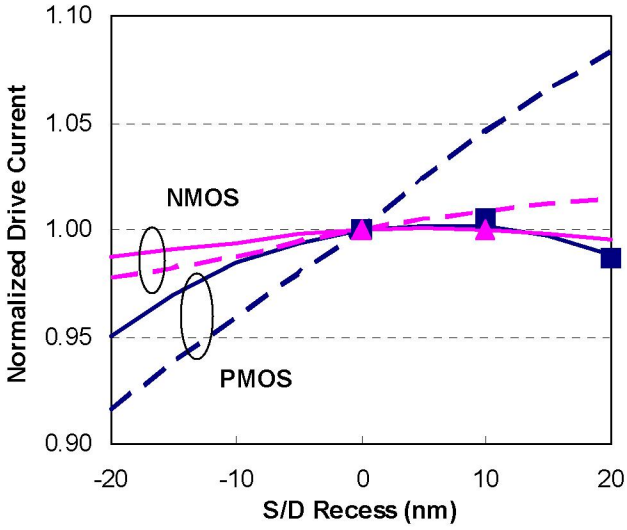

Figure 6. Multi-layer (solid lines) and single-layer (dashed lines) simulation results on NMOS (tensile ESL) and PMOS (compressive ESL) drive current vs. source/drain recess compared to experimental data (symbols).

elevation of the source/drain region. Based on the single-layer simulation, the recess is always beneficial for both NMOS and PMOS. The experimental results do not confirm this conclusion, but agree well with the multi-layer simulation. Fig. 7 shows contours of lateral stress in a simulated structure with the 20nm recess after deposition of a nitride film with compressive intrinsic stress, simulated using the single and multi-layer models. In the multi-layer case, the region of high compression in the nitride extends diagonally towards the bottom of the recess, causing significant vertical non-uniformity of stress in the channel and relative reduction in compressive stress at the channel surface. The single-layer simulation does not capture this phenomenon adequately.

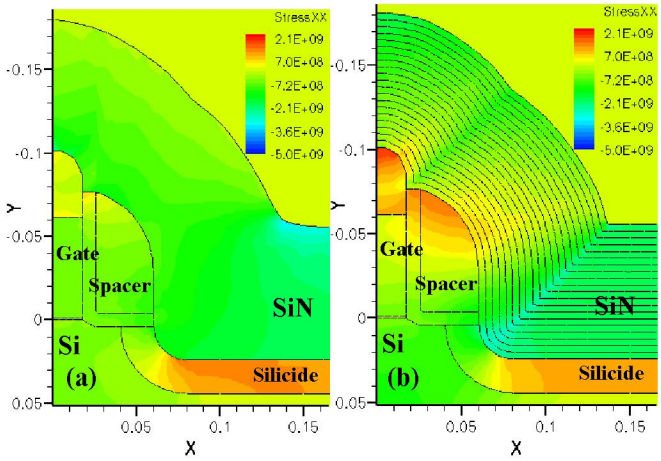

Figure 7. Contours of lateral stress (Pa) in 35nm transistor structures with 20nm source/drain recess simulated using (a) single-layer and (b) 20-layer deposition of nitride with compressive intrinsic stress.

The multi-layer model can be successfully applied to simulating the deposition of stressed films other than ESL, for example spacer. Due to proximity to the gate and despite stress relaxation after spacer etch, stress distribution in the deposited spacer film has a significant impact on channel stress. Fig. 8 shows experimental and simulated transistor drive current vs. spacer stress. As seen, the multi-layer simulation matches the measured data reasonably well, whereas the single-layer simulation predicts a completely different behavior. In the latter case, a more tensile spacer makes lateral channel stress more compressive, which leads to NMOS degradation and PMOS enhancement. With the multi-layer model, the stress trend is opposite. A more tensile spacer increases lateral channel stress. Consequently, NMOS is enhanced and PMOS is degraded, in agreement with experiment.

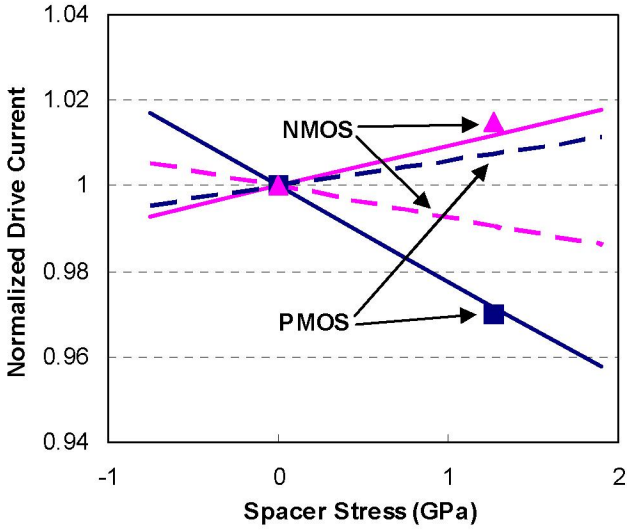

Figure 8. Experimental data (symbols), multi-layer (solid lines) and single-layer (dashed lines) simulation results on NMOS (tensile ESL) and PMOS (compressive ESL) drive current vs. spacer stress.

IV. Conclusions

Convincing evidence has been developed that multi-layer simulation is required for accurate modeling of stressor films. In this work, we compared the multi-layer and single-layer film deposition models using experimental data on drive current enhancement vs. ESL stress, poly pitch, source/drain recess, and spacer stress. We show that only the multi-layer model is able to match all the experimental data.

Acknowledgment

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