Stress Sensitivity of PMOSFET Under High Mechanical Stress

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Abstract—**Using PMOSFETs with a range of built-in process induced stress and four-point bending characterization, we present evidence that the stress response of PMOSFETs increases with channel stress. A novel method incorporating the characterization data with channel stress simulation has been developed which shows excellent agreement between our prediction and measured transistor performance data for nitride etch stop layer splits. Our analysis indicates that PMOSFETs will continue to show increasingly effective performance enhancement at higher channel stress.**

Keywords-stress sensitivity; high mechanical stress; modeling stress response; four-point bending

I. INTRODUCTION

Channel stress engineering is being actively pursued to improve transistor performance and maintain transistor scaling roadmap [1]. Since transistor channel stress is difficult to measure, accurate simulation of device channel stress and coupling of that stress to predictive capability for transistor electrical performance is essential in developing next generation transistor. Device predictive capability using bulk piezoresistance [2] response without considering the magnitude of built-in stress in the devices and surface confinement field was acceptable for capturing stress dependent behavior [3]. However, the stress sensitivity of devices with high built-in stress and under strong confinement field differs from bulk silicon piezoresistance behavior, requiring stress sensitivity measurements for applicable manufactured devices and operating conditions. Scalability beyond current stressor levels will depend on whether device stress sensitivity increases or decreases with increasing built-in process induced channel stress. Incorporating this stress sensitivity variability with increasing channel stress in device simulations is important for accurate prediction of transistor performance. We present data to support this stress sensitivity variability for PMOSFET and propose an exponential model to be used in device simulations including stress-dependent mobility effects.

II. EXPERIMENT AND SIMULATIONS

The MOSFETs used in this study were fabricated using a 65nm high performance SOI technology [4]. The MOSFETs have received five types of nitride etch stop layers (ESL) resulting in varying range of built-in channel stresses. The ESL stressors have film stress (splits A, B, C, D and E) in the ratio +1:-6:-7:-8:-10 relative to split A, where +/- indicate tensile/compressive films. The built-in channel stress in the MOSFETs, which originated from the ESL, is determined through simulations using internally developed multilayer deposition scheme in Synopsys' Sentaurus Process Simulator [5, 6]. In this simulation a real physical process is emulated by dividing the film deposition into several steps. At each step, a thin layer of nitride is deposited with hydrostatic intrinsic stress of constant magnitude. The mechanical equations are solved after the deposition of every layer allowing the hydrostatic stress to relax in order to bring the deposited layer to equilibrium with a free boundary surface. Four-point bend measurements have been performed on wafer samples from splits A and E. The four-point bend technique is widely used to determine the stress sensitivity of devices by adding differential mechanical stress to the existing built-in stress [7, 8]. These measurements coupled with the stress simulations are used to infer the inline performance enhancement measured in splits B, C, D and E relative to A.

III. RESULTS AND DISCUSSION

Fig.1 shows linear and saturation current enhancement measured for short channel (L_poly = 35nm) PMOSFET under uniaxial applied stress in the lateral and transverse direction for sample A. The stress sensitivity is defined as

$$\kappa = \frac{1}{I}\frac{dI}{d\sigma}, \qquad (1)$$

where, I is the current and σ is the stress in the channel. Under bending measurements the added stress in the channel is uniaxial when the device under test is at the center of the sample. Fig.2 shows the stress sensitivity (κ) for samples A and E. It shows that the lateral stress sensitivity ($\kappa_{\parallel}$) is higher for split-E, which received higher film stress. For transverse stress the stress sensitivity ($\kappa_{\perp}$) is effectively the same for samples A and E. A similar observation is also made on long channel devices. As shown in Fig.3, the built-in average lateral channel stress in split E is much higher than that in split A [5].

By contrast, the built-in average transverse channel stress in split E is only slightly higher than split A. In long channels the channel stress in split E is generally higher than split A, but have reduced magnitudes compared to short channels. These results suggest that the stress sensitivity $\kappa_{\parallel}$ and $\kappa_{\perp}$ are sensitive to the magnitude of built-in channel stress.

The short channel devices exhibit lower sensitivity in both lateral and transverse directions compared to long channels. To understand the cause we have measured Idlin-$\kappa_{\parallel}$ and Idsat-$\kappa_{\parallel}$ as determined from linear and saturation current for a range of gate lengths. We found that Idlin-$\kappa_{\parallel}$ decreases when channel length decreases (see Fig.4) suggesting a series resistance effect [8, 9]. Device simulations using DESSIS (Synopsis's Device Simulator) reveal that when the low-field mobility is increased by an amount equal to linear current enhancement obtained for long channel, a reduced linear current enhancement is observed for short channels (see Fig.4); also indicating the series resistance effect. A similar trend is observed when the saturation current is measured (Fig.5). However, in this case, the reduced stress response for short channels is related to the weak effect of stress on high energy carriers. To account for the stress induced change in the device simulations, only the low-field mobility is taken as a function of stress.

Assuming a linear dependence of κ on built-in stress (see Fig.2) we can write Eqn.1 for a uniaxial channel stress case as

$$\ln\left(\frac{I(\sigma)}{I(\sigma_0)}\right) = \frac{1}{2}\alpha(\sigma^2 - \sigma_0^2) + \beta(\sigma - \sigma_0) \qquad (2)$$

Where, α and β represent the slope and intercept of the curves in Fig.2. Equation 2 predicts an exponential drive current enhancement with channel stress similar to the trend predicted in [10, 11]. This leads to the expectation that PMOSFET will continue to show increased performance enhancement even at higher channel stress. When the stress in the channel is not uniaxial, we assume the total enhancement to be linear combination of the enhancement due to lateral, transverse and vertical stress. Based on this assumption and using the channel stress determined through simulations [5], we have calculated current enhancement of samples B, C, D and E relative to A. These results are then compared with inline measured data (see Fig.6). We found that when the vertical sensitivity is ignored our calculation is shy of matching the measured data. However, when small vertical stress sensitivity equal to 0.3% per 100MPa is assumed we find excellent agreement between our calculation and the measured data. The vertical sensitivity determined here is close to the bulk piezoresistance value [2].

We have also investigated the dependence of the stress sensitivity on vertical field. We found that the lateral stress sensitivity increases with surface confinement field (Fig.7). This is expected as the light-hole to heavy-hole band splitting increases with surface confinement under uniaxial stress [12]. In transverse stress (see Fig.7) an interesting result is observed. The stress sensitivity increases at lower field (<0.7MV/cm) and then declines for higher fields (>0.7 MPa).

IV. CONCLUSION

We have presented evidence to show that the stress sensitivity of holes is an increasing function of stress in the stress range investigated. A novel method is also presented to predict PMOSFETs performance enhancement using wafer bending measurements as parameters. As such the performance enhancement of PMOSFETs is expected to increase in the absence of stress and process induced defects.

ACKNOLEDGEMENT

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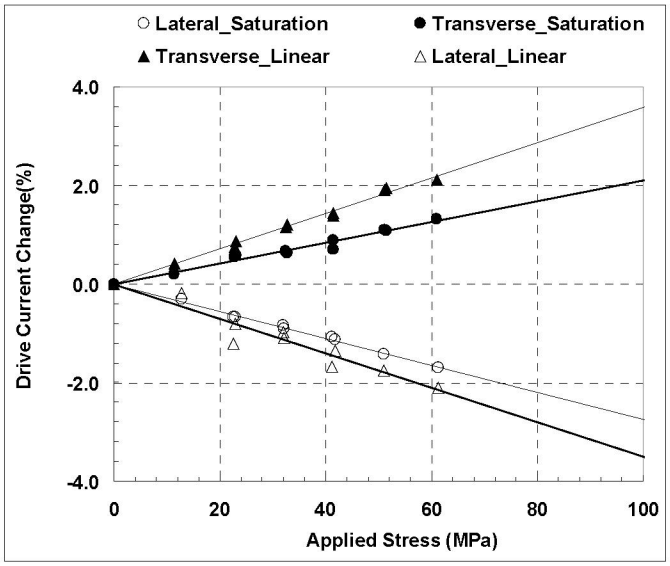

Figure 1: Drive current changes under tensile stress. Lateral stress (open symbols) show degradation and transverse stress (solid symbols) show enhancement. The linear and saturation currents were measured at Vgate=-1.2V, Vdrain=-0.05 and Vgate=Vdrain=-1.2V respectively.

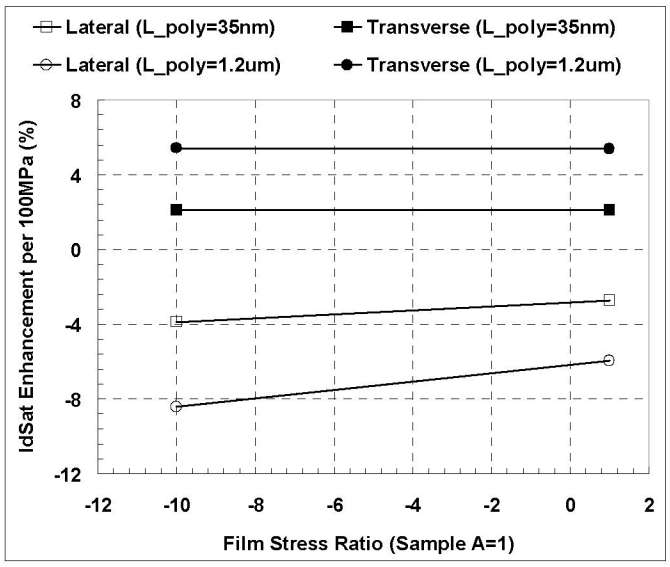

Figure 2: Changes in stress sensitivity. Lateral stress sensitivity increases with film stress (open symbols). Transverse stress sensitivity showed no changes with film (solid symbols).

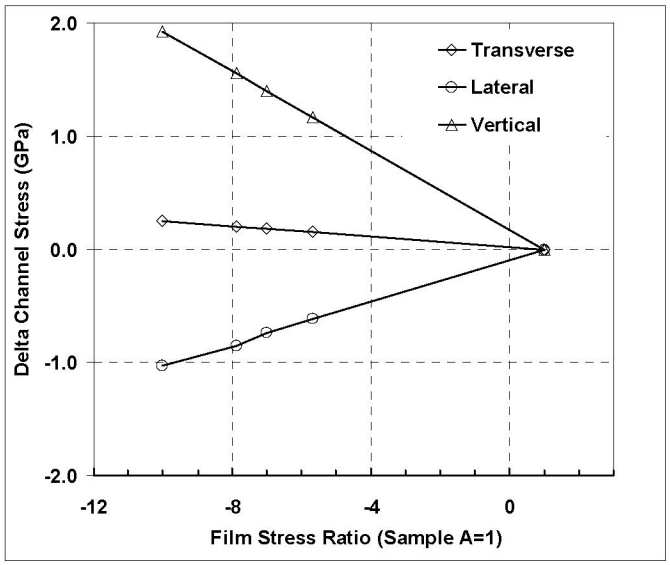

Figure 3: Delta average channel stress determined from simulations for L_poly=35nm. Lateral stress in split E is much higher than split A, however the transverse stress in E is comparable to A.

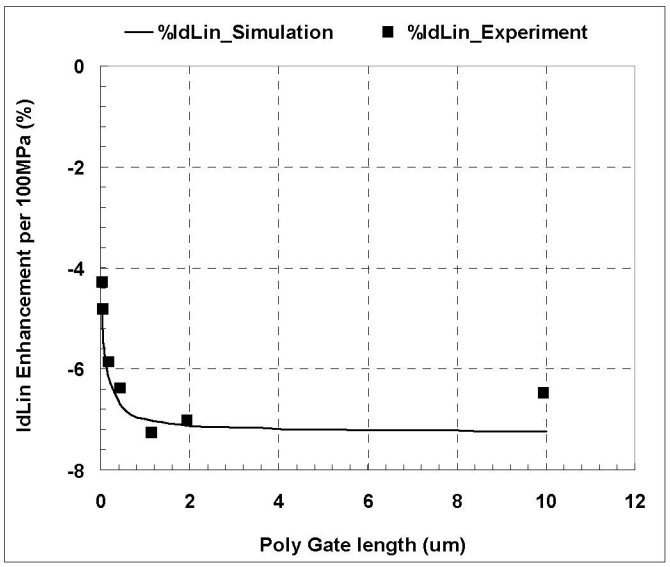

Figure 4: Linear current stress sensitivity changes with channel length. Symbols are experiment and solid line is simulation results.

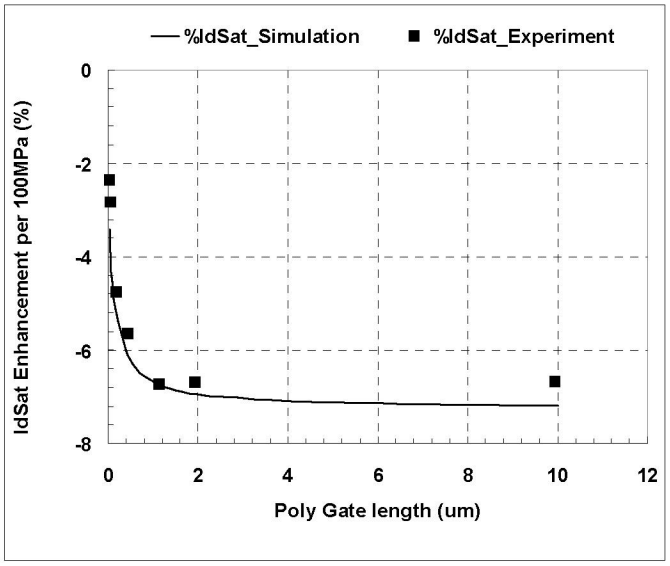

Figure 5: Saturation current stress sensitivity changes with channel length. Symbols are experiment and solid line is simulation results.

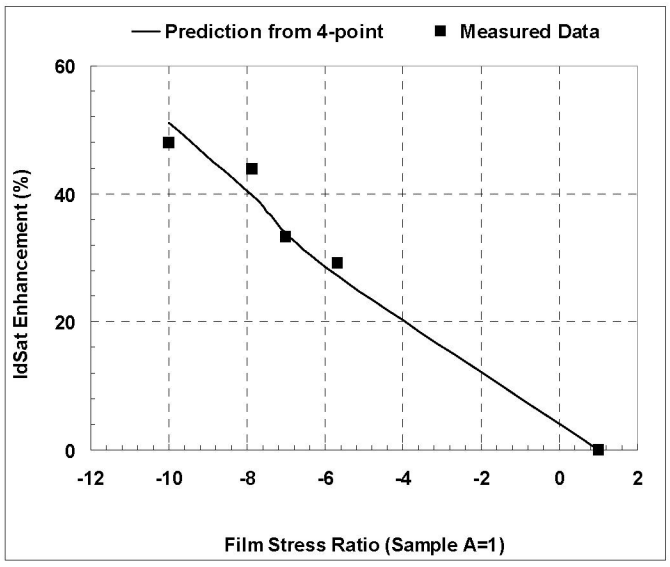

Figure 6: Calculated current enhancement (line) using Eqn. 2 and inline measured data (symbol).

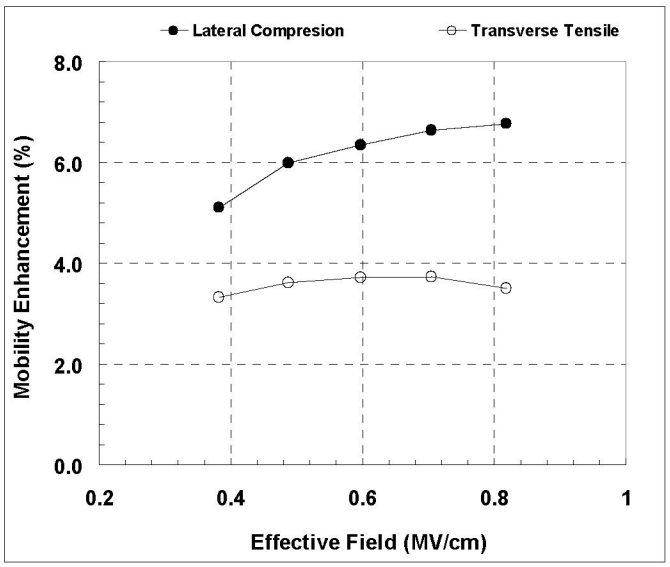

Figure 7: Surface confinement dependence of stress sensitivity. Lateral sensitivity increases with field. Transverse stress sensitivity peaks at Eeff ~ 0.7MV/cm.