Device Simulation of Random Dopant Effects in Ultra-small MOSFETs Based on Advanced Physical Models

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***Abstract*— We discuss random dopant effects in ultra-small MOSFETs associated with quantum confinement effects and contact resistances, along with the separation of impurity number fluctuations and position fluctuations. The contribution ratio of the effect of the channel impurity position fluctuation to the total threshold voltage fluctuation almost reaches 75 %, which indicates the importance of controlling the impurity diffusion process in the scaled MOSFETs. Fluctuations of electron distribution confined in the inversion layer lead to an increase in threshold voltage deviations as compared to the classical simulation. On the other hand, since the potential fluctuations around the Schottky barriers are not so sensitive to random dopant effects, the standard deviation of threshold voltage with contact resistances becomes lower. As we show, random dopant effects have various physical aspects in terms of device characteristics, and therefore, physical models concerning random dopant effects should be appropriately chosen and taken into consideration for correct device simulation.**

I. Introduction

Fluctuations of the device characteristics induced by random dopant effects become serious reliability issue in ultra-small MOSFETs [1-3]. As long as impurities are used as space charges controlling the electric properties of MOSFETs, random dopant effects on device characteristic fluctuations in various physical situations should be considered. In this paper, we construct advanced device simulation models to predict variation of device characteristics associated with random dopant effects in ultra-small MOSFETs. The simulation models are illustrated using MOSFETs with only impurity position fluctuations, with quantum effects, and with contact resistances. Throughout this study, random numbers generate atomistic impurity profiles; the Poisson random number determines the number of impurity contained in each control volume and the uniform random number determines their position in the volume. Random dopant effects in all semiconductor domains, including poly-Si gate region, are taken into consideration. In addition, basically, only the long-range parts of Coulomb potential of impurities are incorporated in the Poisson solver of our simulator so as to avoid unphysical capture of majority carriers around impurity atom [4].

II. Separation of Impurity Number Fluctuations and Position Fluctuations

Random dopant fluctuations consist of two factors. One is their number fluctuations, and the other is their position fluctuations. Understanding how these two factors contribute to the fluctuations of device characteristics helps us designing the effective impurity introduction process. The separation of effects of impurity number fluctuations and position fluctuations on threshold voltage (*Vth*) fluctuation in scaled transistors was studied in [5], but using mainly 2D simulators in which impurity distribution along the gate width direction is not able to be handled. However, in ultra-small MOSFETs, drain-current-path formations determining *Vth* are closely related to "blocking" impurity distributions in the channel along the gate width direction [3], clearly, 3D simulation is indispensable. In order to separate the effects of impurity number fluctuations and position fluctuations on device characteristics fluctuations, we implemented fixed-impurity-number analysis model in our in-house 3D device simulator. In this model, first, fixed-number regions are determined in the semiconductor region. Next, the impurity number contained in the region is calculated by macroscopic impurity concentration times the volume of the region. Finally, the calculated impurity number in the region is fixed in each simulation sample and only the positions of impurities in the region are three-dimensionally fluctuated by uniform random number. The point charge of each impurity atom is assigned to the computational grids according to the long-range model [4]. Fig. 1 shows an example MOSFET structure we used in this study. In this case, a fixed-number region is set in the channel (*x*:-11 nm to 11 nm, *y*: 0 nm to 20 nm, *z*:-38 nm to 0 nm). The number of impurity atoms in the region is found to be 50 (acceptor: 50, donor: 0). Fig. 2 shows the *Id-Vg* characteristics obtained by our three-dimensional classical drift-diffusion (DD) simulator for up to 100 statistical MOSFET samples in which both the number and the position of impurities are fluctuated. Fig. 3 shows the corresponding *Id-Vg* curves for samples in which only the position of impurities are fluctuated. The standard deviations of *Vth* (σVth) in Figs. 2 and 3 are 70.0 mV and 60.5 mV, respectively, it shows the contribution ratio of the effect of

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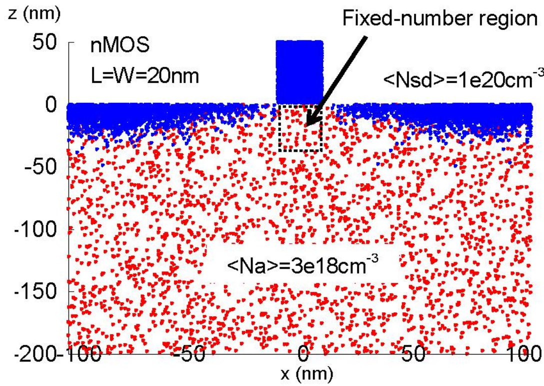

Fig. 1: Cross-sectional view of impurity atom position at the middle of gate width. The number of impurities under the gate electrode is fixed as the number determined by the macroscopic impurity concentration times the volume of region; in this case, the expected number of acceptors is 50. In that region, only the positions of those acceptors are to be fluctuated by uniform random number.

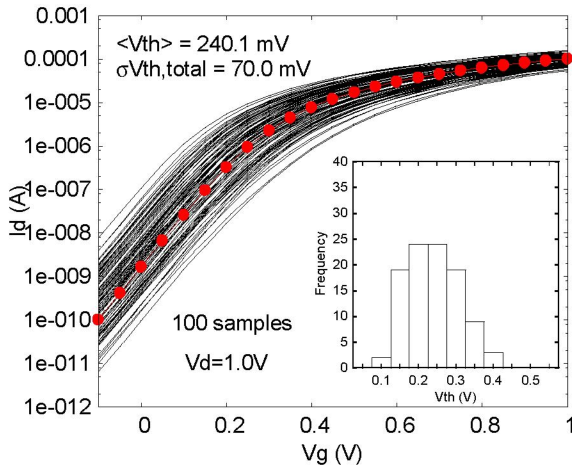

Fig. 2: *Id-Vg* characteristics of MOSFETs in which both the number and the position of channel impurities are fluctuated. Red solid circles mean the sample without random dopants. Threshold voltage *Vth* is defined as the gate voltage at which *Id* reaches 1μA.

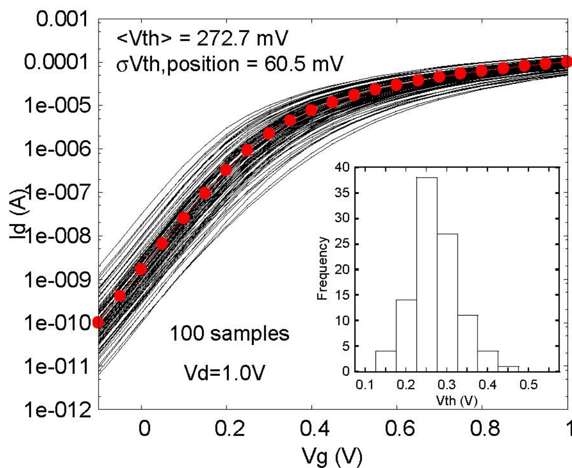

Fig. 3: *Id-Vg* characteristics of MOSFETs in which only the positions of channel impurities are fluctuated.

impurity position fluctuation to the total *Vth* fluctuation defined in [5], $R = (\sigma Vth,position/\sigma Vth,total)^2$, almost reaches 75 %. This result reflects that more elaborate annealing process is needed for suppressing σ*Vth* in ultra-scaled MOSFETs. However, seen from another standpoint, it can be said that fixed-impurity-number MOSFETs contribute to a 14 % reduction of σ*Vth*. This implies that strict control of channel impurity dose is beneficial in terms of the reduction of σ*Vth*, as is experimentally proved for the reduction of conductance fluctuation using the "single ion implantation" technique [6].

III. IMPURITY FLUCTUATIONS WITH ELECTRON QUANTIZATION EFFECT

In line with the downscaling of MOSFETs, the increase in channel dose concentration as a punch-through stopper in the substrate results in a large surface electric field and strong electron quantization. For this situation, classical DD simulations are probably inappropriate but quantum DD (QDD) simulations capable of handling quantum state fluctuations of confined electrons are needed [7]. We would like to stress that, in contrast to the previous density-gradient simulation study [8], our simulator incorporates only the long-range parts of Coulomb potential (QDD long-range), and thus, a smooth potential around a point charge is guaranteed and no artificial capture of majority carrier occurs. Furthermore, this treatment assures good convergence when its CPU consumption time per sample is compared with QDD "bare" model, in which both the short- and long-range parts of Coulomb potential of impurities are incorporated (Table I). The averages of *Vth* (<*Vth*>) and σ*Vth* are also summarized in Table I together with the values for the classical DD case (DD long-range). Threshold voltage *Vth* in this study is defined as the gate voltage at which *Id* reaches 1μA. Inversion layer thickness in QDD causes thicker EOT than in classical DD, and consequently, the gate controllability in QDD becomes weaker. It strengthens short channel effects, and therefore, in ultra-small MOSFETs, the <*Vth*> in QDD is slightly smaller than that in the classical DD case. The electron distributions perpendicular to the substrate in Fig. 4 infer that the fluctuations in average position and concentration of electron due to random dopant effects lead to the fluctuations in the inversion layer capacitance. Consequently, it causes additional σ*Vth* factor in the density gradient studies compared with the classical DD case as seen in Table I.

TABLE I

Comparison between the results of two QDD models with that of the classical DD model. Threshold voltage *Vth* is defined as the gate voltage at which *Id* reaches 1μA. Inversion layer thickness in QDD causes thicker EOT than in classical DD, and consequently, the gate controllability in QDD becomes weaker. It strengthens short channel effects, and therefore, in ultra-small MOSFETs, the average *Vth* (<*Vth*>) in QDD is slightly smaller than that in the classical DD case.

	<Vth>(mV)	σVth(mV)	<CPUtime/sample>(sec) †
QDD long-range	212.4	88.4	65,426
QDD bare	228.4	85.4	76,913
DD long-range	236.7	75.5	3,846

† sun4u Ultra-SparcIII 1280MHz

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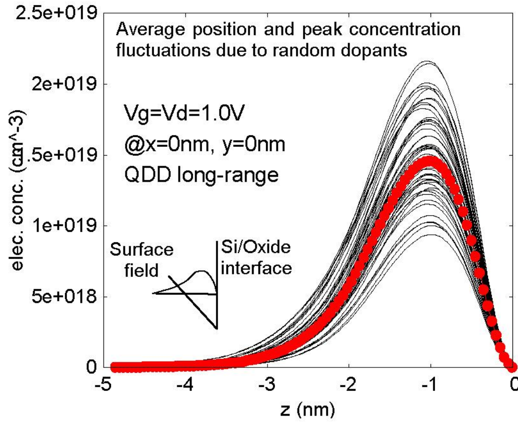

Fig. 4: Fluctuations of confined electron distribution along the depth direction of the substrate due to random dopant effects. In this study, electron penetration into the gate oxide region is not taken into account.

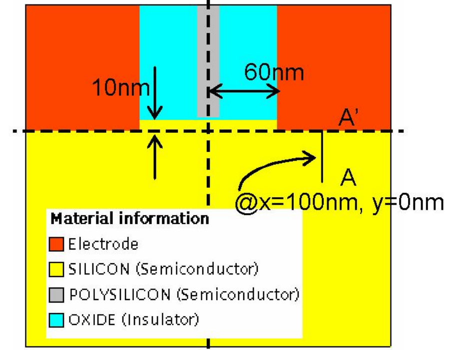

Fig. 5: Simulated structure used for the contact resistance simulation. Source and drain electrodes are buried 10nm from the surface and assumed to be the material which makes Schottky barrier heights of 0.65eV between Si substrate.

IV. Source/Drain Impurity Fluctuations Around Contacts

Until this point, we have restricted our discussion to channel impurity fluctuations, that is, channel resistance fluctuations. However, as MOSFETs are shrinking, increasing understanding of the fluctuation of the parasitic resistance such as the contact resistance is needed. We have already confirmed the simulation method of random-dopant-induced contact resistance fluctuations in Schottky diode structures [9]. In the paper, we showed that the Poisson solver with only the long-range component of impurities could provide stable simulations for contact resistance fluctuations, in terms of suppressing mesh dependencies and extreme local conduction. In this study, we extend the method to MOSFET structures with $L = W = 20$ nm, $tox = 1.4$ nm (Figs. 5 and 6). Simulated MOSFETs form Schottky barrier heights of 0.65eV between S/D electrodes and Si substrates, that is, almost corresponding to $Si/NiSi_2$ or $Si/CoSi_2$ silicide contact system. Changing random number seed, we calculated *Id*-*Vg* characteristics up to 100 samples (Fig. 7). Comparing the drain currents at $Vd = 1.0$ V of the same random number seed sample between the MOSFETs with ohmic contact and those with Schottky contact, the fluctuations in the contact resistance are extracted and summarized as a histogram (Fig. 8). Physically, contact resistance fluctuations come from potential modulations around Schottky barriers due to random dopant effects of S/D impurities, because currents tunneling through these barriers determine *Id* as well as currents thermally overcoming these barriers (Fig. 9). The σVth of MOSFETs with Schottky contact (DD Schottky) and that of MOSFETs with ohmic contact (DD ohmic; i.e. zero contact resistance) are compared in Fig. 10. It is found that σVth with Schottky contact is lower than σVth with ohmic contact. The reason is that Schottky contact resistance (*Rc*) has large average and smaller relative error than the channel-S/D series resistance (*Rser*), for example, the relative error $\sigma Rc/\langle Rc\rangle$ is 0.23, whereas, in contrast, $\sigma Rser/\langle Rser\rangle$ is 1.07 near the threshold. Drain currents of the MOSFETs with Schottky contact are less sensitive to random dopant effects than those with ohmic contact, hence σVth becomes lower.

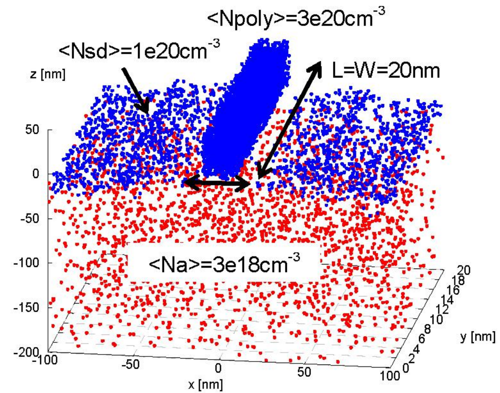

Fig. 6: Generated 3-dimensional impurity profile according to the Poisson and uniform random number. Atomicity of the entire semiconductor regions including poly-Si gate is considered. *Xj*s of S/D extension and deep S/D, usually assumed to be extremely shallow in previous studies, are set as 15 and 30 nm, respectively, in our simulation.

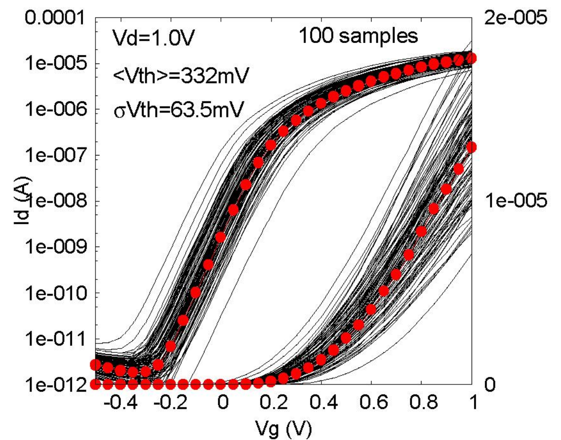

Fig. 7: *Id*-*Vd* characteristics of MOSFETs with Schottky contact resistance. Red solid circles mean the sample without random dopant fluctuations. Threshold voltage *Vth* is defined as the gate voltage at which *Id* reaches 1μA.

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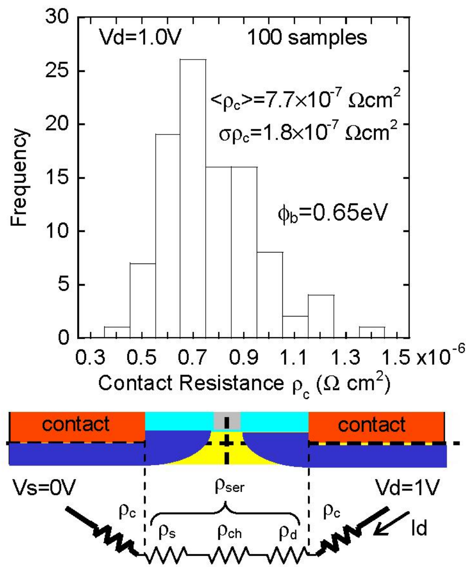

Fig. 8: Histogram of Schottky contact resistance ρ_c.

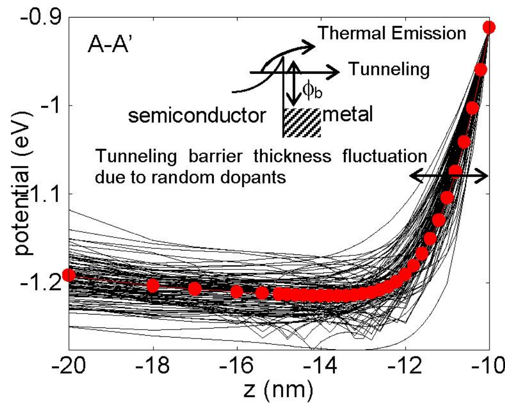

Fig. 9: Schottky barrier fluctuations due to random dopants along the A-A' direction in Fig. 5. These barrier fluctuations bring about tunneling current fluctuations as well as thermal emission current fluctuations across the Schottky contact barrier, causing fluctuations in *Id*.

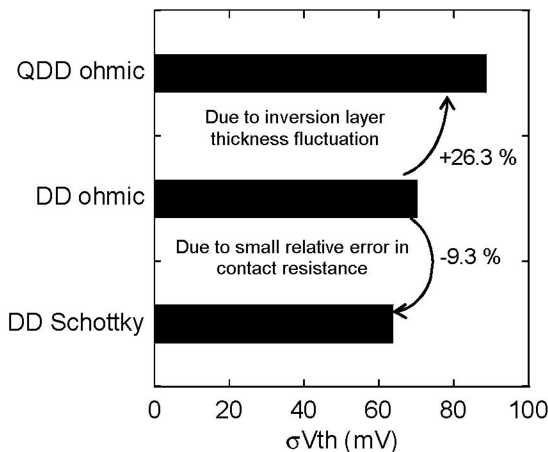

Fig. 10: Standard deviations of *Vth* of the same device structure in various simulation models. Notice here that, in all simulated cases, only the long-range parts of Coulomb potential of impurities are incorporated in the Poisson solver.

V. Summary

In summary, we discussed random dopant problems in ultra-small MOSFETs associated with quantum confinement effects and contact resistances, along with the separation of impurity number fluctuations and position fluctuations. The contribution ratio of the effect of the channel impurity position fluctuation to the total threshold voltage fluctuation almost reaches 75 %, which indicates the importance of controlling the impurity diffusion process in the scaled MOSFETs. Fluctuations of electron distribution confined in the inversion layer lead to an increase in threshold voltage deviations as compared to the classical drift-diffusion simulation. On the other hand, since Schottky contact resistance has large average and small relative error, the standard deviation of threshold voltage with contact resistance becomes lower than that with zero contact resistance.

Acknowledgment

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