Investigation of SNM with Random Dopant Fluctuations for FD SGSOI and FinFET 6T SOI SRAM Cell by Three-dimensional Device Simulation

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***Abstract*— As CMOS technology is dramatically scaled down in recent years, the operation of SRAM becomes one of critical issues for further scaling. In this paper, we have focused on both FD SGSOI and DG (FinFET) devices because of the scaling capabilities, and we have simulated SRAM SNM with discrete dopant fluctuations in the channel regions by 3D simulation. As for SNM, FinFET is a promising candidate up to 32nm node, but for 22nm node, it will be difficult to operate even a FinFET with stability. As for fluctuations, the total number of dopant in channel depletion layer is a key factor. The fluctuations of SNM in FinFET are reduced by balancing fin thickness and dopant density in the channel.**

Keywords-component; FinFET; FDSOI; SRAM; Static Noise Margin; fluctuation; scaling; 3D simulation; TCAD

I. INTRODUCTION

As CMOS technology is dramatically scaled down in recent years, the operation of SRAM becomes one of critical issues for further scaling. The gate length for high performance operation is predicted to be 9 nm in 2016 [1]. It is important for reliability to keep static noise margin (SNM) large enough to overcome random dopant fluctuations. Recently, in addition to bulk SRAM transistors, novel SRAM structures such as single gate (SG) SOI and double gate (DG) device (FinFET) are frequently reported and discussed. SGSOI and FinFET transistors are very strong for short channel effect and have excellent scalability. In addition, its performance becomes enough to be used for industry production [2, 3, 4, 5].

In this paper, we have focused on both FD SGSOI and DG (FinFET) devices because of the scaling capabilities, and we have simulated SRAM SNM with discrete dopant fluctuations in the channel regions by 3D simulation. We will also show the perspective for scaling in the future.

II. SIMULATION METHOD

Fig.1 shows simulated 6T FinFET SRAM cell structure. It was constructed with the combination of 3D process emulator and 3D device simulator.

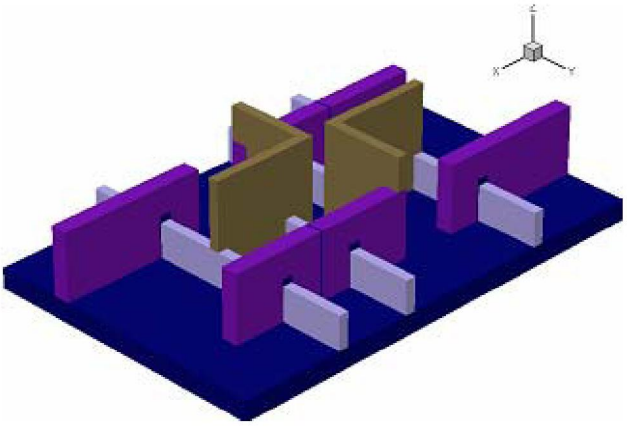

Figure 1. Simulated 6T SOI SRAM structure. This structure is calculated.

SRAM characteristic was calculated by coupling Poisson equation and electron and hole continuity equations. We calculated whole this cell layout structure. By this method, real circuit characteristics can be calculated directly, and we can get very accurate circuit characteristics. By recent computer performance improvement, the 3D simulator becomes very powerful tool for future perspectives. In this calculation, we considered 45nm, 32nm and 22nm technology nodes, and the calculation parameters are listed in Table 1.

TABLE I. CALCULATION PARAMETERS. WE FOCUSED 3 TECHNOLOGY NODES (45, 32, 22NM).

Technology Node	45	32	22
Scaling Ratio	1	0.71	0.69
DRAM Pitch	45	32	22
Lsd	40	28	20
Lg	25	18	13
Lov	3	2.5	2
TfinN	15	12	8
TfinP	15	12	8
Hfin	50	50	50
			Unit: μm
1 Fin Cell size (um^2)	0.2281	0.1473	0.06942
2 Fin Cell size (um^2)	0.3397	0.1742	0.08203
Area Penalty (%)	17.9	18.3	18.2

For the simulation of discrete dopant fluctuations in channel regions, we constructed the methodology shown in Fig. 2.

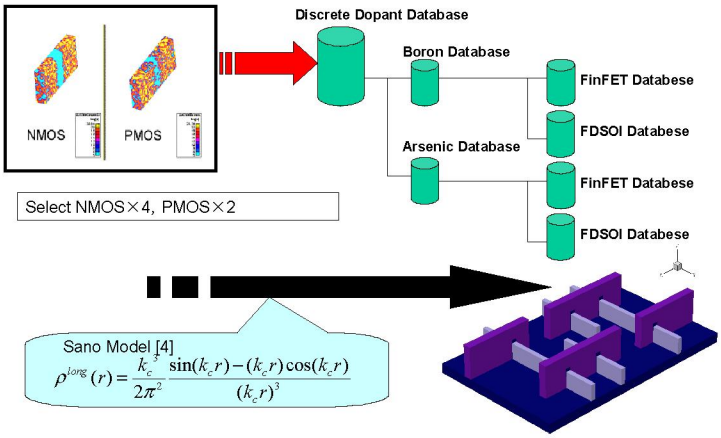

Figure 2. Simulation methodology including random dopant fluctuations in the 6T SRAM.

First of all, we calculate many pairs of NMOS and PMOS structures with random dopant distributions in the channel regions, and build an NMOS and PMOS database. Next, we pick up 4 NMOS and 2 PMOS pairs (for 6T SRAM Cell) from the database randomly. In this calculation, we distributed carrier charges by using Sano Model [6]. Finally we calculate SRAM characteristics for many cases. In Fig.3, we show the Boron distribution in the 6T SRAM, which is introduced by different dopant distribution. By calculating many cases, we can evaluate the fluctuation of SNM statistically.

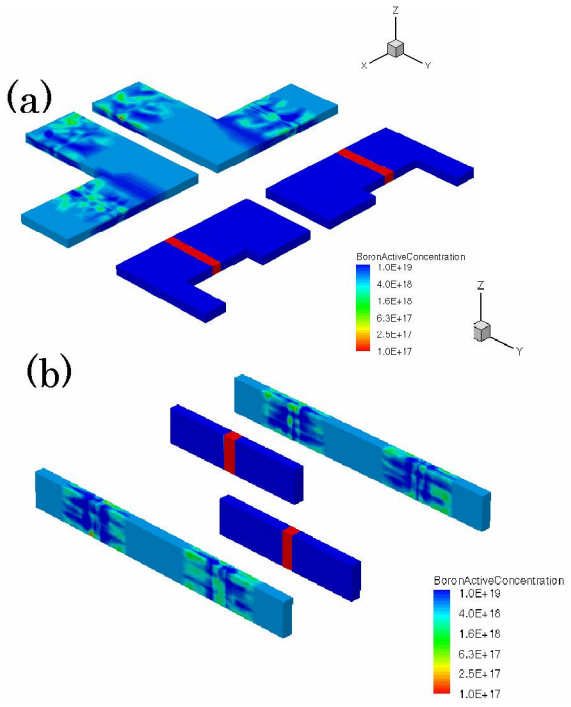

Figure 3. Boron distribution in the 6T SRAM.
(a) FD SG SOI (b) FinFET

III. Results and Discussions

In Fig.4, we show the butterfly curves of FinFET for each technology node. As scaled down, the area of margin window (SNM) becomes smaller, and it decreases dramatically especially in 22nm node.

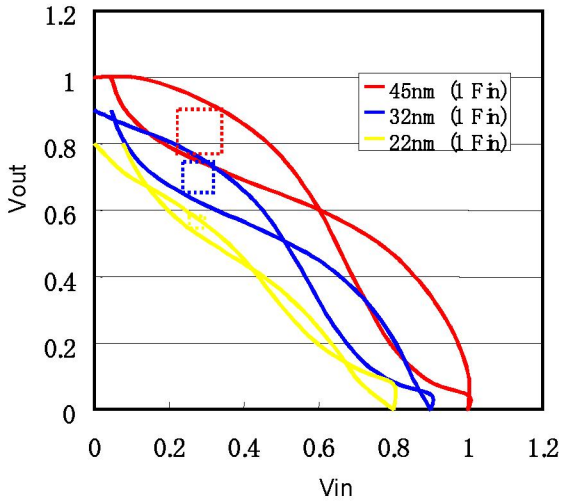

Figure 4. Butterfly curves of FinFET for each technology node.

In Fig.5, the comparison of SNM between FD SOI and FinFET is shown. For 45nm node, both SNMs are almost equal, but for 32nm node, SNM of FDSOI decreases. This is because in FDSOI, short channel effect can not be suppressed enough. For 22nm node, SNM of FinFET also decreases dramatically, and it will be difficult to operate SRAM circuits with stability even in FinFET.

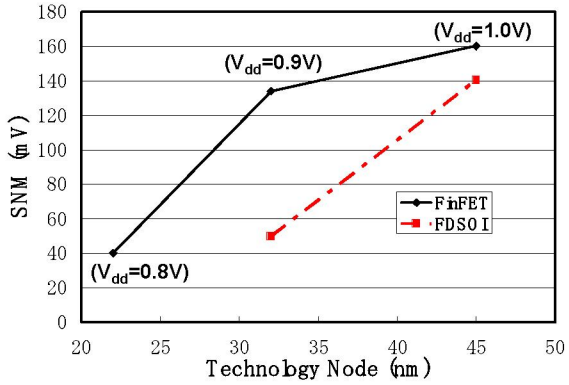

Figure 5. The comparison of SNM for FD SOI and FinFET (45nm node).

Some methods to improve SNM were proposed for FinFETs [7]. According to this method, we have improved β-ratio by increasing the number of fins at the driver NMOSs as shown in Fig.6. We show the butterfly curves for comparison in Fig.6. From this result, two-Fin SRAM improves SNM by about 30 % than one-Fin SRAM. But there is area trade-off because of added number of fins. This penalty is about 18%. As a result, it is very important for circuit designers to balance improvement of SNM and area penalty.

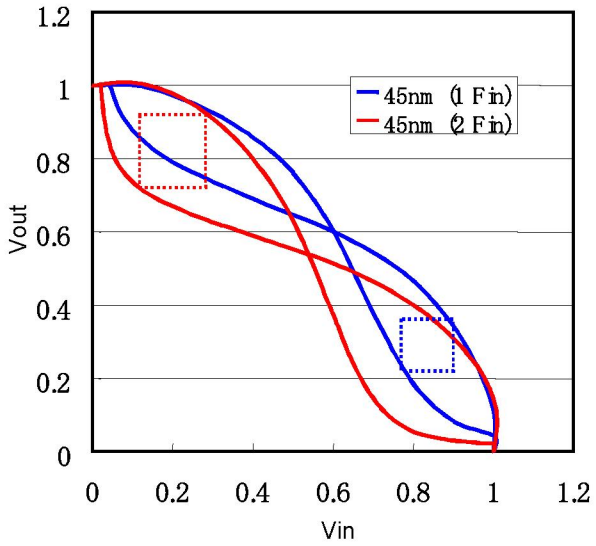

Figure 6. The butterfly curves of 1-Fin and 2-Fin 6T SRAM.

Next, we will discuss the fluctuations of SRAM SNM by random dopant fluctuation. As scaled down with increasing channel dopant density, the fluctuation of discrete dopant in channel becomes very important. In Fig.7, many butterfly curves with different channel distribution are shown. Fig.8 shows the fluctuations of SNM for FD SOI and FinFET at 45nm node. The SNM of FinFET is larger than that of FD SOI, but the fluctuation of FinFET is still smaller than that of FD SOI. These results indicate that FinFET will become the promising candidate for future device structure against both average of SNM and fluctuations. From discussions above, we will focus on FinFET in next session.

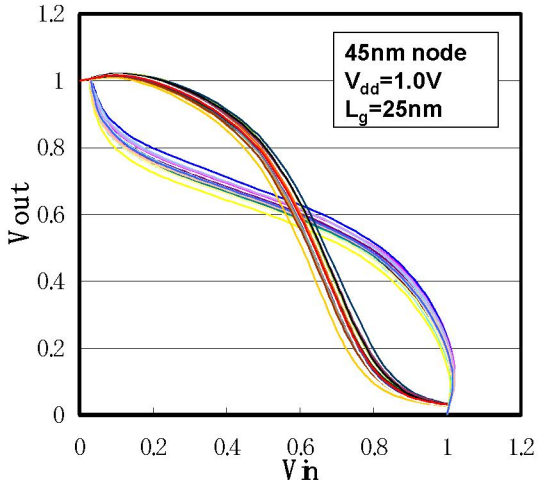

Figure 7. The butterfly curves with random dopant fluctuations for SNM in 6T FinFET SRAM circuit.

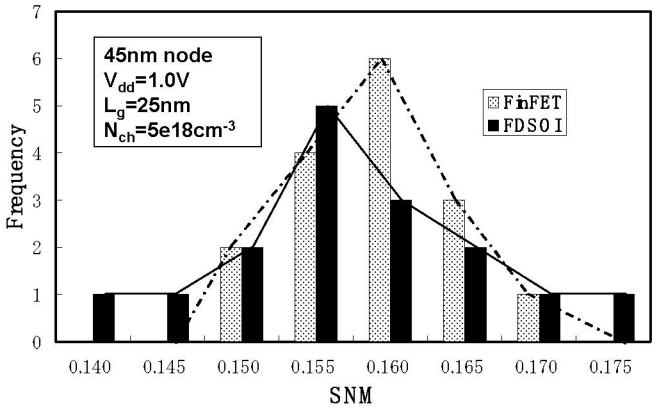

Figure 8. The comparison of SNM frequency distribution between FD SOI and FinFET. Sample number is 18.

It is very important to analyze the scalability of device for future perspectives. Fig.9 shows the fluctuations of SNM in FinFET SRAM for each technology node. Not only the average value of SNM but also the fluctuation decreases as scaled down.

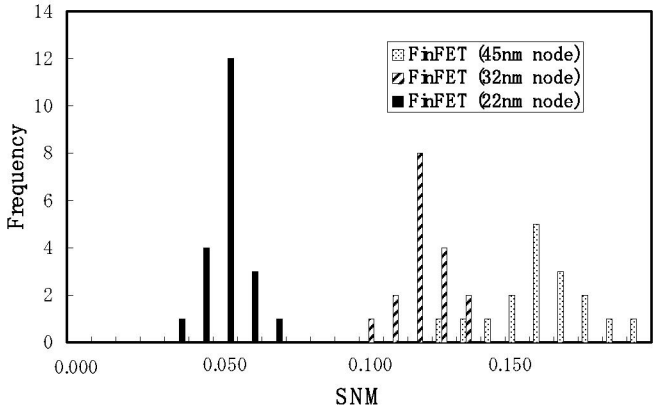

Figure 9. Frequency distribution of SNM as scaled down in FinFET. Sample number is 18.

As channel thickness of the fin becomes thinner and gate area also becomes smaller with scaling, we consider that the total number of dopant in channel depletion layer plays an important role in fluctuation. To clarify this relationship, we will show the total number of dopant in channel as a function of technology node in Fig.10. Because absolute value of dopant in channel decreases as scaled down, the fluctuations of SNM are also suppressed. This is because the volume of channel depletion layer is reduced more aggressively with scaling although dopant density in channel increased conventionally. This result suggests that the fluctuations of SNM can be reduced by using thinner fins even though dopant density in channel increased with scaling. Of course, intrinsic channel for fins is more effective in fluctuations than doping channel. In further scaled regime, these parameters in FinFET will become crucial for designing SRAM circuit.

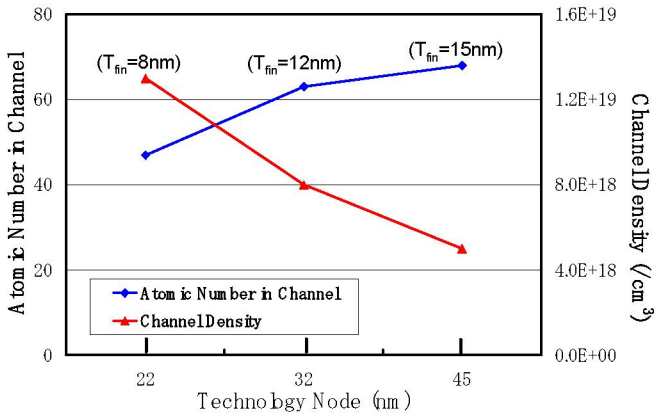

Figure 10. Frequency distribution of SNM as scaled down in FinFET.

IV. CONCLUSION

SNM and fluctuations in FD SGSOI and FinFET 6T SOI SRAM cell were analyzed by 3D process emulation and devise simulation. As for SNM, FinFET is a promising candidate up to 32nm node, but for 22nm node, it will be difficult even for FinFET to operate with stability.

As for fluctuations, the total number of dopant in channel is the key factor. The fluctuations of SNM in FinFET are reduced by balancing fin thickness and dopant density in channel depletion layer. In further scaled regime, these parameters in FinFET will become crucial for designing future SRAM circuit.

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