# Active and Passive RF Device Compact Modeling in CMOS Technoloies

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***Abstract*— A new method for extracting π-type substrate resistance model of RF MOSFETs based on 3-port measurement is presented. Using NQS and macro-model with extracted substrate components, it is verified that the new substrate resistance model is accurate. Also, temperature dependent macro model is developed. An analytical high frequency thermal noise model for short-channel MOSFETs which covers all operating regions is developed. A simple wide-band model for on-chip inductors on silicon is presented. Finally, an RF model of an accumulation-mode MOS varactor is presented.**

***Keywords-Substrate resistance, RF MOSFET modeling, Macro-modeling, Three-port measurement, Non-quasi-static effect, analytical thermal noise modeling***

## I. INTRODUCTION

The RF performance of CMOS transistors has been improved considerably over the past years due to the continuous downscaling of CMOS technology [1]-[4]. Thus, standard CMOS technology has become a popular choice for realizing radio frequency (RF) application. An important issue for RF devices is the availability of compact RF models of both the active devices and the passive devices to accurately predict the RF characteristics at high frequencies, including the millimeter wave range. For modeling of RF MOSFETs, the substrate-signal coupling network model and non-quasi-static effect (NQS) are important at high frequency close to and higher than $f_T$. In this paper, an analytical parameter extraction method of π-type substrate-signal coupling model based on three-port device measurement data is proposed for the first time. All the components of the substrate-signal coupling network including junction capacitances and substrate resistances can be directly extracted from the device measurement raw data. It is verified that the NQS model using the π-type substrate model agree well to the measured Y-parameter data up to 110 GHz. Also, the macro model composed of BSIM4 model, π-type substrate model, and various extrinsic parameters is developed. The macro modeling results at different temperature are compared to the measured S-parameter data.

Noise in MOSFETs are classified into 1/f noise, shot noise, thermal noise, and so on. The 1/f noise mainly affects the low-frequency performance of the device and can be ignored at high frequency. In addition to the channel thermal noise at the drain, at high frequency the local noise sources at the channel are capacitively coupled to the gate and generate an induced gate noise. Several noise models in integral forms have been reported for short-channel MOSFETs. However, analytical noise model is needed for circuit design application. In this paper, analytical channel thermal noise and induced gate noise current are presented, which considered velocity saturation effect and are valid in all operation region ; linear and saturation regions. The predicted niose power spectral density is compared with noise measurements.

Also, we present a simple wide-band inductor model which has the drop-down characteristics of the series resistance ($R_s$) as well as the increase characteristics in the $R_s$ as a function of frequency. The inductor model shows high accuracy over whole frequency range by taking the coupling through the silicon substrate into account to model the decrease in the $R_s$ at high frequency. Finally, an efficient and accurate parameter extraction method of an equivalent circuit of varactors is presented.

## II. HIGH FREQUENCY MODELING OF RF MOSFETS

### *A. Substrate resistance extraction method based on 3-port measurement*

The test device is an n-MOSFET having 16-unit gate fingers with L = 0.13 ㎛ and $W_f$ = 1.8 ㎛. The two-port S-

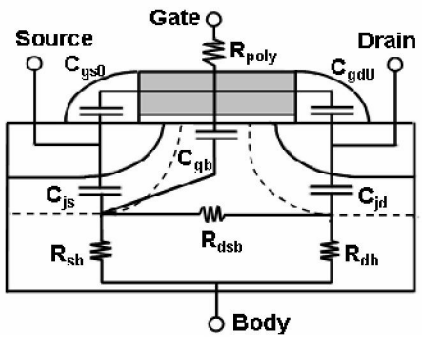


Figure 1. Equivalent circuit of an off-state MOSFET with π-type substrate resistance model.

 

parameters were measured in the common source-body configuration up to 110 GHz.

Fig. 1 shows a small-signal equivalent circuit of an off-state RF MOSFET[1]. The three-port measurement for extraction of π-type substrate resistance is performed by using Agilent N5240A vectornetwork analyzer [2]. $C_{gs0}$ and $C_{gd0}$ represent the gate to source and gate to drain extrinsic capacitances, respectively. $C_{gb}$ is the capacitance between gate and body. $C_{js}$ and $C_{jd}$ represent the junction capcitance of source and drain, respectively. π-type substrate resistance is adopted in the paper. $R_{sb}$, $R_{db}$, and $R_{dsb}$ represent resistances from source and drain to body, and source to drain, respectively. $R_{poly}$ represents the resistance of the polysilicon gate. The small-signal equivalent circuit shown in Fig. 1 can be analyzed in terms of Y-parameters. Using the analyzed Y-parameter equation, $C_{gd0}$, $C_{gs0}$, $C_{gb}$, $C_{js}$, $C_{jd}$, $R_{sb}$, $R_{db}$, and $R_{dsb}$ can be directly extracted from the real and imaginary parts of the Y-parameters. The following equations (1)-(3) represent the results for $R_{dsb}$, $R_{db}$, and $R_{sb}$.

$$R_{dsb} = \frac{\mathrm{Re}(Y_{SS})\mathrm{Re}(Y_{DD})}{\omega^2 C_{js}^2 C_{jd}^2\,\mathrm{Re}(Y_{SD})} - \frac{\mathrm{Re}(Y_{SD})}{\omega^2 C_{js}^2 C_{jd}^2} \tag{1}$$

$$R_{db} = \frac{1}{\omega^2}\frac{\mathrm{Re}(Y_{SS})\mathrm{Re}(Y_{DD}) - \mathrm{Re}(Y_{SD})^2}{C_{jd}^2\,\mathrm{Re}(Y_{SS}) - C_{js}C_{jd}\,\mathrm{Re}(Y_{SD})} \tag{2}$$

$$R_{sb} = \frac{1}{\omega^2}\frac{\mathrm{Re}(Y_{SS})\mathrm{Re}(Y_{DD}) - \mathrm{Re}(Y_{SD})^2}{C_{js}^2\,\mathrm{Re}(Y_{DD}) - C_{js}C_{jd}\,\mathrm{Re}(Y_{SD})} \tag{3}$$

## B. *NQS modeling of RF MOSFET*

Fig. 2 shows a non-quasi-static small-signal equivalent circuit of the RF MOSFET operating in the strong inversion region. $R_{gs}$ and $R_{gd}$ are the distributed channel resistance. $R_s$ and $R_d$ are the source and drain resistances, respectively. Transport delay is represented by $\tau_m$ in the transconductance parameters. $C_{sdx}$ is the capaci-tance between the source and the drain due to the DIBL effect in the short channel devices. The substrate-signal-coupling network consists of junction capacitances and π-type substrate model. In Fig. 3, the Y-parameters simulated with the extracted parameters were compared with the measured data at $V_{GS} = V_{DS} = 1\ V$. The NQS

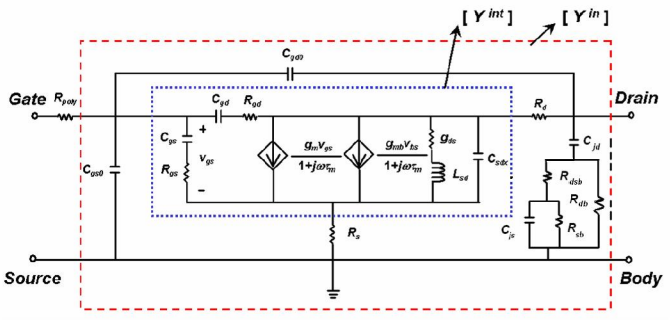


Figure 2. NQS model of RF MOSFET operating in strong inversion region.

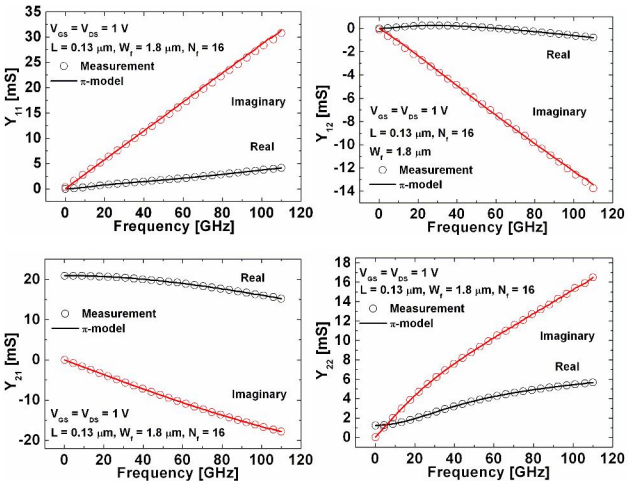


Figure 3. The modeled (NQS) and measured Y-parameters at $V_{GS} = V_{DS} = 1$ V for 0.13 μm RF nMOSFET.

model with π-type substrate model agrees well to the measured Y-parameters up to and above $f_T$ (up to 110 GHz) as shown in Fig. 3.

## C. *Macro-modeling for RF CMOS circuit design*

Fig. 4 shows the macro-model of the RF MOSFETs, which is implemented as a subcircuit extension to the BSIM4 model. It consists of the BSIM4 model, gate electrode resistance $R_{poly}$, distributed channel resistance $R_{ch}$, source/drain resistance $R_s$ / $R_d$, parasitic compensation capacitances $C_{gdx}$ /$C_{gsx}$ /$C_{sdx}$, and π-type substrate model. Fig. 5 compares the measured and the modeled S-parameters of RF MOSFET using the extracted parameters and BSIM4 model. It shows that the modeled S-parameters (solid line) fit the measured ones well without any optimization after parameter extraction. The RMS modeling error is below 10 % up to about 80 GHz. Fig. 6 shows the macro-modeling results at high temperature (125 °C). Through the extraction results from the measurement data, temperature coefficient of substrate resistance was obtained to be 3760 ppm/°C. The RMS modeling error is below 10 % up to about 70 GHz even at 125 °C.

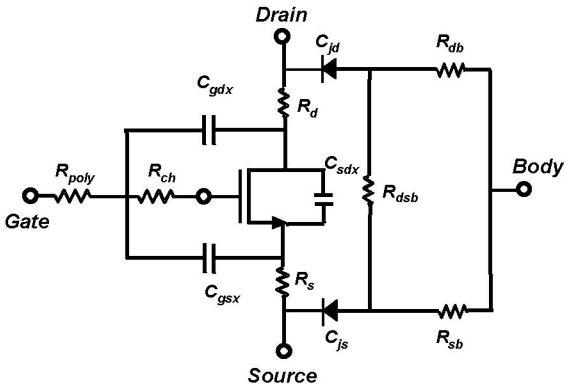


Figure 4. The macro-model for RF MOSFETs, which is implemented as a subcircuit extension to the BSIM4.

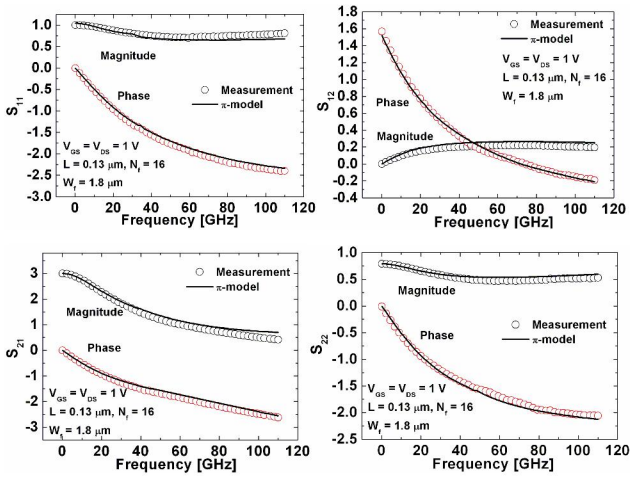


Figure 5. The macro-modeled and measured S-parameters at $V_{GS} = V_{DS} = 1$ V for 0.13 μm RF nMOSFET ( T = 25 °C ).

The small modeling error indicates that the extrinsic parameter extraction method and the BSIM4 parameters are very accurate. Fig. 7 compares the $I_{DS}$-$V_{DS}$ measurement data and simulation data of macro-model. The proposed macro-model agrees well to the DC I-V curve as well as high frequency Y- and S-parameter data.

## III. HIGH FREQUENCY NOISE MODEL

### *A. Analytical modeling of MOSFET thermal noise*

Analytical noise models for the drain thermal noise, induced gate noise, and their correlation coefficient in deep-submicron MOSFETs, which are valid in both linear region and saturation region, are needed for RF IC design and device

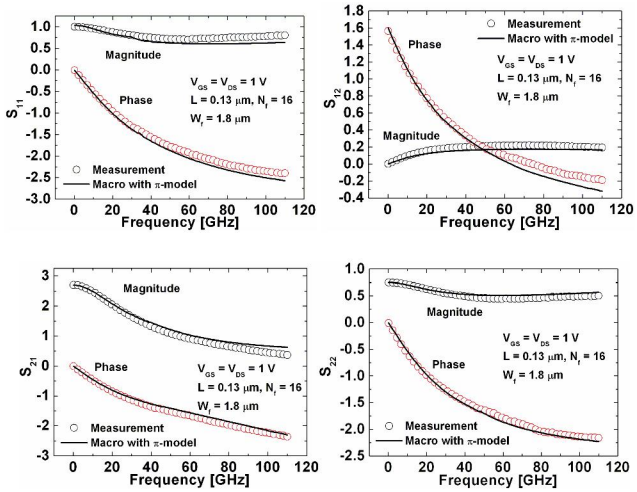


Figure 6. The macro-modeled and measured S-parameters at $V_{GS} = V_{DS} = 1$ V for 0.13 μm RF nMOSFET ( T = 125 °C ).

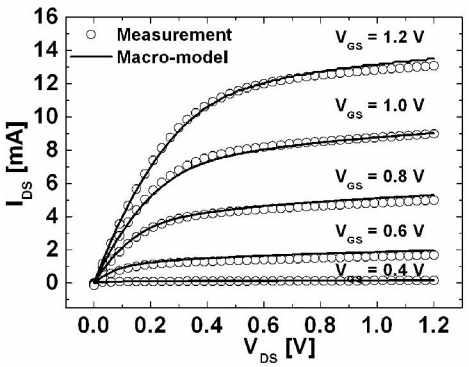


Figure 7. DC $I_{DS}$-$V_{DS}$ measurement and simulation data of macro-model.

optimization. In MOSFETs, the dominant noise contribution comes from the channel thermal noise having a power spectral density given by [5]

$$\left\langle i_{dn}^2 \right\rangle = 4kT\Delta f\, G_{do}\, \gamma \tag{4}$$

with

$$\gamma = \frac{L_{eff}}{L_{elec}}\left( \frac{1-u+\frac{u^2}{3}}{(1-u/2)(1+z)} + \frac{1}{1+z}(1-u/2) \right) \tag{5}$$

where $G_{do}$ is the intrinsic drain conductance at $V_{DS}$=0, $u = \alpha V_{DS}/V_{GT}$, $z = V_{GT}/V_L$, $V_L = L_{elec}E_c$, $L_{elec}$=*electrical channel length*. $L_{elec}$ could be obtained as[6]

$$L_{elec} = \frac{V_{GT}(V_{GT} - V')}{\alpha E_c V'} \tag{6}$$

where $V' = I_{DS}/WC_{ox}v_{sat}$, which can be extracted from dc and S-parameter measurements.

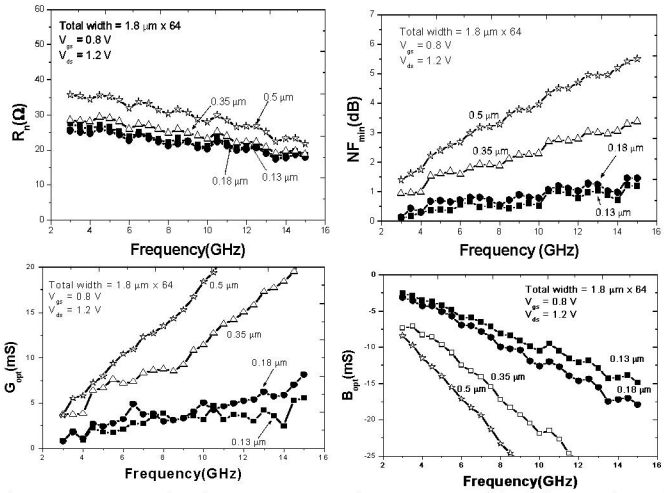


Figure 8. Measured noise parameters of MOSFETs with different channel lengths.

 

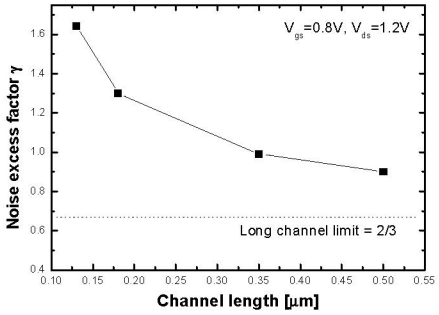


Figure 9. The modeled noise excess factor $\gamma$ versus channel length for NMOS with fixed W = 1.8 μm x 64.

At high frequency, the local channel voltage fluctuations due to channel thermal noise coupled to the gate through the oxide capacitance and it causes the induced gate noise having a power spectral density given by

$$\left\langle i_{gn}^2 \right\rangle = 4kT\Delta f \frac{(\omega C_{gs})^2}{5G_{d0}}\beta \tag{7}$$

with

$$\beta = \frac{(WC_{ox}L_{elec})^2}{C_{gs}^2}\frac{L_{elec}}{L_{eff}}\frac{8(45-90u+63u^2-18u^3+2u^4)}{27(2-u)^5} \tag{8}$$

Finally, the correlation between the channel thermal noise and induced gate noise can be derived as

$$\left\langle i_{gn} i_{dn}^* \right\rangle = 4kT\Delta f(j\omega WC_{ox}L_{elec})\frac{u(6-6u+u^2)}{9(2-u)^3}(1+z)^2 \tag{9}$$

Then, the correlation coefficient **C** can be calculated by using the above results.

$$C \equiv \frac{\left\langle i_{gn} i_{dn}^* \right\rangle}{\sqrt{\left\langle i_{gn}^2 \right\rangle \left\langle i_{dn}^2 \right\rangle}} = j\frac{\frac{u(6-6u+u^2)}{6(2-u)^3}(1+z)^2}{\sqrt{\frac{\gamma\beta}{5}}} \tag{10}$$

## B. *Experimental results*

The test devices have the unit finger width and the number of finger of 1.8 μm and 64, respectively. The noise parameters ($NF_{min}$, $R_n$, and $Y_{opt}$) were measured in the frequency range from 3 GHz to 15 GHz as shown in Fig. 8. Fig. 9 shows the modeled $\gamma$ by using our model. As channel length increases, $\gamma$ in saturation region approches to long-channel limit 2/3[7]. Intrinsic noise source power spectral density ($S_{idn}$, $S_{ign}$) could be extracted from measured noise parameters by using correlation matrix method [8].

Fig.10 shows the extracted and modeled channel thermal noise and induced gate noise as a function of frequency for

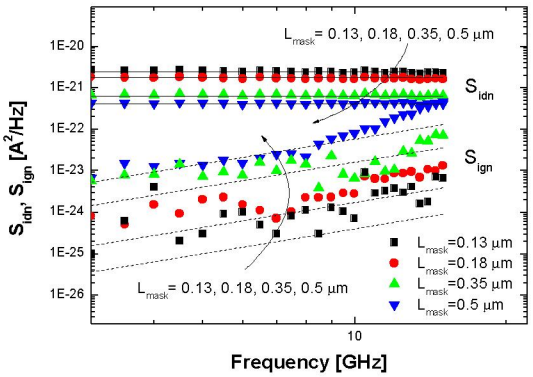


Figure 10. Extracted and modeled channel thermal noise($S_{idn}$) and induced gate noise($S_{ign}$) versus frequency characteristics for n-type MOSFETs biased at $V_{GS}$=0.8V, and $V_{DS}$=1.2V.

various gate length L=0.13 μm, 0.18 μm, 0.35 μm and 0.5 μm, biased at $V_{GS}$=0.8V, and $V_{DS}$=1.2V. Modeling results show good agreement with the extracted data. The channel thermal noise is white and the induced gate noise is proportional to $\omega^2$ as shown in Fig. 10. The solid and dot lines in the Fig. 10 represent the modeled values of $S_{ind}$ and $S_{ing}$ using proposed equations, respectively. The drain thermal noise becomes larger as the gate length scales down because the channel conductance becomes large. On the contrary, since the channel resistance becomes smaller as the gate length scales down, the induced gate noise becomes smaller. We can expect that the gate induced noise becomes less important for future scaled devices.

# IV. RF Modeling of On-Chip Inductors and Varactors

## A. *Modeling of inductors*

The on-chip inductor on silicon substrate can be treated as a collection of metal strips with substrate coupling, and hence the $R_{sub}$ and $C_{sub}$ to represent the lateral substrate coupling is introduced in our model as shown in Fig. 11 [9].

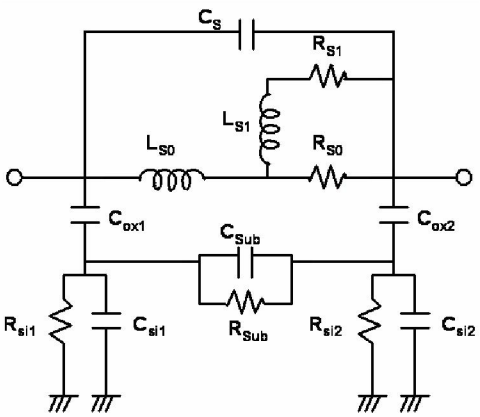


Figure 11. Inductor model with $R_{sub}$ and $C_{sub}$ to model substrate effects.

A parallel combination of $R_{sub}$ and $C_{sub}$ is placed in the silicon substrate similar to the equivalent circuit model for the on-chip interconnects. $C_{ox}$ represents the oxide capacitance between the inductor and the substrate. $R_{si}$ and $C_{si}$ are the substrate resistance and capacitance to ground, respectively. Moreover, the LR ladder circuit formed by $L_{s1}$ and $R_{s1}$ in parallel to $R_{s0}$ is used to capture the increase in the series resistance due to both skin and proximity effects. In order to verify the accuracy of our model, square spiral inductors with various geometrical configurations were fabricated using 0.18 $\mu$m 6-metal CMOS technology. The fabricated inductors have metal width (W) of 14.5 $\mu$m and spacing (S) of 2 $\mu$m. Two-port S-parameters were measured using an Agilent 8510C network analyzer and RF probes. After de-embedding pad parasitics using open pad structure, the equivalent series resistance $R_s(f)$ and series inductance $L_s(f)$ were extracted from $Y_{21}$ :

$$R_s(f)+j\omega L_s(f)=-\frac{1}{Y_{21}} \tag{11}$$

And the quality factor was evaluated by

$$Q=-\mathrm{Im}(Y_{11})/\mathrm{Re}(Y_{11}) \tag{12}$$

Fig. 12 shows the $R_s(f)$ and the $L_s(f)$ curves for six test structures with different number of turns. As the measurement curves show, the series resistance increases with frequency at first and drops down at higher frequency. The decrease in the $R_s(f)$ is caused by the lateral substrate coupling among inductor metal strips. As shown in Fig. 12 (a), the conventional model (the model without the $R_{sub}$ and $C_{sub}$ in Fig. 11) could predict the increase in the $R_s$ but could not model the decrease in the $R_s$ at high frequency. Also, as shown in Fig. 12 (b), the model predicts the change in inductance as a function of frequency, but the conventional model does not. The conventional model significantly overestimates the $R_s$ and underestimates the Ls at high frequency, which introduces large error in the circuit simulation such as transient analysis. As the number of turns increases, the substrate coupling between metal strips becomes larger because the $C_{ox}$ and $C_{sub}$ are larger. And therefore, the $R_s(f)$ drops down at lower frequency.

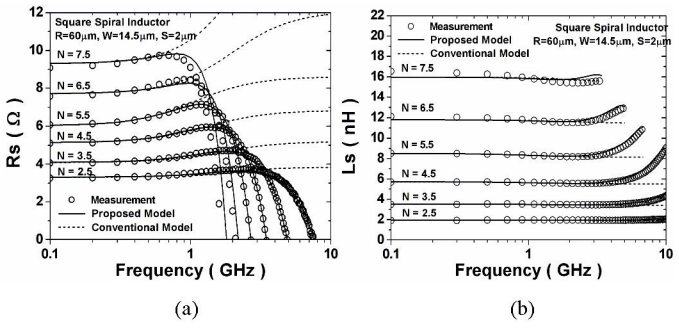


Figure 12. (a) series resistance and (b) series inductance comparison between the measurement and the model.

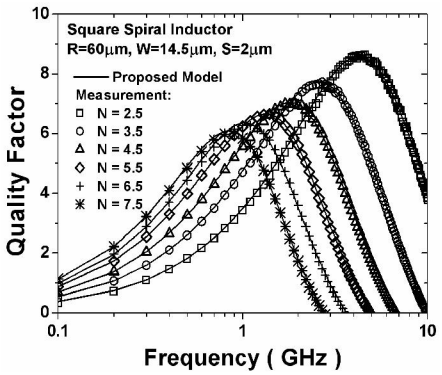


Figure 13. Measured and modeled quality factor of various number of turns.

Fig. 13 verifies quality factor for different number of turns and inner radius. The presented model matched accurately with the measurement over whole frequency range of interest. Also, we obtained excellent agreement in the peak Q, the frequency at the peak Q, and the self-resonance frequency. The model shows excellent scalability and wide-band accuracy.

## B. *Modeling of varactors*

The cross-section of an accumulation-mode MOS varactor is shown in Fig. 14 [10]. An equivalent circuit with physically meaningful components derived from Fig. 14 is shown in Fig. 15. In Fig. 15, $C_s$ refers to the series connection of gate oxide capacitance and depletion capacitance. $C_f$ represents the fringing capacitance associated with the sidewall of the gate. $L_g$ and $R_{poly}$ are the inductance and resistance of the gate, respectively. For accurate modeling of gate bias dependence of channel resistance ($R_{ch}$), $R_{acc}$, $R_p$, and $R_s$ have been used. $R_{acc}$ represents the accumulation resistance in the channel region. $R_p$ is the n-well resistance in parallel with $R_{acc}$ and $R_s$ is the gate bias independent resistance of $R_{ch}$ in series with the parallel connection of $R_{acc}$ and $R_p$. The resistance in the source/drain regions is represented by $R_{sd}$. $R_{well}$ is the vertical resistance of n-well, $C_{sub1}$ is the depletion capacitance between n-well and p-substrate, and the parallel combination of $R_{sub}$ and $C_{sub2}$ models the lossy silicon substrate.

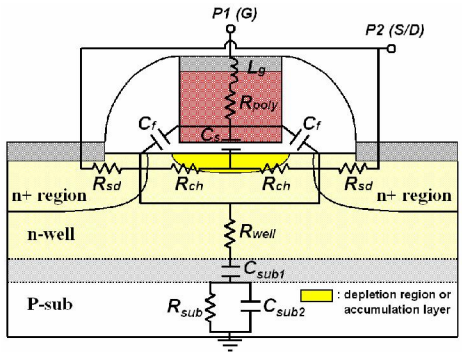


Figure 14. The cross-section of an accumulation-mode MOS varactor.

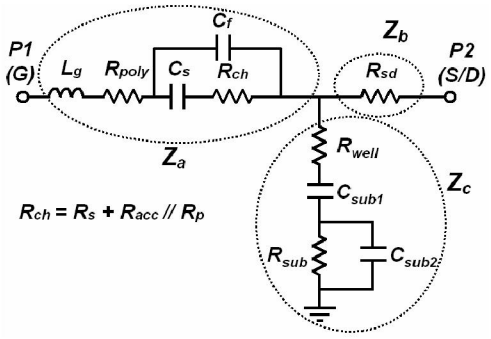


Figure 15. An equivalent circuit for MOS varactor.

To verify the proposed equivalent circuit, we have performed the direct extractions with *Z*-parameters of the MOS varactor having gate length of 0.50 μm and total width of 100 μm, fabricated in a standard 0.18-μm CMOS process. Two-port *S*-parameter measurements were performed in the frequency range from 0.5 GHz to 18 GHz.

Assuming $\omega R_{ch}C_sC_f << C_s+C_f$ and $\omega^2 R_{ch}^2 C_s^2 C_f << C_s+C_f$ in Fig. 15, we can define $R_{g,eff}$ and $C_{g,eff}$ as the following equations:

$$R_{g,eff} \approx R_{poly} + R_{ch}\left(C_s / C_{g,eff}\right)^2, C_{g,eff} \approx C_s + C_f \tag{13}$$

From the equivalent circuit, *Z*-parameters can be obtained with Eq. (13),

$$Z_a = Z_{11} - Z_{12} = R_{g,eff} + j\left(\omega L_g - 1/\omega C_{g,eff}\right) \tag{14}$$

$$Z_b = Z_{22} - Z_{12} = R_{s/d} \tag{15}$$

$$Z_c = Z_{12} = R_{well} + \frac{R_{sub}}{1+\omega^2 R_{sub}^2 C_{sub2}^2} - j\left(\frac{1}{\omega C_{sub1}} + \frac{\omega R_{sub}^2 C_{sub2}}{1+\omega^2 R_{sub}^2 C_{sub2}^2}\right) \tag{16}$$

Using the above equations, all the parameters were extracted. Fig. 16 shows that there is an excellent agreement between the model and the measurement.

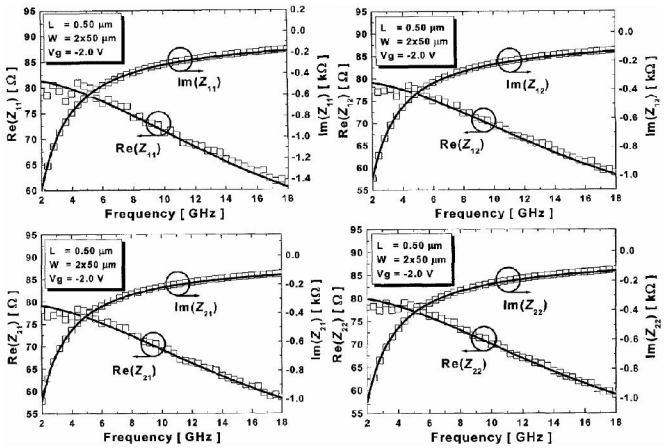


Figure 16. Measured (symbol) and simulated (solid line) Z-parameters at Vg = -2.0 V.

## V. Conclusion

Analytical parameter extraction method for π-type substrate resistance network of RF MOSFETs based on 3-port measurement was presented for the first time. The accuracy of NQS and macro-model with π-type substrate resistance network were verified with the measured data up to 110 GHz. The macro-model verification was performed through measurement and parameter extraction at different temperature. The analytical channel thermal noise and the induced gate noise current have been presented, which are valid in all operation regions for short channel MOSFETs. The analytical noise model was verified using noise parameter measurements. A simple wide-band model for on-chip inductors on silicon was presented. Finally, model verification for a RF model of an accumulation-mode MOS varactor was performed.

## Acknowledgment

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