Exploring Transistor Width Effect on Stress-induced Performance Improvement in PMOSFET with SiGe Source/Drain

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Abstract **-** Stress distribution in the Si channel regions of SiGe source/drain PMOSFETs with various widths is studied by 3D simulations. The width dependence of performance improvement is analyzed via device simulations.

I. INTRODUCTION

PMOSFET with epitaxially grown SiGe source/drain (S/D) or source/drain extension (S/DE) regions has been proven to provide increased performance due to the improved hole mobility [1] [2]. Drive current improvements of 25% (for SiGe at S/D) [1] and 35% (for SiGe at S/DE) [2] have been reported. The drive current improvement and mobility enhancement have been largely attributed to the longitudinal uniaxial compressive stress induced by the SiGe source/drain regions [1]. However, the lattice mismatched SiGe regions also induce stress in the Si channel along the width (transverse) and vertical directions. This paper presents a simulation analysis of width dependence of stress components (longitudinal, vertical and transverse) in PMOS channel region, and subsequently the influence on drive current.

II. METHODOLOGY

A simplified 3D PMOS structure shown in Fig. 1 is studied in this paper. The Si channel is confined by epitaxially grown SiGe in S/D along the transport (x) direction and by STI in the width (z) direction. The whole structure is built on top of a Si substrate.

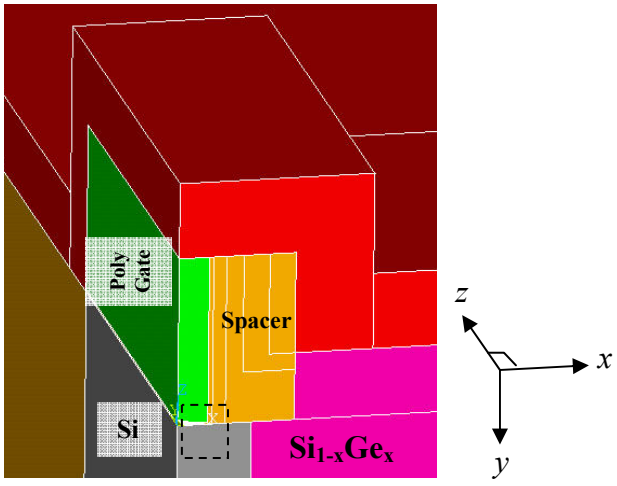

Fig. 1 Schematic PMOS device structure.

A well-developed mechanical stress simulator, ANSYS [3], has been used to calculate stress distribution. Periodic boundary conditions are applied on boundaries far away from the MOSFET. The stress in MOSFET channel region induced by expansion of SiGe is simulated by simultaneously solving equations of continuity and momentum balance together with constitutive relations.

The longitudinal compression of Si lattice in channel region breaks symmetry of the band structure which lifts degeneracy at Gamma point of the heavy and light hole bands. The break of symmetry also results in a decrease of hole effective mass along the transport (x) direction. Fig. 2 illustrates the heavy-hole band structure of a 0.5μm wide PMOSFET, calculated using a $sp^3d^5s^*$ empirical tight-binding model [4]. In addition to the benefit of lower hole effective mass, the stress along x and z directions (S_{xx} and S_{zz}) also cause a redistribution of carriers to low effective mass lobes and result in reduced inter-band scattering in hole transport [5]. Subsequently, the hole mobility in the Si channel increases. The relationship between mobility improvement and stress is well described by Piezoresistivity effect. In the coordinate system where the x-axis is aligned to the <110> crystal axes in the (100) plane,

$$\begin{pmatrix}\mu_{xx}\\ \mu_{yy}\\ \mu_{zz}\\ \mu_{yz}\\ \mu_{xz}\\ \mu_{xy}\end{pmatrix} = \mu^0\left(\begin{pmatrix}1\\1\\1\\0\\0\\0\end{pmatrix} - \begin{pmatrix}\Pi_{//} & \Pi_{12} & \Pi_{\perp} & 0 & 0 & 0\\ \Pi_{12} & \Pi_{11} & \Pi_{12} & 0 & 0 & 0\\ \Pi_{\perp} & \Pi_{12} & \Pi_{//} & 0 & 0 & 0\\ 0 & 0 & 0 & \Pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \Pi_{\Delta} & 0\\ 0 & 0 & 0 & 0 & 0 & \Pi_{44}\end{pmatrix}\cdot\begin{pmatrix}S_{xx}\\ S_{yy}\\ S_{zz}\\ S_{yz}\\ S_{xz}\\ S_{xy}\end{pmatrix}\right),$$

$$\Pi_{//} = \frac{\Pi_{11}+\Pi_{12}+\Pi_{44}}{2},$$

$$\Pi_{\perp} = \frac{\Pi_{11}+\Pi_{12}-\Pi_{44}}{2},$$

$$\Pi_{\Delta} = \frac{\Pi_{11}-\Pi_{12}+\Pi_{44}}{2},$$

where μ^0 denotes the isotropic mobility without stress, $\boldsymbol{\mu}$ is the mobility under stress $\boldsymbol{S}$ in the six-component vector notation, and Π_{ij} are the piezoresistive coefficients for holes. The piezoresistive coefficients for bulk silicon as reported in [6] are listed in Table I. It is noted that the hole mobility along transport (x) direction,

$$\mu_{xx} = \mu^0(1-\Pi_{//}S_{xx}-\Pi_{12}S_{yy}-\Pi_{\perp}S_{zz}),$$

is determined by stress along both the transport and width directions, S_{xx} and S_{zz}, due to the non-negligible value of $\Pi_{//}$ and $\Pi_{\perp}$, while stress along vertical direction, S_{yy},

has little effect on the hole mobility along the x direction due to very small Π_{12}.

The hole mobility in device simulator, Dessis [7] has been modified based on the piezoresistive coefficients. Ideally, piezoresistive coefficients for MOSFET inversion layers should be used. Since accurate and reliable measurements of inversion layer piezoresistive coefficients are not yet available, the bulk values are used as an approximation. Recent wafer bending measurements have confirmed that use of bulk piezoresistive coefficients is a good approximation for hole transport in the <110> channel direction on (100) silicon surface as studied in this paper [8].

The calculated stress components from ANSYS simulations are imported into DESSIS, after transforming stress from ANSYS mesh onto that of DESSIS (Fig. 3).

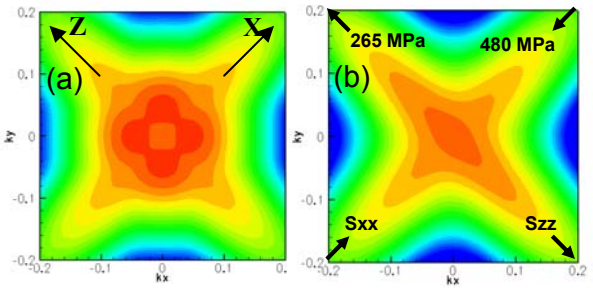

Fig. 2. Ground state bands of holes for a) unstrained transistor and b) transistor with SiGe S/D. Both compressive S_{xx} and tensile S_{zz} components results in lower effective mass along the transport (x) direction

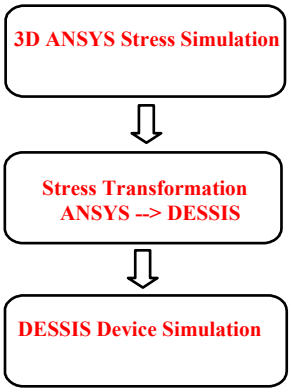

Fig. 3. Flow chart of stress and device simulations

Table I. Piezoresistive coefficients for holes in units of 10^{-12} cm^2 dyn^{-1}

Π_{11}	Π_{12}	Π_{44}	$\Pi_{//} = \frac{\Pi_{11}+\Pi_{12}+\Pi_{44}}{2}$	$\Pi_{\perp} = \frac{\Pi_{11}+\Pi_{12}-\Pi_{44}}{2}$	$\Pi_{\Delta} = \frac{\Pi_{11}-\Pi_{12}+\Pi_{44}}{2}$
6.6	-1.1	138	71.7	-66.2	71.8

III. RESULTS and DISCURSSIONS

A. Width-effect on Stress

The 2D contours in the *x-y* plane (across the center of device along width direction) of the three stress components, S_{xx}, S_{yy} and S_{zz} are plotted in Fig. 4. It can be seen that the stress stays relatively constant in the surface channel region beneath the gate where the hole transport is most critical. S_{xx}, S_{yy} and S_{zz} at the center of the surface channel versus transistor width are plotted in Fig. 5. As expected, in the narrow width regime, the tendency of SiGe to expand causes compressive stress along *x* direction, and tensile stress along *y* and *z* directions.

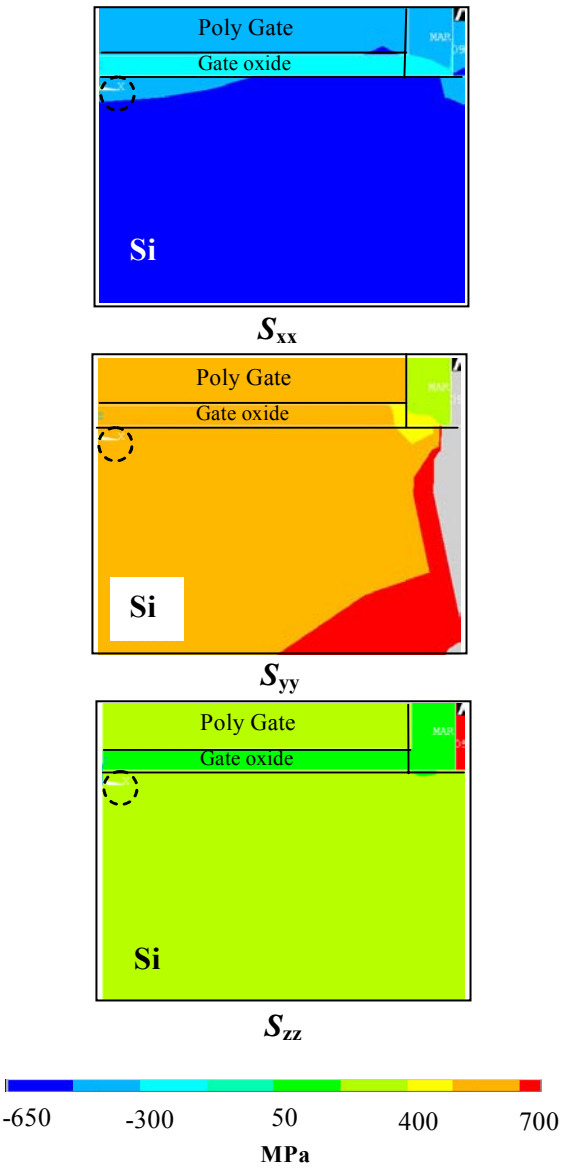

Fig. 4. Stress contours in transport (*x-y*) plane cut at center of the transistor width, which is illustrated as dashed box in Fig. 1. Circled areas are the locations of the surface channel at the center of width.

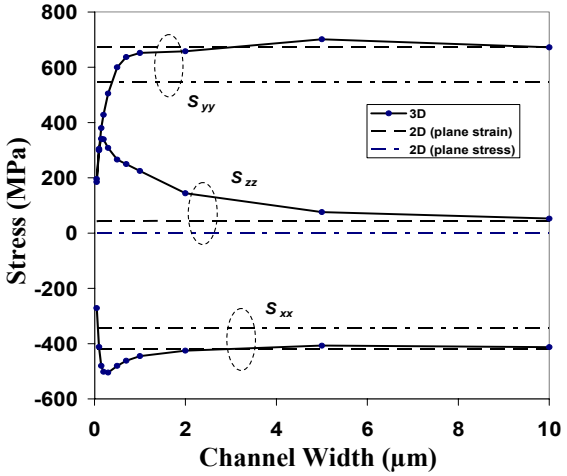

Fig. 5. Width dependence of three stress components (S_{xx}, S_{yy} and S_{zz}) at the center of the surface channel. Results from 2D simulations are also plotted for comparisons.

When the transistor width increases, stress along x direction, S_{xx}, first increases and reaches a peak value at w~0.15µm, then decreases to approach the solution of an infinitely wide device. The solution for an infinitely wide device can be obtained by a 2D simulation in the x-y plane with a plane strain boundary condition (zero strain along z direction). The peak S_{xx} at w~0.15µm is about 25% higher than that at infinite width. Due to the constraint from the Si substrate and STI, the strain in z direction approaches zero with increasing width, as shown in Fig. 6, resulting in the decrement of stress in z direction. On the other hand, S_{yy} increases with increasing width. When the width increases beyond about 5µm, all three stress components approach the 2D solutions with a plane strain boundary condition.

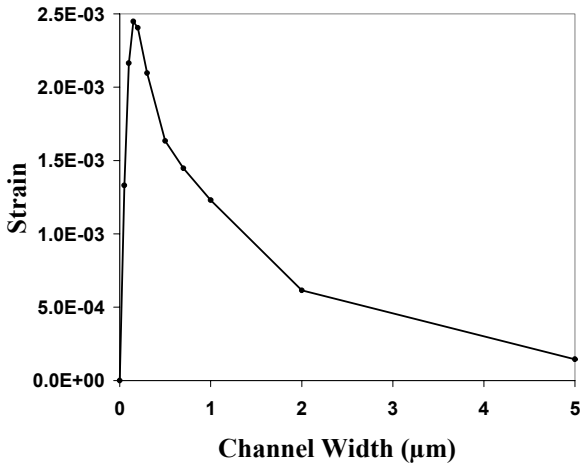

Fig. 6. The strain in z direction as a function of channel width. The strain plotted is at the center of the channel and 10nm below the gate oxide.

In state-of-the-art integrated circuit designs, the majority of PMOS transistors are in the width range between 0.1µm and 1µm, which is the region where the SiGe induced stress is most sensitive to changes in device width. Therefore, 3D mechanical simulation is necessary to accurately predict the stress distribution in the devices. Calculated stress in the Si channel by 2D ANSYS simulations with plain strain (zero strain in width direction) or plain stress (zero stress in width direction) boundary conditions is compared to 3D results as shown in Fig. 5. It is found that 2D stress simulation with plain strain boundary condition is only a good approximation to the real situation in devices wider than 5µm, while 2D stress simulation with plain stress boundary condition is not an appropriate approximation.

B. Width-dependent Drive Current Improvement

The consequent drive current improvement versus width is shown in Fig. 7. Similar to stress, the drive current improvement also shows considerable width sensitivity for widths between 0.1 and 1µm. Drive current gain increases with decreasing width and reaches a peak value at w~0.15µm. The drive current gain at w=0.15µm is ~10% more than that at the wide widths (w>5µm). With the further decrease of the device width, the drive current gain diminishes. In order to understand the stress component contribution to the drive current improvement, each stress component is imported into DESSIS separately; i.e., only one stress component is used in one set of device simulations. It is found that stress along the channel direction, S_{xx}, contributes most to the improvement, while S_{yy} contributes the least. Stress along the width direction, S_{zz}, noticeably enhances drive current in the narrow width regime, contributing almost one third of the total drive current gain.

The stress is not always uniformly distributed along the width direction. The non-uniformity is quite significant at w=0.15µm, as shown in Fig. 8. However, it is found that a simple drive current gain, calculated on a x-y cut plane at the center of the width, is a good approximation to a more accurate method such as weighted average of drive current gain on many x-y plane cut slices.

The effect of shear stress, S_{xy}, on drive current is not taken into account, since it is one order of magnitude lower than the normal stress components, S_{xx}, S_{yy} and S_{zz}.

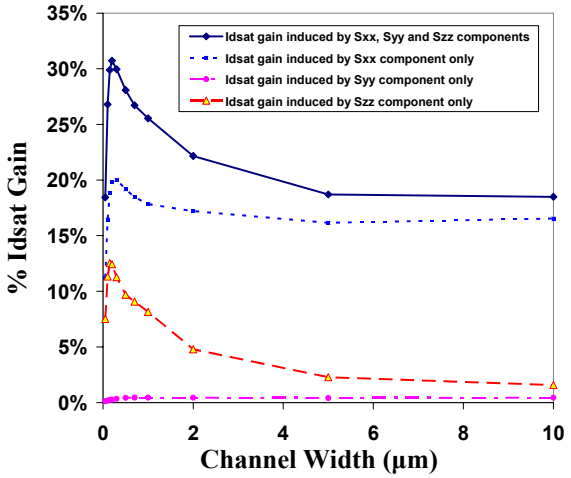

Fig. 7. Width dependence of drive current improvement induced by S_{xx}, S_{yy} and S_{zz} stress components (solid line). Idsat gains due to each individual component alone are also plotted.

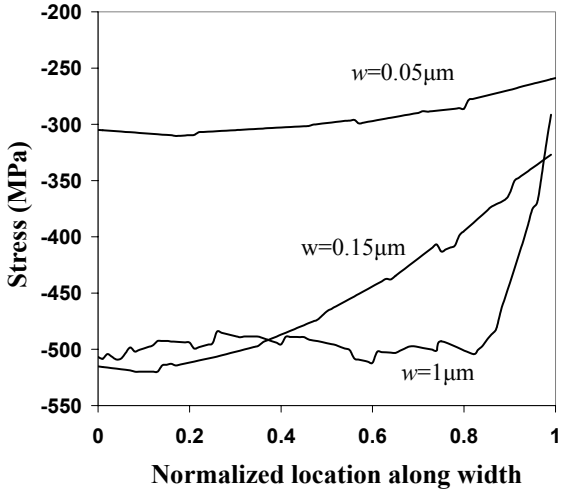

Fig. 8. The stress distribution in x direction as a function of normalized location in width direction. The stress plotted is at the middle of the channel and 10nm below the gate oxide.

IV. CONCLUSION

In this paper, we calculated stress components in three directions in the Si channel of PMOSFETs with epitaxially grown SiGe source/drain. The resulting drive current improvement was analyzed. Compressive stress along the transport direction was found to dominate drive current improvement. Stress along the vertical direction perpendicular to the gate oxide was found to affect drive current the least. However, for PMOSFETs with width between 0.1 and 1 µm, the tensile stress along the width direction makes considerable contribution to drive current improvement and can not be neglected. In conclusion, 3D stress simulations are necessary to accurately calculate drive current improvements induced by epitaxially grown SiGe source/drain.

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