A Quantum-Mechanical Analysis of the Electrostatics in Multiple-Gate FETs

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***Abstract*— In this work we investigate the electrostatics of three multi-gate device structures, namely the rectangular GAA-FET, the tri-gate FinFET and the Π-gate FET, all of them at three different miniaturization limits corresponding to the 90, 65 and 45 nm technology nodes of the ITRS. In doing so, we solve both the classical Poisson equation and the coupled Schrödinger-Poisson equations within the device cross sections, and compare the classical and quantum-mechanical (QM) solutions. This comparison highlights the qualitative and quantitative discrepancies between the two models, both in terms of charge distribution and device performance. These differences turn out to be very relevant for all device structures, and increase as the device size is scaled down. Thus, the main conclusion of this study is that accounting for quantum-mechanical effects in device simulation is essential for a realistic prediction of the device threshold voltage, inversion-layer charge and gate capacitance.**

I. INTRODUCTION

The Microelectronics industry has relied on shrinking transistor geometries for improvements in circuit performance and cost per function over three decades. In the future, continued transistor scaling will not be as straightforward as it has been in the past, because fundamental material and device limits are rapidly being approached with the bulk CMOS technology. Innovative device structures are needed to continue improving the device performance. Non-classical MOSFET architectures, such as ultra-thin-body single- or multi-gate transistors, can in fact be scaled down more aggressively than the bulk-CMOS ones, and may thus become promising candidates for future technology nodes.

The new emerging structures are all characterized by non-planar geometries, which lead to new process technology requirements. In order to meet the specs highlighted by the International Technology Roadmap for Semiconductors [1], future transistors will require high-permittivity (high-κ) gate dielectrics and metal gate electrodes with suitable work functions. Several non-planar, multi-gate (i.e., tri-gate and gate-all-around) structures have been proposed to obtain an effective gate control [2].

As the electrostatics, including quantum effects, becomes a crucial issue in the design of new device architectures, we address here the electrostatics of nanoscale FETs with various gate-geometry configurations, namely, the rectangular GAA-FET, the tri-gate FinFET and the Π-gate FET. Such devices represent the best trade off between performance and manufacturability among the different multi-gate silicon-based proposed structures [3]. Also, their architectures are similar enough to allow for a meaningful comparison between them.

This paper is organized as follows: in section 2, we discuss the numerical details of the approach used for the solution of the electrostatic problem; section 3 illustrates the results and discusses the potential advantages of each device. The conclusions are drawn in section 4.

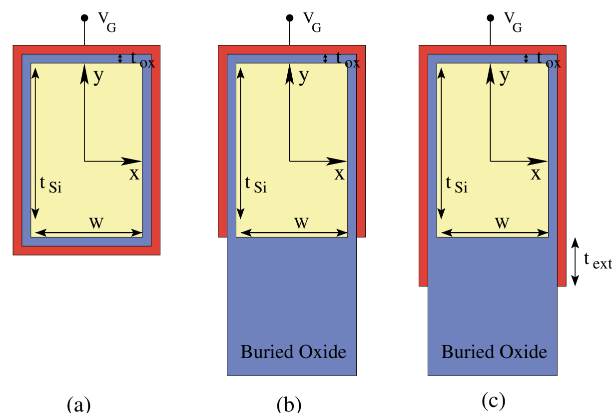

Fig. 1. The analyzed structures: (a) rectangular GAA-FET, (b) tri-gate FinFET and (c) Π-gate FET. Three different device sizes are considered for each of them, corresponding to the 90, 65 and 45 nm technology nodes, namely: $t_{\rm Si} = 40$ nm, $W = 20$ nm and $t_{\rm ox} = 2$ nm (90 nm node); $t_{\rm Si} = 20$ nm, $W = 10$ nm and $t_{\rm ox} = 1$ nm (65 nm node); $t_{\rm Si} = 10$ nm, $W = 5$ nm and $t_{\rm ox} = 0.7$ nm (45 nm node).

II. SIMULATION APPROACH

Figure 1 illustrates the cross section of the devices investigated in this work: (a) the rectangular GAA-FET, (b) the tri-gate FinFET, and (c) the Π-gate FET. These structures have been extensively explored in recent experimental works, due to their technological feasibility (see e.g. [4]). Three device sizes, corresponding to the 90, 65 and 45 nm technology nodes are considered for each of the above structures. The analysis of the electrostatics is carried out assuming zero drain and source voltages. The coupled Schrödinger-Poisson equations are solved in 2D within the device cross section. The electron wave functions are computed using a novel approach based on a rigorous semi-analytical method, which takes advantage from the existence of analytical unperturbed solutions within

the potential wells and provides very accurate results with a fast computation time [5]. More specifically, the devices are first addressed by analytically solving the Schrödinger equation within a rectangular potential well. This provides the unperturbed energy eigenvalues $E_{mn}^{(0)}$ and eigenfunctions $\psi_{mn}^{(0)}$. The first iteration of Poisson's equation is then computed, and its solution is used to determine the perturbation Hamiltonian $\delta\mathcal{H}$. Next, due to the completeness of the unperturbed eigenfunction set, ψ_{mn} is expanded in series of the corresponding unperturbed eigenfunctions $\psi_{mn}^{(0)}$:

$$\psi_{mn} = \sum_{jk} c_{jk}^{(mn)} \psi_{jk}^{(0)} \tag{1}$$

$$\psi_{mn}^{(0)} = \frac{2}{\sqrt{ab}} \sin\left[\frac{m\pi}{a}\left(x + \frac{a}{2}\right)\right] \sin\left[\frac{n\pi}{b}\left(y + \frac{b}{2}\right)\right]$$

$$E_{mn}^{(0)} = \frac{\pi^2\hbar^2}{2}\left(\frac{m^2}{m_x^* a^2} + \frac{n^2}{m_y^* b^2}\right)$$

where a and b are the channel heigth and width, respectively; m_x^*, m_y^* are the electron effective masses along the x, y directions, respectively, and $E_{mn}^{(0)}$ are the energy eigenvalues. Accounting for the 6 equivalent valleys of silicon, $m_{x,y} = m_l$ for 2 valleys and $m_{x,y} = m_t$ for 4 valleys. Hence, three sets of energy eigenvalues are generated, according to the three possible combinations of m_x^* and m_y^*, namely: $m_x^* = m_t^*$, $m_y^* = m_t^*$; $m_x^* = m_l^*$, $m_y^* = m_t^*$; $m_x^* = m_t^*$, $m_y^* = m_l^*$. For the sake of notational simplicity, we do not explicitly introduce an additional index to identify the three sets of eigenvalues.

Inserting (1) into the Schrödinger equation, one finds that the coefficients $c_{jk}^{(mn)}$ are the eigenvectors of the perturbation matrix **H**, whose entries h_{mnjk} are:

$$h_{mnjk} = \langle \psi_{mn}^{(0)} | \delta\mathcal{H} | \psi_{jk}^{(0)} \rangle + E_{jk}^{(0)}\, \delta_{mj}\, \delta_{nk}\,.$$

Also, the eigenvalues of **H** are the energy eigenvalues E_{mn} associated with the perturbed Hamiltonian.

Rather than using the standard textbook formulas of the perturbation theory, as suggested in [6], we numerically solve the resulting eigenvalue problem, and determine the exact expansion coefficients. The new sets of perturbed eigenvalues and eigenfunctions allow for the determination of the updated space charges. In this way the Schrödinger equation is solved in a semi-analytical form, thus largely eliminating discretization errors and providing very accurate energy eigenvalues and eigenfunctions. Also, we integrate the non-linear Poisson equation by the Newton-Raphson method, and compute the Jacobian matrix at each iteration by numerically differentiating the space charge. This approach turns out to be stable, and an order-of-magnitude faster than a fully-numerical solution, because the rank of the eigenvalue problem to be solved is equal to the number of unperturbed eigenfunctions used for the expansion, which is not too large for relatively-small device sizes. A classical model is used instead for holes, owing to their small influence on the device behavior.

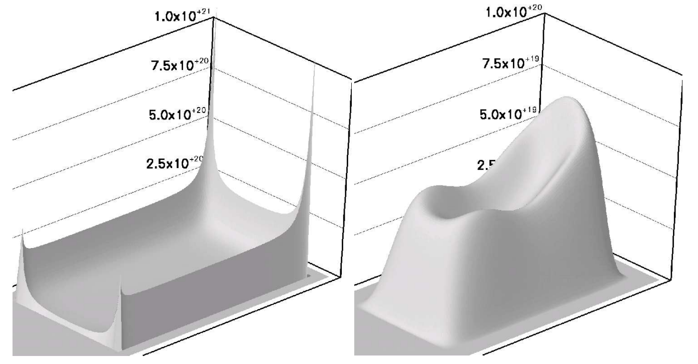

Fig. 2. Electron concentration n (cm^{-3}) in the tri-gate FinFET of $t_{\text{Si}} = 10$ nm, $W = 5$ nm, $t_{\text{ox}} = 0.7$ nm for $V_G = 1.0\,$V. Left: classical solution, right: quantum solution.

III. Results

Unlike single- or double-gate MOSFETs, multi-gate devices exhibit non-planar Si-SiO$_2$ interfaces with corners, which are expected to be responsible for an undesirable carrier non-uniformity within the inversion layer. Figure 2 shows the classical (left) and QM (right) electron concentration n within the channel of the tri-gate FinFET at $V_G = 1\,$V. The classical solution exhibits sharp peaks at the upper corners of the device, where n approaches $10^{21}\,\text{cm}^{-3}$. The QM solution is instead much more uniform along the inversion-layer ridge, with a peak concentration below $7 \times 10^{19}\,\text{cm}^{-3}$ at the center of the upper planar interface. Rather surprisingly, such a markedly-different behavior marginally affects the device threshold voltage at the device sizes considered in this work, so long as the impurity concentration is small enough to provide a negligible contribution to the band bending.

Figure 3 (top) shows the second derivative of the electron charge per unit length $N_e''(V_G)$ with respect to V_G for the largest tri-gate FinFET at two different impurity concentrations. The maxima of this plot represent the peak curvatures of the $N_e(V_G)$ function, which are related with the turning on of the inversion layer. The device with the lower impurity concentration exhibits a single peak, indicating that both corners and edges build up the channel at the same gate voltage, while the heavily-doped one exhibits two peaks in both models. The first peak corresponds to the charge inversion at the top corners; the second one is related to the top and sidewall channel formation. As expected, in the latter case the QM model predicts a larger threshold voltage, because the band bending within the depletion region is not negligible at high impurity concentrations. At the same time, the charge confinement at the center of the cross section increases the surface potential and reduces the corresponding voltage drop across the oxide, leading to a smaller amount of channel charge for a given gate voltage. This effect is stronger the higher the impurity concentration.

The electron charge per unit length at the top corners (n_{top}) is plotted in normalized form as a function of the gate voltage at the bottom of figure 3. This quantity has been computed as the

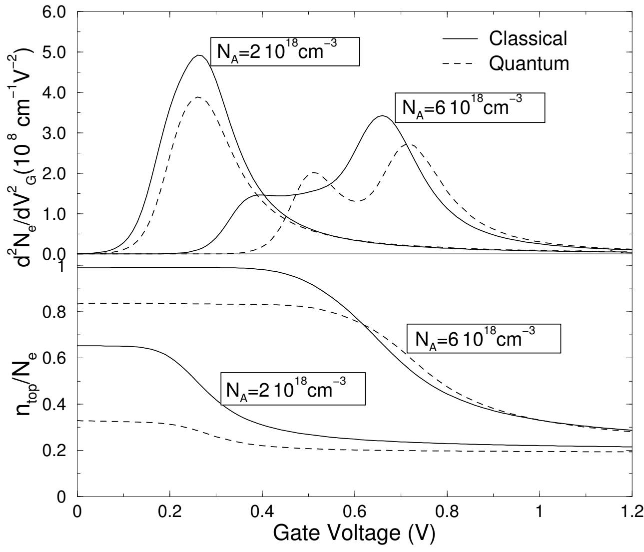

Fig. 3. Top: second derivative of the total electron density with respect to the gate voltage for the tri-gate FinFET of $t_{\mathrm{Si}} = 40$ nm, $W = 20$ nm, $t_{\mathrm{ox}} = 2$ nm and $N_A = 2 \times 10^{18}$ cm^{-3} and 6×10^{18} cm^{-3}. Bottom: relative contribution n_{top}/N_e of top corner densities to the total electron density (n_{top} has been obtained integrating the electron density over two squares with 5 nm side length on the two corners). Solid lines: classical solution, dashed lines: quantum solution.

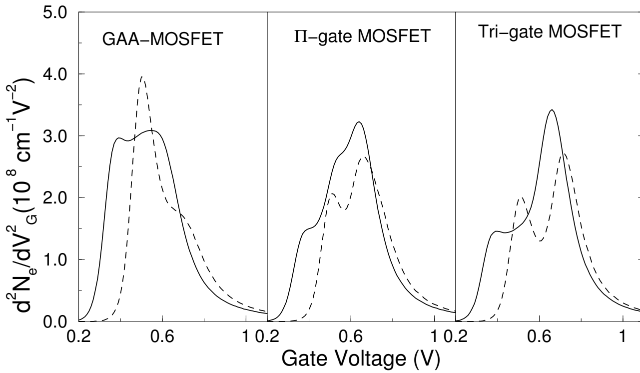

Fig. 4. Second derivative of the total electron density with respect to the gate voltage for the GAA-, the Π-gate FET and the tri-gate FET. $t_{\mathrm{Si}} = 40$ nm, $W = 20$ nm, $t_{\mathrm{ext}} = 10$ nm, $t_{\mathrm{ox}} = 2$ nm and $N_A = 6 \times 10^{18}$ cm^{-3}. Solid lines: classical solution; dashed lines: quantum solution.

integral of the electron density within two small squares with 5 nm side length on the two corners. Interestingly, n_{top}/N_e increases at low gate voltages from 60% to nearly 100% as the doping density N_A grows from 2 to 6×10^{18} cm^{-3}. This behavior indicates that the corner effect is stronger as doping increases. The QM solution provides a markedly smaller n_{top}/N_e ratio, because the charge is removed from the interface and more uniformly distributed. As the gate voltage increases, a transition occurs from the corner-dominated to the

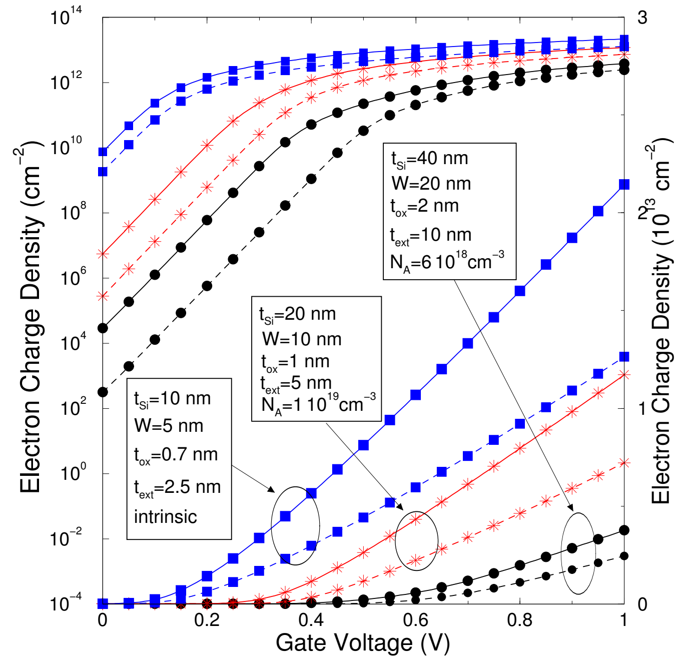

Fig. 5. Electron charge density per unit area of the Π-gate FET. The parameters of the 90 (circles), 65 (stars) and 45 nm (squares) technology nodes reported in the insets have been used. Solid lines: classical solution; dashed lines: quantum solution.

sidewall-dominated charge distribution, which is reflected by the decrease of the n_{top}/N_e ratio.

The effectiveness of the gate control on the electrostatic performance of the devices is shown in figure 4, which compares the second derivative N_e'' with respect to the gate voltage for the three FETs at their largest dimensional size. This comparison shows a better uniformity for the GAA-FET, where the gate completely surrounds the device active area.

Moreover, the influence of the scaling rules is investigated by changing the geometrical parameters t_{Si}, W, and t_{ox} according to the ITRS prescriptions for the 90, 65 and 45 nm technology nodes [1]. Figure 5 shows the charge density per unit area $N_e/[2(W + t_{\mathrm{Si}})]$ for the Π-gate FETs at each technology node. The electron density has been normalized to the device perimeter, in order to provide a fair comparison among devices with a different cross section. The subthreshold slope S is nearly ideal for the two smaller devices, whereas it becomes $\simeq$ 70 mV/dec for the larger one, which is only partially depleted. Also, the smaller devices exhibit a higher electron density per unit area, but the global electron charge per unit length is of course lower. For a fixed gate overdrive $V_G - V_T$ the difference between the QM and classical electron charge density per unit area turns out to be 29%, 38% and 45%, for the 90, 65 and 45 nm nodes, respectively. The reduced performance predicted by the QM model is due to the vanishing of the wave functions at the Si-SiO_2 interface, which shifts the inversion-layer charge away from it, thus reducing the inversion-layer capacitance.

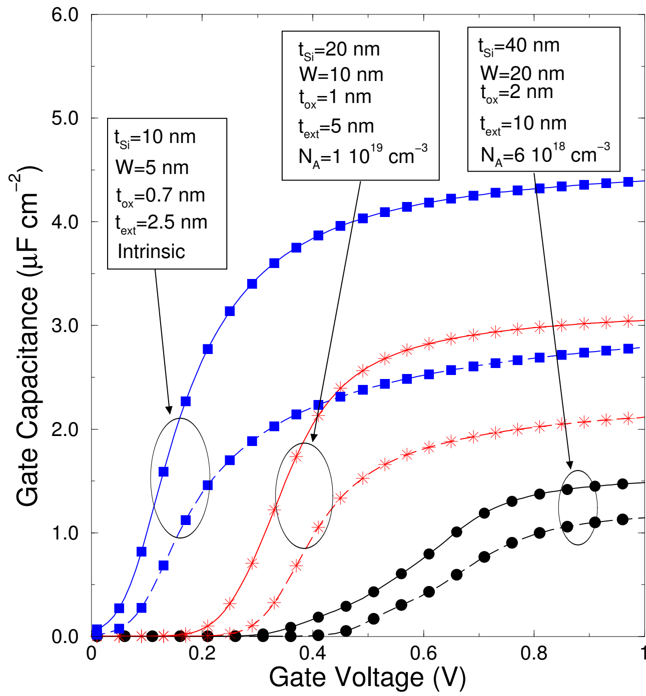

Fig. 6. Top: Gate capacitance per unit area vs. gate voltage for the Π-gate FET. The 90 (circles), 65 (stars) and 45 nm (squares) technology node parameters have been used in the computation. Solid lines: classical solution; dashed lines: quantum solution.

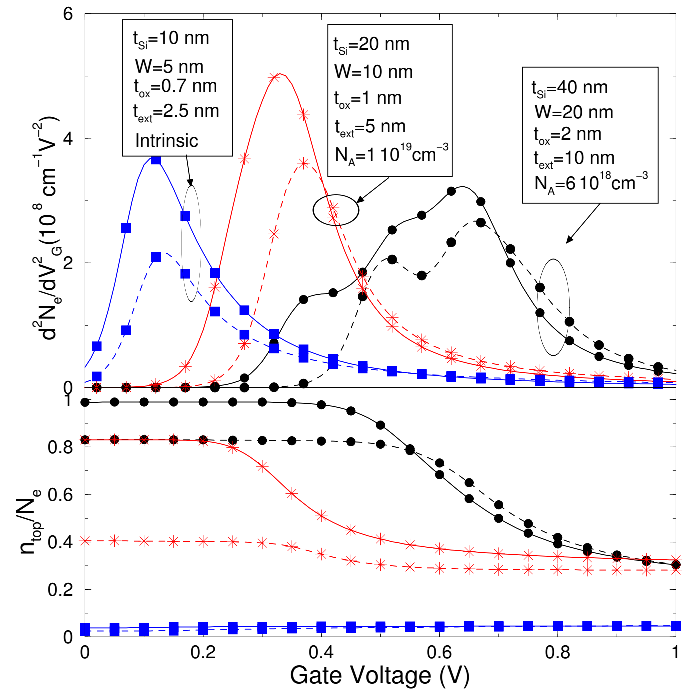

Fig. 7. Top: second derivative of the total electron density with respect to the gate voltage for the Π-gate FET. The 90 (circles), 65 (starts) and 45 nm (squares) technology nodes parameters have been used. Bottom: relative contribution n_{top}/N_e of top corner densities to the total electron density. Solid lines: classical solution; dashed lines: quantum solution.

Figure 6 represents the gate capacitance per unit area for the Π-gate FETs at each technology node. Here again, the gate capacitance per unit length has been normalized with respect to the device perimeter, in order to make the comparison among the three device sizes more easily understandable. The figure shows again fairly large discrepancies between the classical (solid lines) and the QM (dotted lines) models, which may be as large as 57%. The threshold shift which occurs as the device size increases is also highlighted by the figure. The smaller devices exhibit a higher gate capacitance per unit area, but a lower global capacitance per unit length.
Figure 7 (upper) shows the second derivative $N_e''(V_G)$ for the three Π-gate FETs with different sizes. Here again we see that, as the doping and the device size increase, the FET experiences a double threshold, and an increasing discrepancy between the classical and QM thresholds shows up. The lower figure shows the fractional charge at the corners for the same devices. As expected, corner effects become less pronounced the smaller the device size and the doping density.

IV. Conclusions

This study shows that accounting for quantum-mechanical effects in the analysis of multi-gate structures at low dimensional limits is essential for a realistic prediction of the device performance. The QM model invariably predicts a larger threshold, a less pronounced corner effect, a smaller charge density and a smaller gate capacitance. The error on the channel charge for a fixed gate overdrive may be as large as 29%, 38% and 45% at the 90, 65 and 45 nm technology nodes, respectively, if a classical solution is used.

Acknowledgment

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