# Physics and Performance of Phase Change Memories

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***Abstract* – Phase change memories (PCM) are considered promising candidates for the replacement of non-volatile Flash technology at the nanoscale. The paper reviews the physics of PCM operation, the scaling potentials of these devices, some options recently proposed for the cell structure, the main challenges for the PCM to become fully competitive with standard Flash technology.**

## I. INTRODUCTION

In the last decade, the impressive growth of the market for portable systems has been sustained by the availability of successful semiconductor Non-Volatile-Memory (NVM) technologies, the key driver being the Flash memories. In the last fifteen years the scaling trend of these memories has been straightforward. The cell density of NOR Flash, which is adopted for code storage, has doubled every two years, following the Moore's law. The memory cell size is 10-12$F^2$, where F is the technology feature size. The NAND Flash, which is optimized for sequential mass storage, has been aggressively scaled and, nowadays, has a cell size of about 4.5$F^2$. However, as the scaling proceeds the requirements for floating gate devices become even more challenging. The number of electrons stored on the floating gate decreases and, at the 32nm node, the maximum acceptable leakage over a ten years period will be less than 10 electrons per cell. It is therefore clear that floating gate devices should be replaced by other approaches providing reliable non-volatile devices at the nanoscale.

Different alternative memory concepts have been explored in the last years. Among them the phase change memory (PCM) is attracting growing interest. These devices were first proposed by S. Ovshinsky who, in the late 1960's, reported a reversible memory switching in chalcogenide materials [1]. The ability of these materials to undergo fast phase transformation has led to the invention and development of rewritable optical media (CD, DVD) [2]. Recently, the exploitation of the same concept for large-size solid-state memory circuits has been considered [3,4], making the PCM a candidate for mainstream non-volatile technology due to their large cycling endurance [5], fast program and access times, extended scalability [6].

Figure 1 shows the projection of the PCM scaling trend. The PCM cell size (8-10$F^2$ with a bipolar selector) will take full advantage of the technology

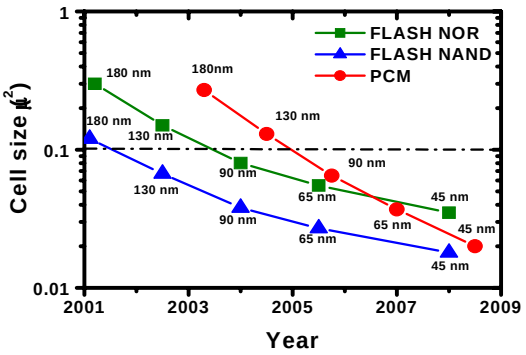


Fig. 1 - Scaling roadmap for Flash and Phase Change Memories.

scaling, reaching the NAND cell size around the 45-nm node. No intrinsic limitations are expected to stop the further scaling of this technology. Moreover the memory is ideally suited to store more than two levels per cell. This approach may become a viable option to further reduce the cost per bit of PCM devices.

## II. CELL STRUCTURE AND PROGRAMMING

A PCM cell is essentially a resistor (Fig. 2) with a phase-change chalcogenide material placed between bottom and top contacts. The active material (typically $Ge_2Sb_2Te_5$, or GST) presents two different phases (amorphous and polycrystalline) with largely different resistivity. Memory programming is accomplished by Joule heating: to form the amorphous phase, a 50 to 100ns current pulse heats up the region where current crowding takes place. GST reaches the melting temperature (620 °C). The following swift cooling, along the falling edge of the current pulse, freezes the molten material into a disordered, amorphous phase (Fig. 2-a). To recover the crystalline phase, Joule

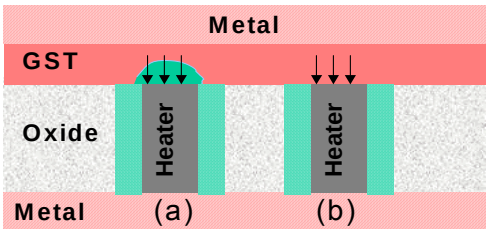


Fig. 2 - Schematic PCM cell structure, representing the different phase states.

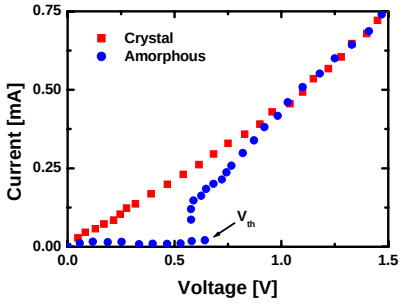


Fig. 3. Current-voltage characteristics of a PCM cell in both the reset and set state.

heating from another current pulse, with a lower amplitude, is used to speed-up the spontaneous amorphous-to-crystalline transistion: the crystalline phase builds-up in about 100ns by nucleation and growth processes (Fig. 2-b). Since the electrical resistivity of the two phases differs by orders of magnitude, the resistance of the two memory states ranges from kΩ (*set state*) to MΩ (*reset state*). Reading is then accomplished by measuring the current flowing through the cell at low bias voltage.

Figure 3 shows the typical I-V curve of a cell. When the cell is in the highly resistive state, *threshold switching* takes place. As the voltage rises above a threshold value, the curve suddenly snaps-back and the amorphous layer becomes highly conductive. Threshold switching makes possible to have large currents flowing through an amorphous layer even at low voltages. In this way amorphous to crystalline transformation (from Fig 2-a to Fig. 2-b) can be induced without the need of large supply voltage. In PCM programming, this effect plays a key role. No practical electrical memory could be conceived without threshold switching.

Figure 3 can help to discuss switching physics. In the low bias regime the amorphous GST layer is highly resistive. However, as the bias increases, the current exponentially rises due to impact ionization. The amorphous GST (Fig. 2-a) sustains most of the voltage drop and has a high density of localized states along the Te-Te chains ($10^{18}$-$10^{20}$cm$^{-3}$). At each bias point,

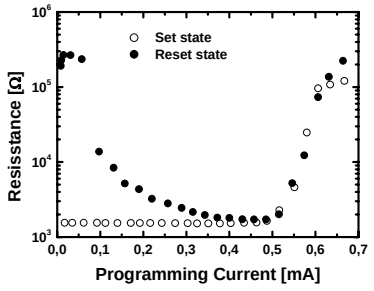


Fig. 4. Resistance as a function of programming current. Before each program pulse the cell is prepared either in the reset or set state.

carrier generation is balanced by recombination via these localized defect-states. However, by increasing the bias all the defects become fully saturated by recombining carriers and the only way the device has to find a new steady state condition is to swiftly reduce the voltage across the amorphous layer, quenching the generation rate [4]. A snap-back takes place and after switching the GST is still amorphous but highly conductive.

The I-V curve of the crystalline GST (*set state*) does not feature threshold switching and approaches the I-V of the reset state after switching. At large current values the slope of the curve is due to the resistance of the heater (Fig. 2). Across the GST layer there is an almost constant voltage drop, the hold voltage, $V_H$, which is of the order of the material gap (0.5eV).

## III. Cell Performance

Figure 4 shows the programming characteristic of a PCM cell, that is the dependence of the cell resistance, R, as a function of the programming current. Filled symbols refer to the resistance obtained starting with a cell in the reset state. A 100ns programming pulse with different peak current value is applied and the resulting R value after programming is read at 0.2V. Before the subsequent measurement the cell is brought again in the initial reference reset state using a proper current pulse. Three different regions can be recognized: i) below 50μA, the device is off. The very small current does not provide any phase change. ii) In the 50-500μA range, the resistance decreases following the crystallization of the amorphous GST after switching. iii) Above 500μA the programming pulse melts some GST close to the GST-heater interface leaving it in the amorphous phase. The cell resistance therefore increases. Circles in Fig. 4 also shows the R-I characteristics obtained for the same cell, but starting from the set (crystalline) state. The resistance value changes only when the current exceeds 500μA, where the characteristic overlaps to the previous R-I. In conclusion, programming pulses of 500μA and 700μA make possible to switch the device between low and high-resistance states.

A simplified electro-thermal model [6] may help in understanding how to reduce the current consumption. At steady-state the temperature rise ΔT needed to reach the melting temperature in the active volume can be written as:

$$\Delta T = P R_{th},$$

where P is the power dissipated by Joule heating and $R_{th}$ is the total thermal resistance connecting the hot spot to the thermal sink at room temperature (metal layers). The power dissipated in the GST layer is $P=V_H I$, since the hold voltage $V_H$ is the voltage drop

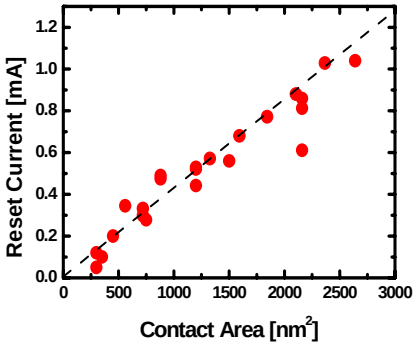


Fig. 5. Experimental scaling trend of the reset current in PCM cells as a function of the contact size.

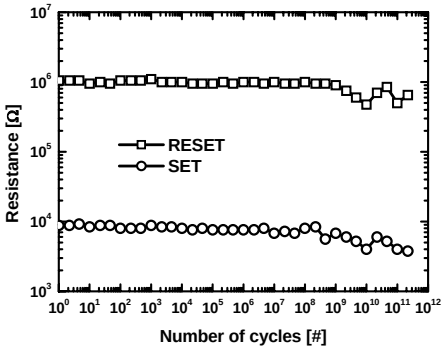


Fig. 6. Resistance of reset and set states measured under repetitive cycling.

across the chalcogenide layer in the conducting regime The required programming current is therefore:

$$I=\Delta T/(V_H R_{th}), \quad (1)$$

Since both $\Delta T$ and $V_H$ are physical quantities which do not scale, the programming current should scale as $1/R_{th}$, and can be optimized by accurate design of the bottom electrode. The major consequence of (1) is that, since $R_{th}$ is inversely proportional to the contact area A, the current should scale linearly with A. Data in Fig. 5 demonstrate the linear dependence on A down to a contact size of about 20nm [6].

If current consumption can be reduced by shrinking the contact area, endurance and retention has to be checked. Figure 6 shows the resistance of the set and reset states as a function of the programming cycles. Each program cycles included a 40-ns reset pulse and a 100-ns set pulse. A resistance window of a factor $10^2$ is retained over $10^{11}$ cycles, confirming the excellent stability of the programming characteristic and the extended endurance reliability with respect to the standard Flash technology. After $10^{11}$-$10^{12}$ cycles, the PCM cell fails featuring either a stuck-set (inability to reset the cell) or a stuck-reset (inability to set the cell) [7,8]. Both failures critically depend on the quality of the bottom interface, of the active layer and on possible inter-diffusion processes between GST and adjacent materials.

The most critical issue for a non-volatile memory is however data retention, that is the capability to retain the stored information during the memory lifetime. The reset state of the PCM is particularly sensitive from this standpoint, as the amorphous GST can spontaneously evolve towards the more stable crystalline phase. Figure 7 shows the Arrhenius plot for the failure time, defined as the time required to the resistance of a fully-reset cell to decay to half of its original value. The activation energy of 2.6eV corresponds to 10-years lifetime at the maximum temperature of 110°C.

A further concern for reliability is the program disturb. While a cell is being programmed, an adjacent amorphous cells can suffer a parasitic heating, which can result in data loss. Such a thermal crosstalk is also expected to become more critical as the device is scaled down. However, no signature of thermal cross-talk has been so far reported on memory arrays fabricated in 180-120nm technologies. Moreover numerical simulations have pointed out that cross-talk should not be an issue down to the 45-nm node [6]. Below the 45-nm node, interaction between adjacent bits may impose a cell spacing slightly larger than the feature size.

## IV. Cell Structures

Literature results are encouraging and supporting the feasibility of a competitive PCM technology. The first industrial results on PCM cells were presented by Intel-Ovonyx [3]. The cell structure was similar to the one presented in Fig.2 (*lance-like*). The size of the heater sets the cell programming current. The heater, usually made by TiN, adds some further joule heating and keeps the hot spot far from the cold contacts. Samsung, following the same lance-like approach, has demonstrated 64Mb arrays with MOSFET selectors, scaling progressively the reset current from the 2.0mA in the 240nm technology [9], to 600μA at the 120nm node with nitrogen-doped GST [10].

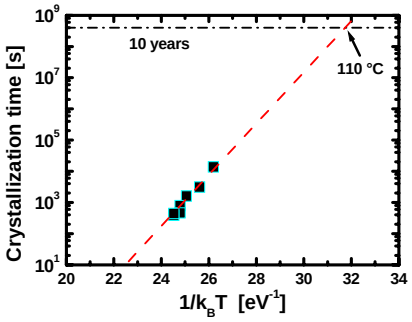


Fig. 7. Crystallization time of the reset state as a function of temperature. Retention up to 10 years requires operation below 110°C.

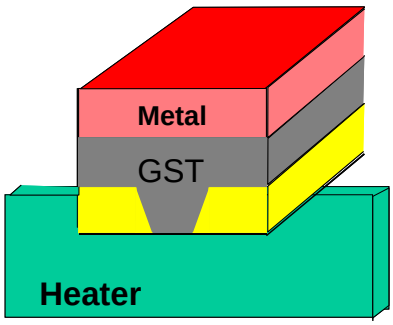


Fig. 8. Schematic view of a μtrench cell.

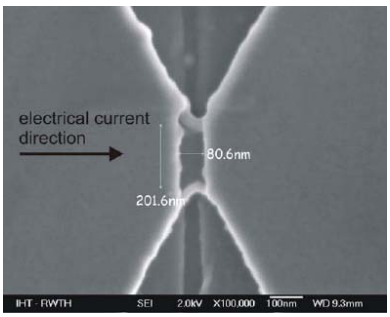


Fig. 10. Top view of planar PCM cell [13]

Reliable contact size control has been also demonstrated by STMicroelectronics with the so-called μtrench approach [11] (Fig. 8): the contact size is limited in one direction by the heater thickness (few-nm range), and by a sub-litho trench (few tens of nm) filled by GST in the other one. The μtrench PCM cell reaches a 600μA reset current at the 180-nm technology node. Fig. 9 shows the read current distributions for set and reset states within an 8Mbit μtrench PCM array. The program window is compatible with a high-density memory. Placing a read threshold at 15μA the information stored in the entire array can be correctly decoded.

Another possible cell geometry is the so-called *pore-like* structure. In this case the GST is deposited within a pore (in place of the heater in Fig.2). In this structure the hot-region is better confined by the surrounding insulating walls. The approach is critical from the processing standpoint since the GST has to be conformally deposited within a narrow feature, but it is capable to further reduce the programming current by about 50% [12].

The resistor can be also fabricated horizontally. Figure 10 shows the top view of a planar cell [13], consisting of a patterned GST layer with a bottleneck, where phase change occurs. This topology takes advantage of the distance between the phase-change volume, which is in the middle of the line, and the contacts at room temperature. By reducing heat diffusion towards the contacts, a lower programming current may be attained.

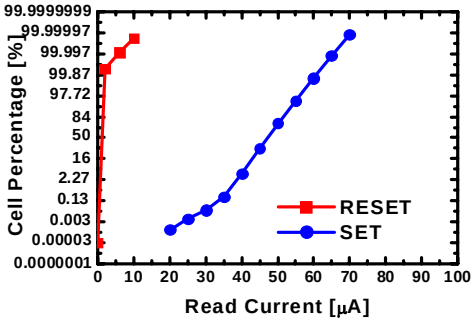


Fig. 9. Read current distribution within a 8Mb μtrench PCM array.

However, the need for two contacts makes this cell design hardly suitable for high-density applications. The same planar structure has been recently investigated at Philips Research [14] using Sb–Te doped with one or more elements from the series Ge, In, Ag, and Ga. Planar cells with 450μA/30ns programming current has been reported using chalchogenide lines 200nm long with $(20nm)^2$ cross section. These results may open the way to further investigations of performance trade-off in PCM devices using materials different from GST.

## V. Conclusions

The paper reviews the basic issues of current PCM technology discussing programming and reliability performance, cell structures and scaling perspectives. The development of a cell design compatible with writing, reliability, scalability and process integration requirements is under way. However results support the feasibility of a competitive PCM technology as non-volatile memory at the nanoscale.

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