Efficacy of the Thermalized Effective Potential Approach for Modeling Nano-Devices

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Abstract - **The efficacy of the thermalized parameter-free effective potential approach described elsewhere is examined with regard to its application to modeling of alternative device technologies. Our investigations suggest that the Hartree correction is significant only for very high doping densities, as it is the case in deca-nano MOSFETs. For low doping densities, as it is usually the case in alternative device structures, such as dual-gate and FinFET devices, the Hartree term can be neglected and the Barrier term needs to be included in the model only. Since the Barrier field is pre-calculated in the initialization stages of device simulation, it does not add any additional computational cost, thus leading to a very effective way of including quantum mechanical space-quantization effects in the computational model.**

I. INTRODUCTION

It is well known that scaling of nano-MOSFETs beyond the 15 nm node is a significant challenge from both fabrication and device operation point of view. As a result, proposals for alternative device structures have come up in the last few years that include ultra-thin body FETs, dual-gate structures, FinFETs, etc. All of these device structures have two key attributes in common: (1) the channel is either undoped or lightly doped, and (2) quantum-mechanical space quantization takes place in one or two spatial directions. One way of including quantum-mechanical space quantization effects into the computational model is via the solution of the corresponding effective mass Schrödinger equation. This is very time-consuming, however, because the Schrödinger equation has to be solved in slices along the channel and the corresponding scattering tables to be re-evaluated at each iteration step. An alternative to this approach, which has become very popular in recent years, is to use effective potentials [1] in conjunction with particle-based device simulations [2]. In this work, recently proposed thermalized effective potential approach by Ringhofer, Vasileska and Ahmed [3,4] has been used in investigating transport in dual-gate device structure proposed in Ref. [5] and briefly described in Section 2. Simulation results that test the range of validity of this model under certain approximate conditions are presented in Section 3. Details of the structure being simulated and the key results from our numerical experiments are described in Section 4. Conclusions drawn from this work are summarized in Section 5.

II. BRIEF DESCRIPTION OF THE THERMALIZED EFFECTIVE POTENTIAL APPROACH

In this work we utilize a new form of the effective quantum potential for use in Monte Carlo device simulators. The proposed approach is based on perturbation theory around thermodynamic equilibrium and leads to an effective potential which depends on the energy and wavevector of each individual electron, thus effectively lowering step-function barriers for high-energy carriers [3,4,6]. The quantum potential is derived from the idea that the Wigner and the Boltzmann equation with the quantum corrected potential should possess the same steady state. The resultant quantum potential is, in general, two-degrees smoother than the original Coulomb and barrier potentials, i.e. possesses two more classical derivatives, which essentially eliminates the problem of statistical noise.

The basic idea is that the total potential energy term can be represented as a sum of two potentials: the *barrier potential* $V_B(x)$, which takes into account the discontinuity at the Si/SiO_2 interface due to the difference in the semiconductor and the oxide affinities, and the *Hartree potential* $V_H(x)$ that results from the solution of the Poisson equation. The barrier potential is 1D and independent of time and needs to be computed only once in the initialization stage of the code. On the other hand, the Hartree potential is 2D and time-dependent as it describes the evolution of charge from quasi-equilibrium to a non-equilibrium state. Since the evaluation of the effective Hartree potential is very time consuming and CPU intensive, approximate solution methods have been pursued to resolve this term within a certain level of error tolerance.

III. VALIDATION OF THE APPROACH

To verify the validity of this new approach, self-consistent simulations of MOS capacitor structures have been performed and the reduction in the sheet electron density due to the band-gap widening effect is calculated. The simulation results from these investigations are shown in Figure 1. Notice the excellent agreement between the SCHRED (1D Schrödinger-Poisson solver) simulation data for the sheet

electron density and the simulation results obtained by utilizing the thermalized effective potential approach used in this work.

The next task in our simulation experiments was to examine the relative importance of the Barrier and the Hartree terms. For that purpose we also considered a prototypical MOSFET device and we varied the doping in the active channel region. The influence of the Hartree term on the on-state current for MOSFET devices with different doping densities is presented in Figure 2. We find that for low doping densities, the influence of the computationally expensive Hartree term is insignificant and can be omitted from the calculations. Whether the Barrier field alone can properly describe quantum-mechanical size quantization effects in undoped or lightly-doped devices is discussed next.

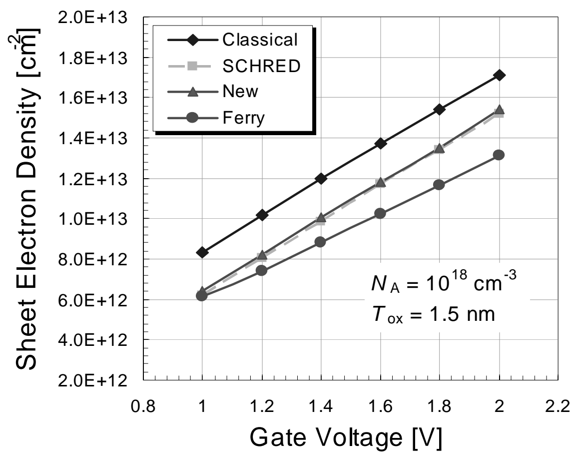


Figure 1: Variation of the sheet electron density versus gate voltage in a MOS capacitor structure.

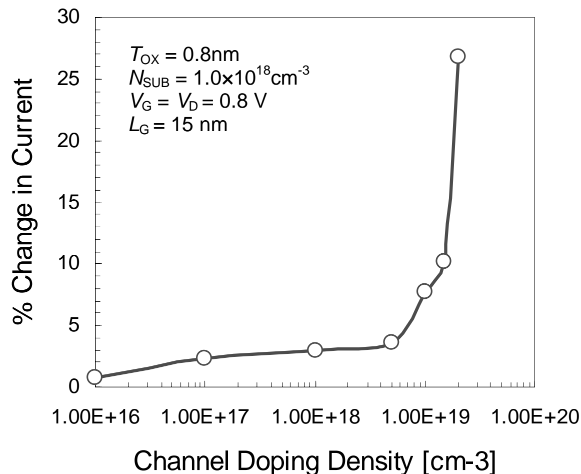


Figure 2: Importance of the Hartree Corrections.

Because of using lightly/nearly undoped channel region, size-quantization effects in nanoscale fully-depleted SOI devices find a major source in the very physical nature of the confined region which remains sandwiched between the two oxide layers. In order to verify the applicability of the quantum potential approach developed in this work, a single gated SOI device structure is studied first. Simulations are carried out to calculate the threshold voltage as a function of the silicon film thickness and the results are compared to other available methods. The SOI device used here has the following specifications: gate length is 40 nm, the source/drain length is 50 nm each, the gate oxide thickness is 7 nm with a 2 nm source/drain overlap, the box oxide thickness is 200 nm, the channel doping is uniform at 1×10^{17} cm^{-3}, the doping of the source/drain regions equals 2×10^{19} cm^{-3}, and the gate is assumed to be a metal gate with workfunction equal to the semiconductor affinity. There is a 10 nm spacer region between the gate and the source/drain contacts. The silicon (SOI) film thickness is varied over a range of 1–10 nm for the different simulations that were performed to capture the trend in the variations of the device threshold voltage. Similar experiments were performed in Refs. [7] and [8] using the Schrödinger-Poisson solver and Ferry's effective potential approaches, respectively. For comparison purposes, threshold voltage is extracted from the channel inversion density versus gate bias profile and extrapolating the linear region of the characteristics to a zero value. This method also corresponds well to the linear extrapolation technique using the drain current - gate voltage characteristics.

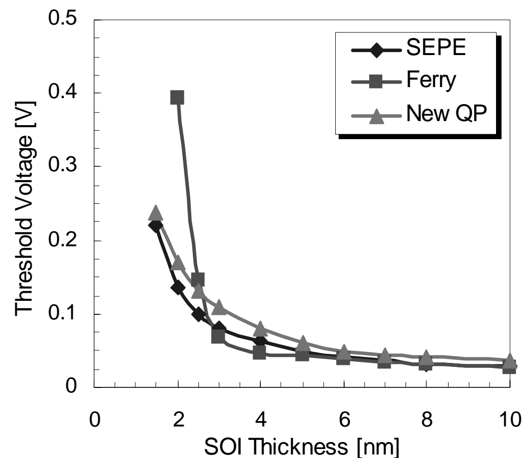


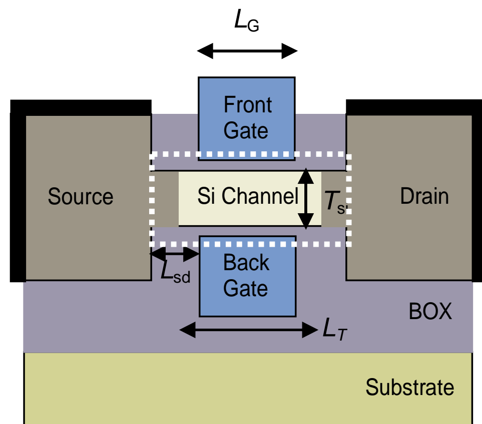
Figure 3: Threshold voltage variation with respect to the SOI film thickness.

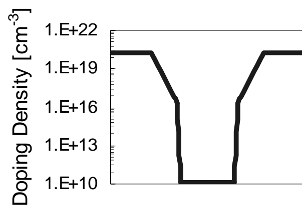
The result showing the trend in the threshold voltage variation with respect to the SOI film thickness is depicted in Fig. 3. One can see that Ferry's effective potential approach overestimates the threshold voltage for a SOI thickness of 3 nm due to the use of rather approximate value for the standard deviation of the Gaussian wave packet which results in a reduced sheet electron density. As the silicon film thickness decreases, the resulting confining potential becomes more like rectangular from combined effects of both the inversion layer quantization and the SOI film (physical) quantization, which also emphasizes the need for

using a more realistic quantum-mechanical wavepacket description for the confined electrons. Of most significant importance in this figure is the fact that the thermalized quantum potential approach is free from this large discrepancy and can capture the trend in the threshold voltage as obtained from the more accurate Schrödinger-Poisson solver. These results indicate that the new quantum potential method can be applied to the simulations of SOI devices with a greater accuracy and predictive capability as it will be seen from the results presented in the next section.

IV. SIMULATION RESULTS FOR THE DUAL GATE STRUCTURE

The double gate MOSFETs with 10nm channel length [9] have been designed for two purposes: (1) as a vehicle for examining device design/performance issues at the 10nm scale, and (2) as a computational benchmark for comparing the various advanced simulation tools that are being developed. "Well-Tempered" is Prof. Dimitri Antoniadis' term for a device that is designed to minimize electrostatic short-channel effects. The SOI device is a follow-up to the "Well-Tempered" Bulk-Si MOSFET project.





T_{ox} = 1 nm	T_{si} = 3 nm
L_G = 9 nm	L_T = 17 nm
L_{sd} = 10 nm	N_{sd} = 2 x 10^{20} cm^{-3}
N_b = 0	g = 1 nm/decade
Φ_G = 4.188	V_G = 0.4 V

Figure 4: Simulated DG SOI device structure.

Fig. 4 shows the simulated DG SOI device structure used in this study, which is identical to the devices reported in Refs. [9,10]. For quantum simulation purposes only the dotted portion of the device which has been termed as the *intrinsic* device is taken into considerations. The device was originally designed to achieve the ITRS performance specifications for the year 2016. The effective intrinsic device consists of two gate stacks (gate contact and SiO_2 gate dielectric) above and below a thin silicon film. For the intrinsic device, the thickness of the silicon film is 3 nm. Use of a thicker body reduces the series resistance and the effect of process variation, but it also degrades the short channel effects (SCE). From SCE point of view, a thinner body is preferable but it is harder to fabricate very thin films of uniform thickness, and the same amount of process variation (±10%) may give intolerable fluctuations in the device characteristics. A thickness of 3 nm seems to be a reasonable compromise, but other body thicknesses are also examined. The top and bottom gate insulator thickness is 1 nm, which is expected to be near the scaling limit for SiO_2. As for the gate contact, a metal gate with tunable workfunction, Φ_G, is assumed, where Φ_G is adjusted to 4.188 to provide a specified off-current value of 4 μA/μm. The background doping of the silicon film is taken to be intrinsic, however, due to diffusion of the dopant ions, the doping profile from the heavily doped S/D extensions to the intrinsic channel is graded with a coefficient of g which equals to 1 nm/dec. For convenience, the doping scheme is also shown in Fig. 4. According to the roadmap, the high performance (HP) device should have a gate length of L_G = 9 nm at the year 2016. At this scale, two-dimensional (2D) electrostatics and quantum mechanical effects both play an important role and traditional device simulators may not provide reliable projections. The length, L_T, is an important design parameter in determining the on-current, while gate metal workfunction, Φ_G, directly controls the off-current. The doping gradient, g, affects both on-current and off-current. Values of all the structural parameters of the device are shown in Fig. 4.

The intrinsic device is simulated using the new quantum potential approach in order to gauge the impact of size-quantization effects on the DG SOI performance. The results are then compared to that from a full quantum approach based on the non-equilibrium Green's function (NEGF) formalism (NanoMOS–2.5) developed at Purdue University. In this method, scattering inside the intrinsic device is treated by a simple Buttiker probe model, which gives a phenomenological description of scattering and is easy to implement under the Greens' function formalism. The simulated output characteristics are shown in Figure 5.

Devices with both 3 nm and 1 nm channel thickness are used with applied gate bias of 0.4 V. The salient features of this figure are as follows: (1) Even with an undoped channel region, the devices achieve a significant improvement with respect to the short channel effects (SCEs) as depicted in flatness of the saturation region. This is due to the use of the two gate electrodes and an ultra-thin SOI film which makes the gates gain more control on the channel charge. (2) Reducing the channel SOI film thickness to 1 nm further reduces the SCEs and improves the device performance. However, the reduction in the drive current at higher drain biases is due to series resistance effect pronounced naturally when the drain current increases. (3) Regarding the quantum effects, one can see that quantum-mechanical size quantization plays not a very dominant role in degrading the device

drive current mainly because of using an undoped channel region. Also, looking at the 3 nm (or 1 nm) case alone one can see that the impact of quantization effects reduces as the drain voltage increases because of the growing bulk nature of the channel electrons. (4) Percentage reduction in the drain current is more pronounced in 1nm case throughout the range of applied drain bias because of the stronger physical confinement arising from the two SiO_2 layers sandwiching the silicon film. (5) Finally, the comparison between the quantum potential formalism and the NEGF approach for the device with 3 nm SOI film thickness shows reasonable agreement which further establishes the applicability of this method in the simulations of different technologically viable nanoscale classical and nonclassical MOSFET device structures.

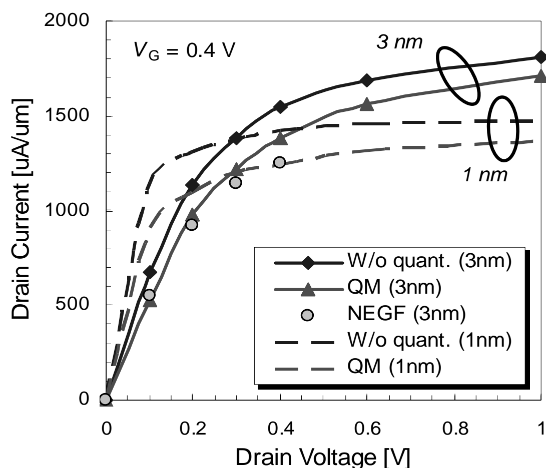


Figure 5: Generic DG SOI device output characteristics.

V. CONCLUSION

In this work a thermalized effective potential approach has been utilized in modeling of dual gate structures. Our validation simulations of the approach demonstrate that there is an insignificant current degradation due to the Hartree part of the quantum correction in devices without or very low substrate doping. This has been used as a sufficient argument to perform device simulations of dual gate structures in which only the Barrier potential is taken into consideration. Excellent agreement has been obtained with our Effective Potential Monte Carlo device simulations data and the results that utilize the NEGF formalism. It is important to note, however, that the Barrier field used in the free-flight portion of the simulator, is precomputed and stored when we do the initialization of the program and, as such, does not add any additional computational cost to the simulations.

ACKNOWLEDGEMENTS

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