Linearity Analysis of RF LDMOS Devices Utilizing Harmonic Balance Device Simulation

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***Abstract* – Linearity is one of the most important characteristics for current and next-generation RF power devices for wireless communication. In this work, linearity of power LDMOS devices is analysed by using a unique harmonic balance device simulator. Sweet-spots in the third order intermodulation distortion product (IM3) are explained and found to be in agreement with measurements and compact modeling. For demonstration of the simulation methodology, a change in the lightly doped drain (LDD) region doping concentration was performed and the effect on linearity was analysed.**

I. INTRODUCTION

Linearity is one of the most important concerns for power amplifiers in third-generation (3G) wireless systems and is expected to become even more important in the future. A lot of effort is being put into linearization of amplifiers at different levels, from device design and circuit-techniques up to system-level with correction techniques such as feedforward and digital predistortion. A significant amount of work has been put into empirical modeling of different devices on a circuit-level. However, up to now analysis of the distortion generated by the device itself and its relation to different device design parameters have been fairly limited [1-4]. In this paper, we demonstrate that harmonic balance device simulation can be used for improved understanding and analysis of linearity in radio frequency (rf) power devices. The tool used is a unique harmonic balance (hb) device simulator [1] with the capability of including external circuitry [2]. Variations in for instance doping profiles are directly reflected in the final large-signal RF performance and detailed design changes or completely new device designs can therefore be investigated and analysed in depth. In this study, we will start by analyzing a small LDMOS test structure without any internal or external matching. To separate the influence of nonlinearities in static IV-characteristics from nonlinearities in intrinsic capacitances, simulations will first be performed at low frequencies, and as a second step, frequency is increased to take capacitances into account. Finally, a full-sized die with low impedance and including internal and external in- and output matching and surrounding test circuitry will be simulated.

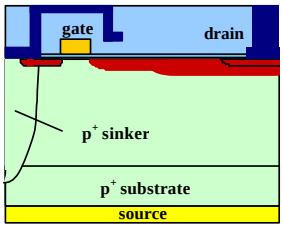

Fig. 1 Schematic cross-section of Infineon 2.1 GHz 45 W LDMOS device.

II. DEVICE STRUCTURE AND OPERATION

Fig. 1 shows a schematic cross-section of the Infineon 2.1 GHz 45 W LDMOS device (Infineon product PTF210451) used in this study. It has two different lightly doped drain regions for optimization of on-resistance and breakdown voltage. A Faraday shield is used to optimize low feedback capacitance (Cdg), high breakdown voltage and suppressed hot carrier injection into the gate oxide. The source is contacted to the backside through a deep p^+ sinker for low parasitic resistance and inductance, which is critical for the rf performance of the device. The device geometry and doping profiles used in the hb device simulations were extracted from process simulation of the actual manufacturing process in the fab. Fig. 2 shows simulated IdVgs-characteristics at Vds=28 V for a small device with

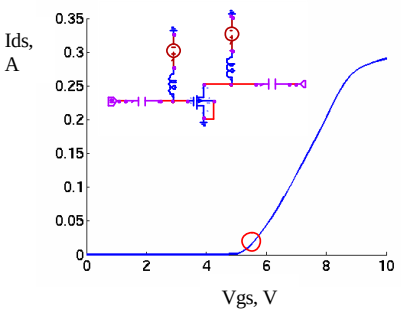

Fig. 2 IdVgs-characteristics and selected bias point for class AB operation indicated; insert shows simple test circuit used in the first phase of this study.

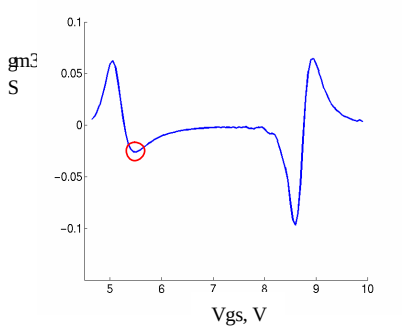

Fig. 3 gm3, third order derivative of IdVgs-characteristics at Vds=28 V.

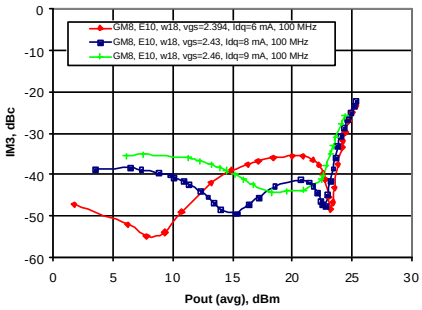

Fig. 5 Double sweet-spots from measurements on 1.2 mm test structure. Vgs=2.394 (♦ red), Vgs=2.43 (▪ blue) and Vgs=2.46 (+ green). f=100 MHz.

1.2 mm gate periphery. The inset shows the simple test circuit used in the first phase of this study, consisting of input and output blocking capacitors, RF chokes, gate and drain bias supplies. The device is biased slightly above threshold (indicated by circle in fig. 2) in class AB operation; this has been found to give the best trade-off between linearity and efficiency in wireless and broadcasting applications and is standard in the industry.

III. LINEARITY AND SWEET-SPOTS

Fig. 3 shows gm3, third-order derivative of the IdVgs-characteristics at Vds = 28 V from device simulation; the circle indicates the selected bias point for class AB operation (compare with fig. 2). This characteristic is important in determining where the nulls of the third-order intermodulation product (IM3), so-called 'sweet-spots', are generated during large-signal operation. Depending on the choice of bias point (class of operation) along the gm3 curve, different patterns can be identified [5,6]. For LDMOS, if the device is biased with a negative gm3 slightly above threshold in class AB operation, IM3 will switch signs and go through a null, a so-called sweet-spot as the device traverses the expanding non-linearity of the turn-on region [5]. The expanding non-linearity of the turn-on region needs to be strong enough to create this sweet-spot and is not always seen in FET devices, which usually exhibit softer turn-on characteristics. By increasing the power further, the signal will eventually reach the compressing non-linearity of the transfer function (compare fig. 2) and IM3 will switch signs again, creating a second sweet-spot. Fig. 4 shows these two-sweet-spots from harmonic balance device simulation. It is also indicated how the first sweet-spot moves as a function of bias in class AB operation. For a higher Vgs, or in other words a higher quiescent current (Idq) setting, the sweet-spot moves to the right since more input power is required for the signal to arrive at the expanding non-linearity of the turn-on region for creation of the IM3 null. This is in agreement with measurements. Fig. 5 shows measured data on a 1.2 mm test structure for different Idq settings. The relatively large absolute difference in threshold voltage between the measurements and the hb device simulations can be attributed to the fact that measured data is on a device that is more advanced in technology development and to some uncertainty in the extraction of doping profiles from process simulation. It is clear that the first sweet-spot moves with bias, very much in agreement with the hb device simuations. It is also noted that by proper biasing, the two sweet-spots can be made to merge into one (green curve), thereby creating improved linearity over a wider power range. The location of the first sweet-spot is very sensitive to bias and this is also the experience when optimizing linearity for a given product at high frequencies. It is highly desirable to operate around a deep and wide sweet-spot in an application for low distortion and maximum efficiency for a given linearity.

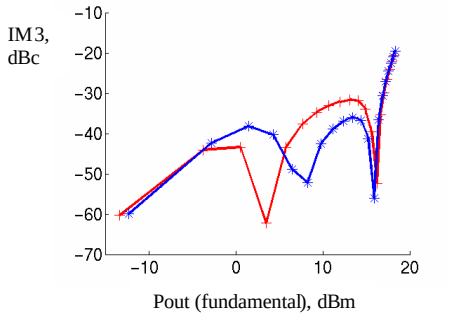

Fig. 4 Double sweet-spots for studied LDMOS device from harmonic balance device simulations. Vgs=5.45 V (+ red) and Vgs=5.5 (* blue). f=10 MHz

Fig. 6a shows results of hb device simulations at frequencies 10 MHz, 1 GHz and 2 GHz. It is noted that both sweet-spots are smoothed out at higher frequencies, induced by non-linearities in capacitances. Fig. 6b shows corresponding measured data on a 1.2 mm test structure. The qualitative behavior is very similar. Additionally, fig. 6c shows results using a calibrated compact electrothermal model [7] and it also agrees qualitatively very well with the hb device simulations and the measurements.

As an example of how changes in device design parameters affect rf performance, the doping of the lightly doped drain region (LDD1) was decreased from 9e16 cm^{-3} to 5e16 cm^{-3}. This leads to a higher on-resistance and earlier quasi-saturation and pinch-off in the LDD region [8]. Fig. 7 shows the difference in IdVds-characteristics for the two

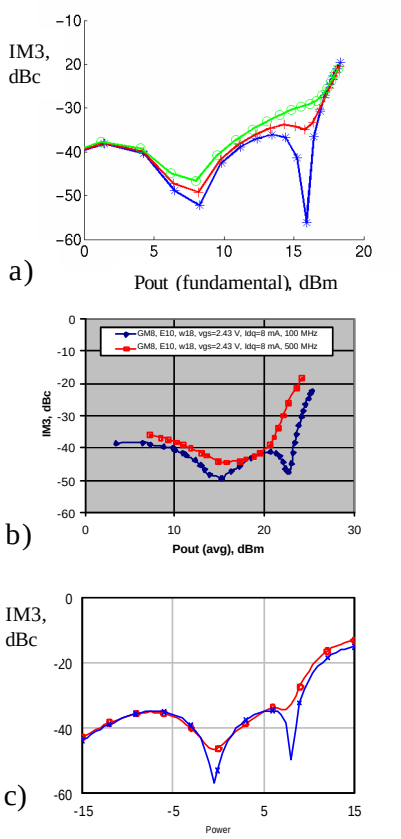

Fig. 6 Double sweet-spots in IM3 for varying frequencies. a) hb device simulation. 10 MHz (* blue), 1 GHz (+ red) and 2 GHz (o green). b) measured data on 1.2 mm test structure. 100 MHz (♦ blue) and 500 MHz (¦ red). c) compact modeling. 100 MHz (+ blue) and 500 MHz (o red).

cases; a schematic load-line is also indicated. Simulation was performed at low frequency for ease of interpretation. Fig. 8 shows the resulting IM3 as a function of output power (for one fundamental tone). We notice that only the second sweet-spot is affected and that its location moves up in power. This is consistent with the previous arguments, since only the compressing non-linearity in the upper part of the transfer function is affected by this device design change. The lower LDD1 doping concentration leads to an earlier compressing non-linearity and earlier clipping of the waveform as the power and signal swing increase. Threshold voltage and gm in the lower part of the characteristics are not affected. This is an interesting result, since it shows that the linearity in the important back-off region not necessarily improves by expanding the linear region of the transfer function of the device. In an optimized case, the two sweet-spots may interact to create one deep and wide sweet-spot as discussed earlier and separating them by moving the second sweet-spot up in power might degrade linearity in the region in between. However, by doing so, the device size can be scaled down and still achieve the same required output power. This means that the intrinsic capacitances, in particular the critical feedback capacitance Cdg,

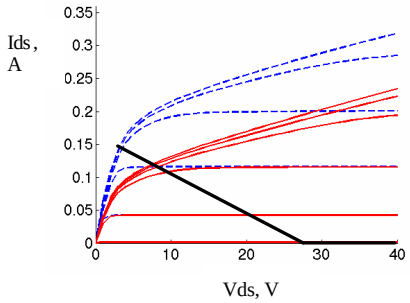

Fig. 7 Simulated differences in IdVds-characteristics for ldd1 doping concentration 9e16 cm^{-3} (dotted blue lines) and ldd1 doping concentration 5e16 cm^{-3} (solid red lines). Schematic load-line indicated by black solid line.

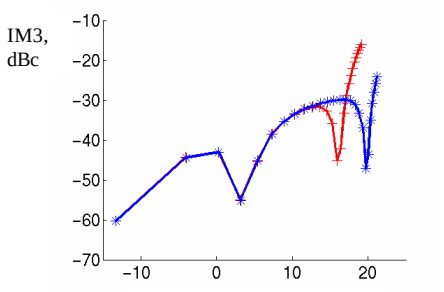

Fig. 8 Differences in IM3 characteristics for ldd1=9e16 cm^{-3} (* blue) and ldd1=5e16 cm^{-3} (+ red).

will scale down accordingly, which can indirectly lead to an improvement in linearity and backed-off efficiency in a real application at high frequencies. In other words, by proper choice of biasing and die size, linearity and backed-off efficiency can be optimized for a given application and linearity requirement.

IV. HB DEVICE SIMULATION FOR REAL APPLICATIONS

To demonstrate the capability of the simulation methodology, a 2.1 GHz 45 W product (Infineon product PTF210451) was simulated including internal and external matching and test circuitry. A schematic of the test circuit is shown in fig. 9. It includes external matching and bias feed networks. The s-parameters of the lossy transmission lines were fitted individually to a set of lumped representations consisting of series inductance L, series resistance R and shunt capacitance C, shunt conductance G by optimization [9] and were fed into the hb device simulator. The frequency-dependence of the bias network impedances, that can lead to asymmetries in the intermodulation distortion products [10], are also included.

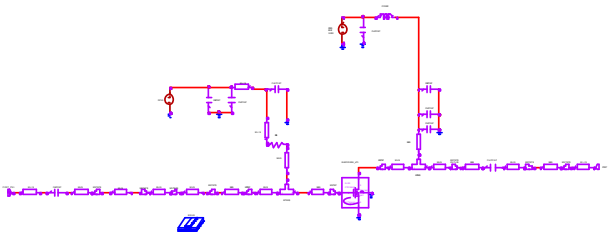

Fig. 9 Schematic of test circuit for PTF 210451 including external input and output matching and gate and drain bias circuitry.

Fig. 10 shows resulting IM3 as a function of output power (one fundamental tone) at 2.1 GHz. It shows the typical behavior seen in measurements on the test bench with one sweet-spot and positive slopes for low and high powers. By changing detailed device design parameters, influence on the large-signal rf performance of a final product can be predicted.

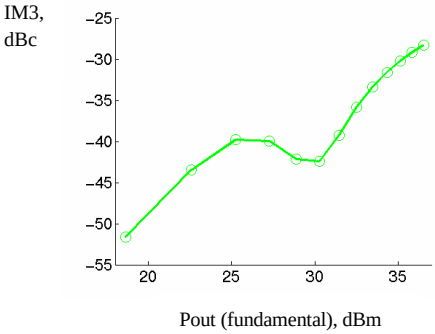

Fig. 10 IM3 as a function of output power (for one fundamental tone) for PTF210451 including internal and external input and output matching and test circuitry.

V. CONCLUSIONS

In summary, it was shown that linearity of rf power LDMOS devices can be analysed in depth by using a unique harmonic balance device simulator. Sweet-spots in the third order intermodulation distortion product (IM3) were explained and found to be in agreement with measurements and compact modeling. To demonstrate the effect of varying device design parameters, a change in the lightly doped drain (LDD) region doping concentration was performed and the effect on linearity was analysed. The demonstrated analysis and simulation techniques helps in laying ground-work for improved device design and investigation of new device concepts for improved linearity.

ACKNOWLEDGEMENTS

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References:

[1] B. Troyanovsky, "Frequency Domain Algorithms for Simulating Large Signal Distortion in Semiconductor Devices", PhD-thesis, ICL 97-080, Stanford University, 1997.

[2] F. Rotella, PhD-thesis, ICL 00-095, Stanford University, 2000.

[3] F. Rotella, G. Ma, Z. Yu and R.W. Dutton, "Modeling, Analysis and Design of RF LDMOS Devices Using Harmonic Balance Device Simulation, IEEE Trans. Microwave Theory and Techniques, vol. 48, no. 6, June 2000.

[4] J. Sato-Iwanga, K. Fujimoto, H. Masato, Y. Ota, K. Inoue, B. Troyanovsky, Z. Yu and R.W. Dutton, "Distortion Analysis of GaAs MESFETs based on physical model using PISCES-HB", *IEDM Techn. Dig.*,pp. 163-166, Dec. 1996.

[5] N.B. De Carvalho, J.C. Pedro, "Large- and small-signal IMD behaviour of microwave power amplifiers, *IEEE Trans. Microwave Theory and Techniques*, vol. 47, no. 12, Dec. 1999.

[6] C. Fager, J.C. Pedro, N.B. de Carvalho and H. Zirath, "Prediction of IMD in LDMOS Transistor Amplifiers Using a New Large-Signal Model, *IEEE Trans. Microwave Theory and Techniques*, vol. 50, no. 12, Dec. 2002.

[7] O. Tornblad and C. Blair, "An Electrothermal BSIM3 Model for Large-Signal Operation of RF LDMOS Devices", *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 861-864, 2002.

[8] J. Jang, O. Tornblad, T. Arnborg, Q. Chen, K. Banerjee, Z. Yu and R.W. Dutton, "RF LDMOS Characterization and its Compact Modeling", *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 967-970, 2001.

[9] Microwave Office Simulator ver 6.02, Applied Wave Research.

[10] S. Cripps, "Advanced Techniques in RF Power Amplifier Design", Artech House 2002.