Analysis and Simulation of Self-Heating Effects on RF LDMOS Devices

M. A. Belaïd, K. Ketata, H. Maanane, M. Gares, K. Mourgues, J. Marcon
LEMI, University of Rouen, IUT Rouen, 76821, Mont Saint Aignan, France
E-mail : Mohamed-ali.Belaid@univ-rouen.fr

Abstract **- This paper presents a study of the temperature and self heating effects on RF LDMOS devices. A new electro-thermal model is implemented in Agilent's ADS, using a Symbolic Defined Device (SDD). The proposed model takes into account the thermal effects and the influence of temperature on the I-V and C-V characteristics, by providing three thermal resistances and three thermal capacitances, which represent the heat flow from the chip to the ambient air (thermal network). The new model is thoroughly assessed against extensive 2-D simulations performed using a numerical device model. The results indicate a good agreement with all operating conditions.**

I. INTRODUCTION

The current tendency in microelectronic industry is to the down scaling of electronic components leading to power increase. This means that thermal effects must be taken into account both in the design as well as in the exploitation [1]. It is known that the temperature reached by the power device under operation exercises has a considerable influence on reliability and performances [2], which can modify and degrade transistor behavior. The temperature is one of the critical parameters in particular RF power electronic devices and many properties of these devices are strongly dependent on temperature. This element can limit the lifetime of semiconductors and plays an essential part in failure mechanisms [3].

The channel current models based on analytic expressions, have been reported by Miller et al. (Motorola model) [4] and Angelov et al. (Chalmers model) [5] and have shown further good results. Nevertheless, the new model proposed in this paper has additional advantages. It is based on three cells representation (thermal network), from the chip to the ambient air, in order to fully describe the normal RF LDMOS I–V and C-V curves and to obtain a characterization able to evaluate the temperature variation and the self-heating effects during LDMOS operation. These results are compared and proved by a numerical simulation analysis (Silvaco-Atlas, 2D).

II. RF LDMOS EXPERIMENTAL CHARACTERISATION

It is essential to characterize RF LDMOS in order to extract model parameters. A commercial Philips RF LDMOS has been used for this study. The main characteristics of this device are as follows: frequencies up to 2 GHz, output power of 10 Watts, breakdown voltage of 75 V. I-V and C-V measurements were performed, respectively, by an Agilent E5270 DC analyser and HP 4194A impedance analyser, piloted by IC-CAP Agilent software. Special attention was paid to the fact that the RF LDMOS is a power device, so it heats up at high bias. The method presented is based on a comparison of I-V and C-V characteristics of the transistor in various conditions (chip, package, heat sink, different temperatures) with the same component. This type of measurement is a necessary step before the modeling approach. The main interest is to inform us about the component's behavior in its various operating modes (linearity, saturation...). From these different characteristics, we can deduce the channel current, the threshold voltage, forward transconductance, on-state resistance, capacitances, etc.

Fig. 1 (line) shows the instability and the thermal runaway which occurred due to self-heating effects. To limit and decrease this problem and to improve the measurement conditions, a solution which proves to be a precious working tool would make it possible to stabilize the self-heating effects and to thermal protect the component. It consists of mounting the component on a heat dissipator (a heat sink or a Peltier module). Thanks to this solution, we can obtain more thermally stable measurement conditions (Fig. 1, dashed).

III. ELECTRO-THERMAL MODEL

In this part, we present a new electro-thermal model for power RF LDMOS transistors that can take into account self-heating and thermal effects. It has been implemented in Agilent's ADS software using a Symbolic Defined Device (SDD), by providing a more accurate and flexible model, from the chip to the ambient air. The empirical nonlinear model is shown in Fig. 2. This single-piece model is continuously differentiable and includes thermal dependencies. It is able to represent accurately the current-voltage characteristics and their derivatives at any bias point and operating temperature. A commonly adopted approach, originally proposed by Székely and Tarnay [6], is to couple the electrical circuit to a suitable thermal network modeling the self-heating and the thermal phenomenon. The ability to analyse the two coupled phenomena is consequently becoming a key point for a reliable and accurate design. The expression for the instantaneous junction temperature of the transistor was developed by making use of the existing duality [7] between heat transfer and electrical phenomena.

The power RF LDMOS model consists of several lumped passive linear components, nonlinear capacitances, nonlinear current source, and an additional thermal circuit, as shown in Fig. 2. In the model, the channel current depends on the gate–source and drain–source voltages. This is significant because it introduces the nonlinear behavior of the component [8]. A set of static thermal equations governing the electro-thermal behavior of the drain-to-source non-linear current and the associated model parameters has been developed [4,8]. These equations take

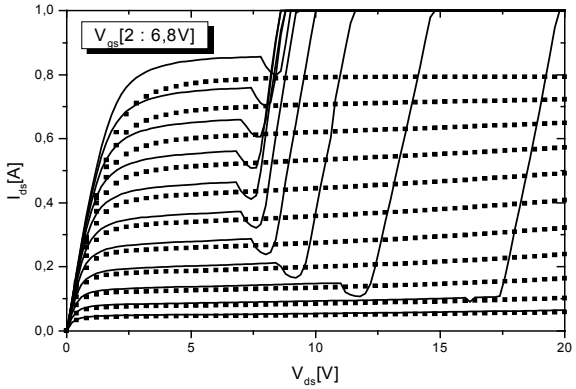

Fig. 1. Output characteristics: Thermal instability effect (line) and stable temperature conditions (dashed).

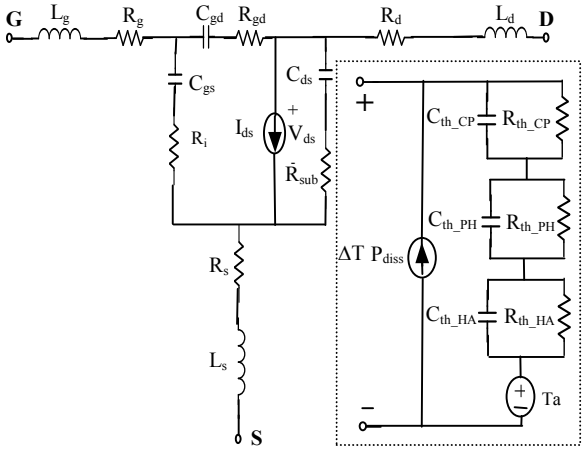

Fig. 2. Large-signal equivalent circuit of the power RF LDMOS model with a thermal circuit including three cells.

into account the non-linear drain current and the temperature dependent parameters at different conditions of heat dissipation, that also reflects various temperature values. The proposed channel current model is formulated as follows [8,9]:

$$I_{ds} = \text{Beta}\cdot\left(V_{gm}^{Vg\,exp}\right)\cdot\left(1+\text{Lmabda}\cdot V_{ds}\right)\cdot\tanh\left[\frac{\left(V_{ds}\cdot\text{Alpha}\right)}{V_{gm}}\right]$$
$$\cdot\left[1+K_1\cdot\exp\left(V_{breff1}\right)\right] \quad (1)$$

$$V_{gm} = V_{ST}\cdot\ln\left[\exp\left(\frac{V_{gm1}}{V_{ST}}\right)+1\right] \quad (2)$$

$$V_{gm1} = V_{gm2}-\frac{1}{2}\left[V_{gm2}+\left(\sqrt{\left(V_{gm2}-V_K\right)^2+\text{Delta}^2}\right)-\left(\sqrt{V_K^2+\text{Delta}^2}\right)\right] \quad (3)$$

$$V_{gm2} = -V_t+\left(\text{Gamma}\cdot V_{ds}\right) \quad (4)$$

$$V_{breff\,1} = \frac{1}{K_2}\left(V_{ds}-V_{breff}\right)+M_3\left(\frac{V_{ds}}{V_{breff}}\right) \quad (5)$$

$$V_{breff} = \frac{V_{br}}{2}\left[1+\tanh\left(M_1-V_{gm}\cdot M_2\right)\right] \quad (6)$$

$$V_{br} = V_{br0}+\left(V_{brT}\cdot\Delta T\right) \quad (7)$$

The main significant parameters of the model are shown in Table1. The threshold voltage and the effective mobility are sensitive to the junction temperature [8]. Hence, we take V_t and Beta to be the temperature dependent parameters. The two parameters are depicted as shown in the following equations, to provide range restriction (i.e., always positive) to the parameters:

$$V_t = V_{t0}+\left(V_{tT}\cdot\Delta T\right) \quad (8)$$

$$\text{Beta} = \text{Beta}_0+\left(\text{Beta}_T\cdot\Delta T\right) \quad (9)$$

The new thermal network of the power RF LDMOS shown in Fig. 2 represents a low-pass circuit with shunting R_{th_CA} and C_{th_CA}. The R_{th_CA} is correlated to static characteristics, while C_{th_CA} represents the dynamic characteristics of the channel current with temperature variation behavior of the heat flow inside the transistor. From the thermal circuit given in Fig. 2, the static channel temperature can be written as below:

$$\Delta T = R_{th\_CA}\cdot P_{diss}+T_a \quad (10)$$

$$P_{diss} = I_{ds}\cdot V_{ds} \quad (11)$$

$$R_{th\_CA} = R_{th\_CP}+R_{th\_PH}+R_{th\_HA} \quad (12)$$

Where ΔT is the junction temperature, T_a the ambient temperature, P_{diss} is the total instantaneous power dissipated in the transistor, R_{th_CP} the thermal chip-package resistance (a technological characteristic specific to a transistor and given by the manufacturer), R_{th_PH} the thermal package-heat sink resistance (referring to a conduction transfer; this resistance can be decreased by improving the contact between the package and the heat sink surface, by using silicone oil), R_{th_HA} the thermal heat sink-ambient air resistance (depending not only on the size, form and structure of the heat sink, but also on its orientation and on the air stream flowing around it).

Table 1. Model parameters.

Parameter	Definition	Unit
Beta	Transconductance parameter	Siemens
V_t	Threshold voltage	V
Delta	Vt variation according to V_{ds}	V
V_{br}	Break down voltage	V
$K_{1/2}$,$M_{1/3}$	Break down parameters	--
V_K	I_{ds} equation coefficient	V
Alpha	Linear range	1/Ω
Gamma	Slope of the channel current	--
Lambda	Shapes of the I_{ds} saturation	1/V
V_{gexp}	Term of power	--
V_{ST}	Sub-threshold slope coefficient	V

For C-V characteristics, the functions of non-linear capacitances C_{gs} (gate–source capacitance), C_{gd} (gate–drain capacitance) and C_{ds} (drain–source capacitance) used in this modeling are as follows with linearized temperature dependence, where $C_{gs1\text{-}gs6}$, $C_{gd1\text{-}gd4}$ and $C_{ds1\text{-}ds3}$ are the equations coefficients respectively, of $C_{gs,}$ C_{gd} and C_{ds}:

$$C_{gs}\left(T\right) = \left(C_{gs1}+C_{gs2}\cdot\left[1+\tanh\left(C_{gs6}\cdot\left(V_{gs}+C_{gs3}\right)\right)\right]+C_{gs4}\right.$$
$$\left.\cdot\left[1-\tanh\left(V_{gs}\cdot C_{gs5}\right)\right]\right)\cdot\left(1+C_{gs}\cdot\Delta T\right) \quad (13)$$

$$C_{gd}(T) = \left[C_{gd1} + \left(C_{gd2} / \left(1 + C_{gd3} \cdot \left(V_{gd} - C_{gd4}\right)^2\right)\right)\right] \cdot \left(1 + C_{gd} \cdot \Delta T\right) \quad (14)$$

$$C_{ds}(T) = \left[C_{ds1} + \left(C_{ds2} / \left(1 + C_{ds3} \cdot V_{ds}^2\right)\right)\right] \cdot \left(1 + C_{ds} \cdot \Delta T\right) \quad (15)$$

The physical equations for I-V and C-V characteristics and their dependence temperature are detailed in Atlas manual [10].

IV. RESULTS AND DISCUSSION

In conventional MOS transistors, the highest current density is located in the channel region. Therefore, the most extensive power dissipation occurs in the channel [1]. In addition, the rise of temperature is considerably larger when the device is operating in saturation, as a result of higher power dissipation than in the case of a device operating in the linear region [2]. Maximum temperature is observed in the channel pinch-off region because of maximum current density [2]. The I-V characteristics of the transistor in various conditions (chip, package, heat sink) and the fitted results are in good agreement as shown in Fig. 3. Different levels of heat dissipation are presented which describes the temperature variations in the component.

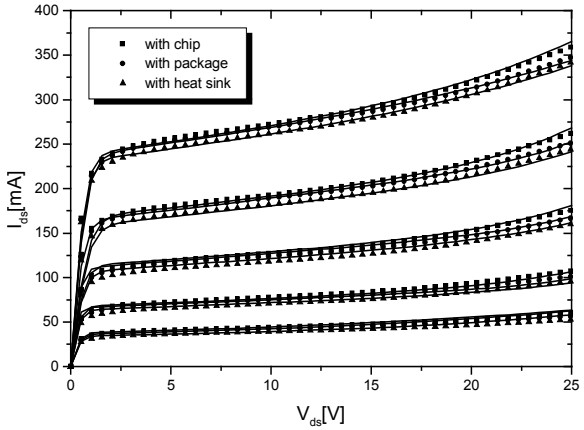

Fig. 3. Measured (dashed) and modeled (line) output characteristic at various conditions, V_{gs}=[3 : 6V], step=600mV.

These techniques also deal with the same phenomenon studied by Y. Yang [11] in pulsed (long and short pulse) and in DC characterization. This explains the different means of component dissipation power, by using a cooling system in the case of DC characterization or exploiting pulse width to avoid heat rise in the case of pulsed characterization [12]. A self-heating effect has been observed and simulated in Fig.4. Therefore, a model that represents the temperature rise due to self-heating is essential for reliable results. It increases when a voltage is applied (drain voltage and gate voltage) in the device. Knowledge of the temperature distribution inside the structure and in particular in the conduction channel and thus in the drift area, is necessary to identify local "hot spots" (Fig. 5). The self-heating effect is estimated by using physical simulation software (Silvaco-Atlas, 2D). However, the non-uniform distribution of dissipated power has been observed and is located in the drift region. It is caused by the breakdown effect and can lead to thermal runaway, if the rise in channel temperature is high enough. As in other power devices, the temperature rise due to device self-heating takes place inside the LDMOS active area, thus degrading the static and dynamic electrical characteristics of the device and finally altering the performance to a considerable extent [8]. Besides the electro-thermal modeling improvement, accurate prediction of the temperature in the source/drain/channel

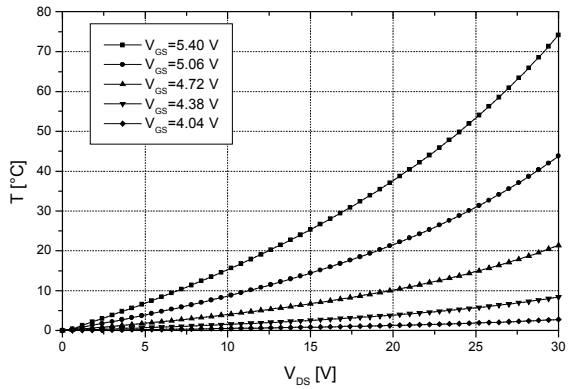

Fig. 4. ADS simulation of the temperature inside the chip, for DC biased condition.

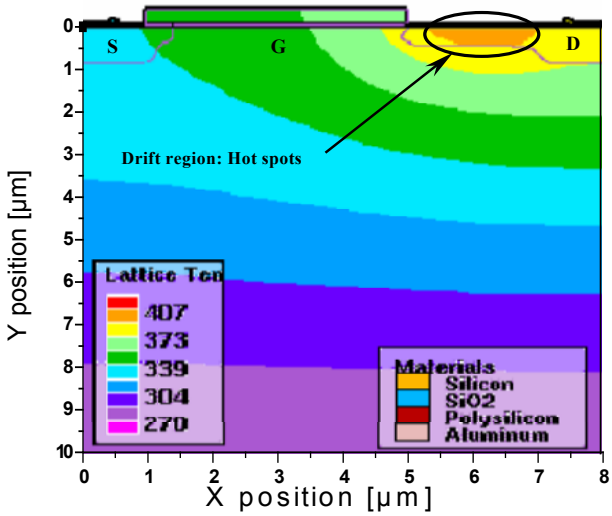

Fig. 5. Distribution of power dissipation and temperature rise within the RF LDMOS at T_a: V_{gs} =8V, V_{ds} =30V.

is also desirable for a reliability study. Indeed, the failure rate depends on the temperature, as previously reported in [1,11]. Moreover, information on temperature increase is crucial to understanding the failure mechanisms in the device. The temperature rise increases the drain current due to the reduced threshold voltage at a low current region and decreases it due to the effective mobility degradation at a high-current region [8]. These results are confirmed by numerical simulations as shown in Fig. 6.

The C-V characteristics of the transistor in various temperature and the fitted results form IC-CAP plot optimiser are in good agreement, as presented in Figs. 7 and 8. The temperature influence is confirmed by numerical simulations (Fig. 9 and 10). The variation of this could be explained by the effect of the temperature on the Fermi level, which affects thereafter the width of the space charge zone and induce the variation of capacitance value.

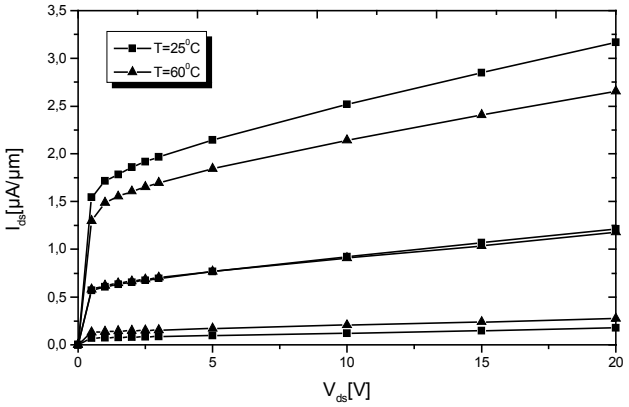

Fig. 6. Output characteristic obtained from a numerical simulation (Silvaco-Atlas) at different T_a: V_{gs} =[1:5V].

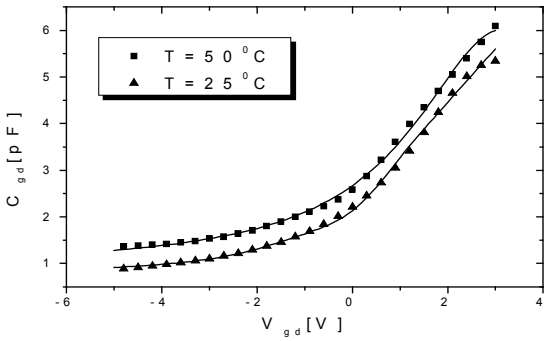

Fig. 7. Measured (dashed) and modeled (line) gate-drain capacitance at different T_a, with Freq=1Mhz

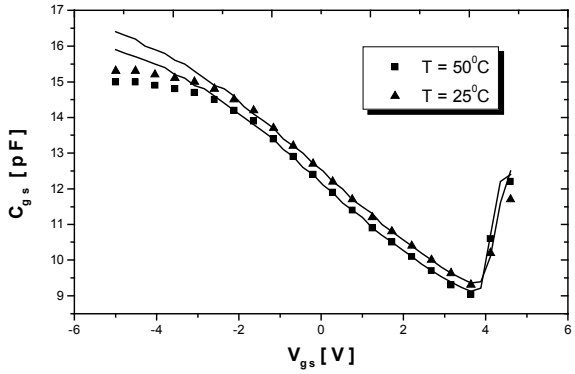

Fig. 8. Measured (dashed) and modelled (line) gate-source capacitance at different T_a, with Freq=1Mhz

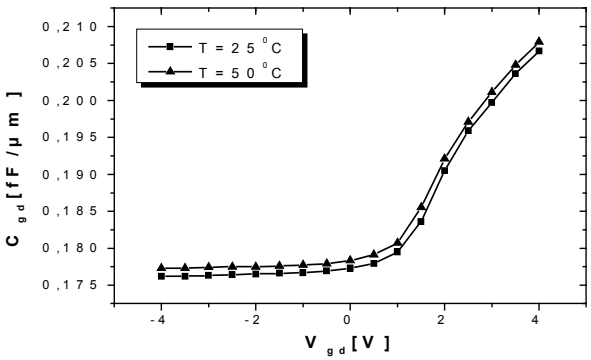

Fig. 9. C_{gd} obtained from the physical simulation approach (Atlas 2-D) at different T_a, with Freq=1Mhz

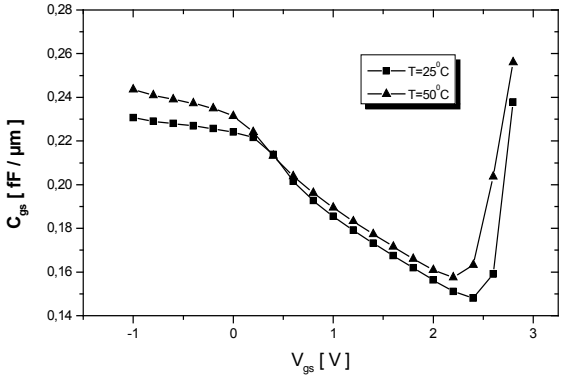

Fig. 10. C_{gs} obtained from the physical simulation approach (Atlas 2-D) at different T_a, with Freq=1Mhz

IV. CONCLUSION AND PROSPECTS

A new electro-thermal model (three thermal cells), taking into account self-heating effects and the temperature influence was developed. In other words, self-heating effects on a LDMOS transistor have been characterised. Consequently, temperature effects and all the thermal aspects from the chip to the ambient air have been taken into account. The results are in good agreement with those obtained from the rigorous device numerical simulation including self-heating effects. Different layers of the device are modeled, so we can add, for instance, other thermal cells to better fit the device's thermal behavior and its heat dissipation. Measurements and simulations of the S-parameters are in progress to obtain a complete compact model.

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