Modeling of energy capability of power devices with copper layer integration

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Abstract:

High power devices can generate large amount of heat dissipation that limits severely their power handling capability. In this paper, we propose intensive investigations of the electro-thermal characteristics of lateral nDMOS transistors processed in a 0.7 µm CMOS based smart power technology. In particular, it is demonstrated, both experimentally and theoretically, that the thermal management improves substantially when a layer of an electroplated copper is deposited on top of the power device. The latter serves as a heat sink to help dissipate the heat generated during operating conditions. More importantly, we have derived a simple but yet potential theoretical model which predictions are in complete agreement with experimental and simulation results.

Keywords – Power devices, heat dissipation, heat sink.

1. Introduction

In the current trend of smart IC technology, the power density is getting increasingly important such that thermal management of high power devices has become one of the most challenging key factors for design engineers to keep junction temperatures within safe operating limits [1,2]. Therefore, thermal solutions are strongly required to meet technological requirement in the presence of harsh operating conditions like those encountered in the case of automotive applications. One potential solution to improve thermal performance and reliability of high power devices consists in integrating materials that provide a highly conformable path between hot regions and heat spreaders. Because of its thermal properties and compatibility with other involved materials, copper constitutes a good candidate to achieve this task as has been demonstrated in [3] and more recently in [4]. Nevertheless, fundamental understanding of all issues related to the modelling and simulation of the impact of the topologies and thickness of the copper layer has not been examined in detail.

In this paper, we give a quantitative understanding of the impact of a copper cover layer integration on the electro-thermal performances of the device using intensive investigations based on both experimental measurements and transient electro-thermal simulations. In section 2 we will give a brief description of the studied DMOS transistor device as well as the obtained experimental and simulation results. In section 3, an original theoretical model that reveals and explains the action of the copper layer is derived and which predictions are in complete agreement with the experimental and simulation results. Finally, we conclude in section 4.

2. Experimental and Simulation Results

To quantify the impact of an electroplated Cu layer on energy handling capability of high power semiconductor devices, different thickness and placements, with respect to the active region, of the copper layer have been integrated in the design of 40V lateral nDMOS transistors processed in a 0.7 µm CMOS I2T platform technology [5]. These power devices have a square shape of area $A = 0.36mm^2$ and contain a large number of cellular MOSFET transistors. In this paper, we will focus especially on devices with a centrally located copper layer for which a schematic representation is given in Fig. 1b together with the reference structure where no copper layer is present, Fig. 1a. The electroplating of copper has been realized on wafers after the end of the conventional smart power process flow and selective opening of windows in the passivation layer according to the process flow described briefly in [4].

Power-to-failure and energy capability measurements are an important figure-of-merit for the analysis of the electro-thermal behavior of power devices. In fact, due to the power dissipation, the internal temperature of the device increases with time and leads to the opening of the parasitic bipolar transistor, which triggers the thermal failure of the device. The moment at which this occurs defines the time-to-failure, t_f, for the given dissipated power, P_f. A schematic representation of the corresponding experimental setup is shown in Fig. 2,

where a rectangular pulse, V_d, is applied at the drain electrode and the gate electrode is biased to a constant voltage. The other electrodes are grounded.

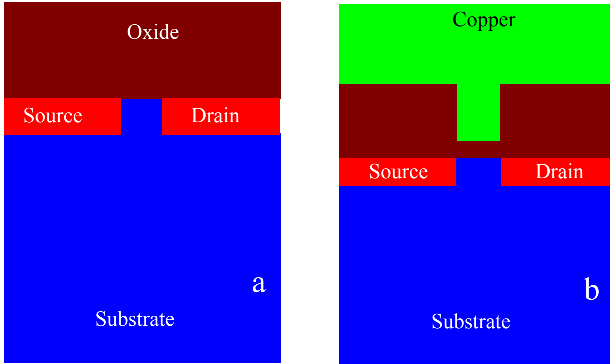

Figure 1: Schematic cross section of the power structures: reference device (a) and device with copper layer (b).

A typical waveform indicating the irreversible destruction of the device is illustrated in Fig. 3 by an abrupt increase of the drain current due to the opening of the parasitic bipolar transistor. In this figure, the observed decrease of the current before thermal failure reflects mobility degradation due self-heating effects.

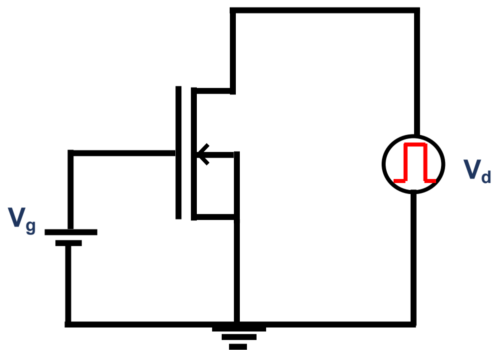

Figure 2: Schematic diagram for the measurement setup used for the energy capability investigations.

On the basis of physical considerations, it is expected that the introduction of a copper layer on the top of the device structure acts as a thermal heat capacitor to absorb and store heat. The heat storage capability of the copper layer should therefore increase with increasing copper thickness and, hence, improve the thermal performance of the device. To verify the validity of this argument and quantify the effectiveness of the copper layer, we have performed a series of single pulse experimental measurements on various devices with different copper thicknesses. In Fig. 4 the energy handling capability, which in the case of a rectangular pulse is defined by:

$$E_c = P_f t_f ,$$

as obtained from power pulse measurements [4], shows an almost linear improvement as a function of Cu thickness in accordance with the above statement.

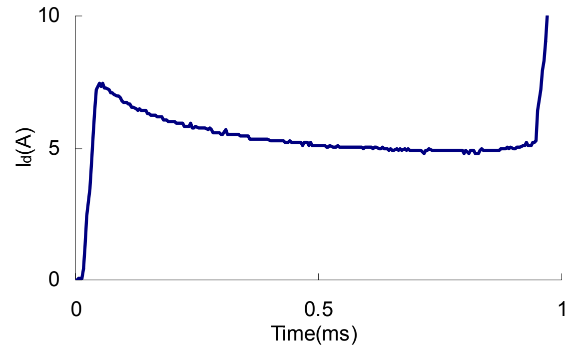

Figure 3: Typical waveform for the measured drain current, illustrating the thermal failure of the power device.

To explain this behavior and clarify the impact of the Cu layer on the cooling process, we have performed transient electro-thermal device simulations for structures with different Cu layer thicknesses in addition to the reference structure. In these simulations, the top surface of the device structure is assumed to be adiabatic whereas the bottom plate is maintained at ambient temperature.

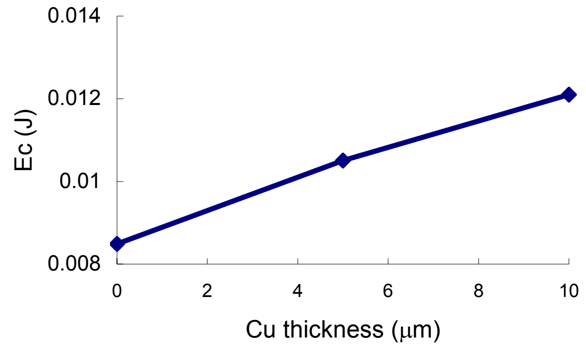

Figure 4: Change in energy capability with thickness of the copper layer for a power device with area A = 0.36 mm^2, as obtained from measurements.

In Fig. 5a and Fig. 5b, we show the temperature distribution within the half structures of the reference and capped device with copper layer , respectively. The corresponding operating conditions are characterized by an applied rectangular pulse of magnitude Vd = 30V and width of t_l = 1.6ms on the drain contact and a constant gate voltage of V_g = 3.3V. Both figures show a gradual decrease of the temperature from the central region (The upper corner of the right-hand side of the figures) where the hot spot is located to the other parts of the devices. This gradient of temperature occurs in both silicon and oxide materials, Fig. 5a, whereas there is almost no temperature gradient in the copper material, Fig. 5b. This is a direct consequence of the difference of the thermal conductivities of the silicon, oxide and copper. In fact, while oxide is a good thermal insulator, copper is a good thermal conductor. Therefore, copper does not only act as a thermal capacitor that stores heat, but it may as well serve as a good heat spreader. Therefore, under the same operating conditions, we expect the maximum lattice

temperature reached within the device with an electroplated Cu layer implemented on the top of it to be less important than that attained in the reference device.

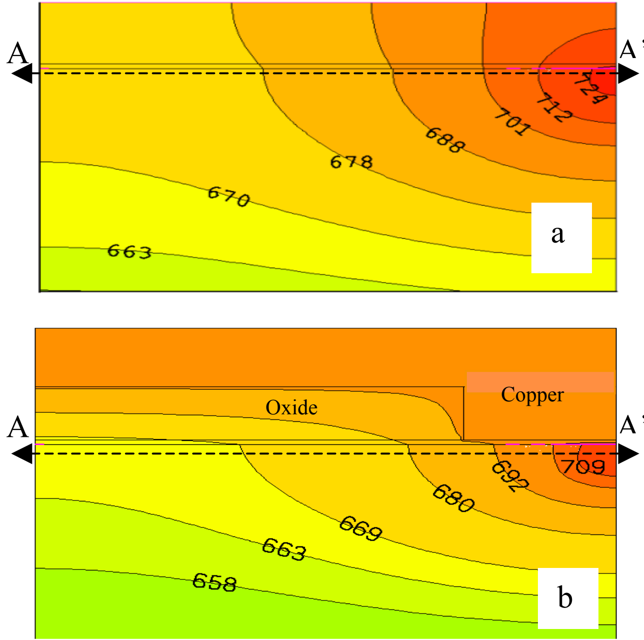

Figure 5: Temperature distribution within half structures at time, t_1 = 1.6ms, for the reference (a) and the electroplated copper layer (b) power devices.

This feature is clearly demonstrated in Fig. 6 where the temperature along the lateral direction and passing by the hot spot region (AA' in Fig. 5) is given in comparison with the reference case. As a consequence of this, we have obtained, for the same dissipated power, a significant improvement of the time-to-failure of about 20% for 5µm thick copper layer with respect to the reference one.

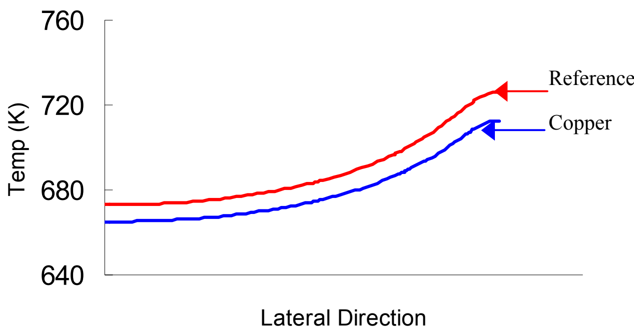

Figure 6: Temperature distributions along the lateral direction, AA', as obtained at time t_1 for the two power devices under the same operating conditions.

To proceed further with our analysis, we give in Fig. 7 the simulated energy absorption capability of the power devices as a function of the Cu layer thickness. This figure shows a linear increase in the energy handling capability in agreement with experimental results shown in Fig. 4.

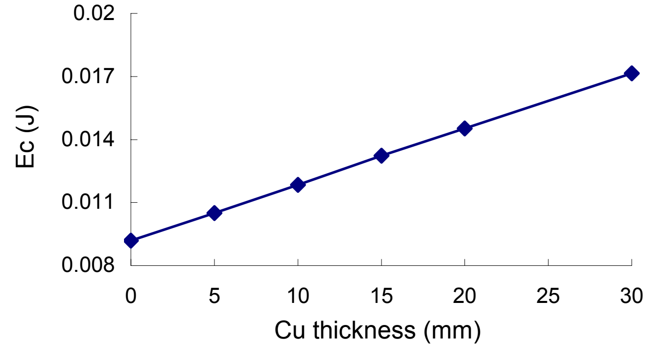

Figure 7: Change in energy capability with the thickness of the copper layer, as obtained from the simulation.

3. Theoretical Model

To quantify the effect of the copper layer on the safe operating area and derive an analytical expression for the energy capability of the structure as a function of the thickness of the copper layer, we have developed a simple, but effective, theoretical approach based on the well-known heat transfer partial differential equation:

$$c\frac{dT}{dt} - \nabla K \nabla T = Q\,. \qquad (1)$$

Where K and c are the thermal conductivity and the heat capacity, respectively. Q is the dissipated power per unit volume. Due to the large thermal conductivity of the copper material, the temperature gradient inside it can be neglected and the above equation can be reduced to:

$$c\frac{dT}{dt} = Q\,. \qquad (2)$$

Hence, if we imagine an experiment in which a copper layer of area A and thickness d, at room temperature, T_0, is in contact with a hot-spot region of a power device at temperature, T, then the energy stored by the copper layer to reach the final temperature, T, is given by:

$$E_{cu} = dAc(T - T_0)\,. \qquad (3)$$

On the other hand, the heat balance equation for this experiment permits us to write the total dissipated energy, E_{tot}, as the sum of two components:

$$E_{tot} = E_{eff} + E_{cu}\,, \qquad (4)$$

where E_{eff} is the necessary energy to bring the power device from room temperature to the final temperature T. Therefore, if the final temperature is equal to the critical temperature, T_c, at which point the device fails, the energy sustained by the device with copper layer before destruction can be written as:

$$E_c = E_r + dAc(T_c - T_0) \qquad (5)$$

E_r may be considered as the energy capability for the reference power device without copper layer. Eq. 5, then, predicts that the energy capability of a power transistor is a linear increasing function of the thickness, d, of the copper layer. This is in total agreement with the above experimental and simulated results. Furthermore, Eq. 5 predicts that the improvement of E_C with respect to the reference device is constant and does not depend on time-to-failure, t_f, for a fixed Cu thickness, which is confirmed by the experimental data illustrated in Fig. 8 with a constant Cst = 40mJ/mm^2.

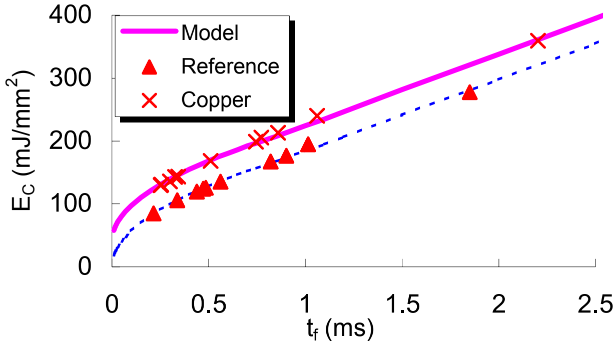

Figure 8: Experimental energy handling capability for the reference and for a device with 25µm thick copper layer. The solid line represents the results of our model.

On the other hand, one can easily demonstrate from Eq. 5 that the power-to-failure, P_f, for the full device can be expressed as:

$$P_f = P_r + \frac{d A c \Delta T_c}{t_f}, \qquad (6)$$

where P_r is the dissipated power at breakdown for the reference device and ΔT_c is the critical temperature measured with respect to the ambient temperature T_0. This result, predicted by our model, is confirmed experimentally in Fig. 9. In this figure we can also see that for large enough, t_f, the power-to-failure, P_f, merges with the reference one, P_r, in complete accordance with Eq. 6.

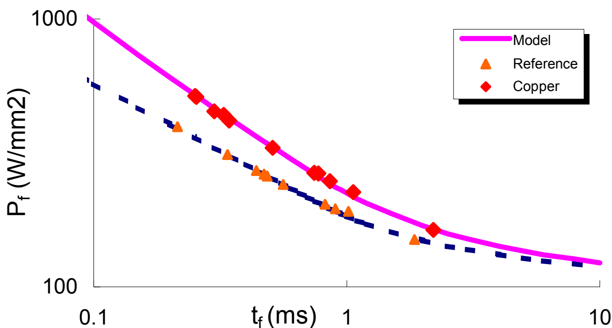

Figure 9: Experimental power-to-failure for the reference and for a device with 25µm thick copper layer. The solid line represents the results of our model.

Finally, we have to mention that heat distribution is a dynamical process that is characterized by a finite time scale, τ, that determines the time needed for heat to diffuse over an entire physical layer. Therefore, if the time-to-failure, t_f, is smaller than the diffusion time, τ, over the entire volume of the deposited copper layer, one would not expect further optimization of the energy capability of the device when the thickness of the copper layer increases and a quasi-saturation behavior of E_C might be observed for small t_f. This statement is demonstrated using pure thermal simulations for power devices with various thickness, d, of the integrated copper layer in Fig. 10. In fact, we show in this figure that there is a time scale τ_d before which the impact of the increase of the thickness of the copper layer can change the evolution of the temperature increase ΔT as a function of time.

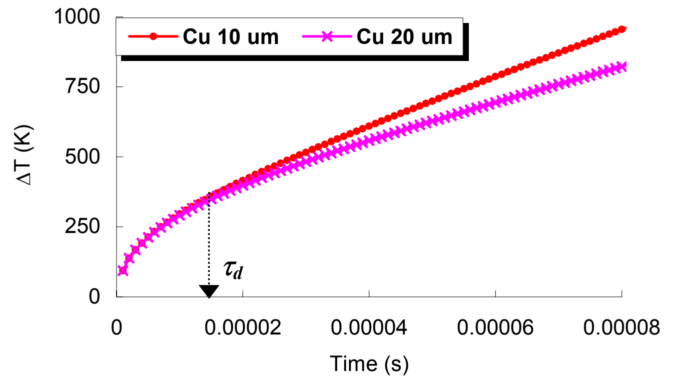

Figure 10: Evolution of the temperature increase with time as obtained from pure thermal simulation, for various copper layer thickness.

4. Conclusion

In this paper, we presented an intensive investigation of the impact of a copper cover layer integration on the electro-thermal characteristics of power devices using both experimental measurements and simulations. In particular, it is demonstrated that the thermal management of smart power devices improves substantially when a layer of an electroplated copper is deposited on top of the power device. The later serves as a heat sink to help dissipate the heat generated during operating conditions. More importantly, we have developed a simple but yet a potential theoretical model that reveals and explains the action of the copper layer and which predictions are in complete agreement with experimental and simulation results.

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