Monte Carlo Simulation of Ion Implantation for Doping of Strained Silicon MOSFETs

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Abstract— **Strain is recognized as one of the key technology features to increase the drive current in scaled MOS devices. We present a Monte Carlo simulation study for introducing dopants into a strained Si/$Si_{1-x}Ge_x$ system at very low energies. The lattice constant in the epitaxial growth direction of the biaxial tensile strained silicon layer is calculated according to the elastic theory. The accuracy of the simulation results is evaluated by comparing the predicted boron and arsenic doping profiles with SIMS measurements. It was found that the predicted arsenic distribution in strained silicon shows a slightly deeper penetration compared to unstrained silicon due to the stress-induced volume dilation. Finally the simulation result of source/drain and extension implants into a three-dimensional strained silicon MOS structure with an STI isolation scheme is presented.**

I. Introduction

Research on biaxial tensile strained silicon on relaxed $Si_{1-x}Ge_x$ has demonstrated that strain is a key parameter in controlling carrier mobility in silicon, and moreover that drain current enhancements associated with improved mobility in long-channel devices persist at short channels. Either uniaxial or biaxial strained silicon can be used to build high-performance MOSFETs required in advanced CMOS microprocessor logic technology. Due to the remarkable potential of strain engineering to enhance the performance of scaled MOS devices, "strained silicon" in its various forms has been included in the International Technology Roadmap for Semiconductors recently.

There are two dominant methods, global and local stress, for introducing strain in the silicon surface channel. Both methods produce changes in the silicon bandstructure due to breaking of the crystal symmetry, and hence alter carrier scattering and effective masses. Global stress techniques employ epitaxial technology to generate a thin layer of strained silicon on relaxed $Si_{1-x}Ge_x$ subsequently grown on a graded SiGe buffer layer grown at first on the silicon substrate. Local stress relies on process techniques such as modifications to shallow trench isolation, high-stress nitride-capping layers around the gate, and selective epitaxial $Si_{1-x}Ge_x$ in the sourcs/drain regions [1]. These techniques are effective in small device geometries where it is possible to induce uniaxial strain in the channel by stressing the regions around the channel. However, it turned out that the improvement in n-MOSFET mobility using biaxial tensile strained silicon on relaxed $Si_{1-x}Ge_x$ is larger than that obtained for local stress techniques [2].

A prerequisite for the scaling of strained silicon MOSFET devices is the formation of highly conductive ultra-shallow source/drain extension junctions. We performed a Monte Carlo simulation study for the doping of a strained Si/$Si_{1-x}Ge_x$ system with boron and arsenic at very low energies. All Monte Carlo simulation experiments were performed with the object-oriented, multi-dimensional ion implantation simulator MCIMPL–II [3] [4], which is embedded in a three-dimensional process simulation environment. The simulator is based on a binary collision approximation (BCA) and can handle three-dimensional device structures consisting of amorphous and crystalline materials including $Si_{1-x}Ge_x$ targets of arbitrary germanium fraction [5]. In order to allow also the simulation of strained silicon layers, the model of a biaxial tensile strained silicon crystal has been implemented in the simulator.

The ion implantation process is accurately simulated by computing a large number of individual ion trajectories in a semiconductor material. The incoming dopant atoms are slowed down due to the nuclear and electronic stopping power of the target material. The final position of an implanted ion is reached where it has lost its kinetic energy. The Monte Carlo simulator uses an atomistic crystal model which allows to simulate the channeling effect of ions in crystalline targets. Being based on appropriately scaled random numbers, the results obtained with the Monte Carlo method are never exact, but they converge to the used model characteristics by increasing the number N of simulated ions. The statistical error vanishes for $N \rightarrow \infty$ [6]. After performing the Monte Carlo calculation, both the doping and damage information are stored in histogram cells aligned on an orthogonal grid. A sophisticated three-dimensional smoothing algorithm based on the Bernstein polynomials is applied in order to reduce the statistical fluctuation of the predicted doping profiles. The smoothed data are then translated from the internal orhogonal grid to an unstructured grid suitable for the subsequent simulation of annealing processes.

II. Modeling of Biaxial Strained Silicon

A strained silicon channel is formed by a silicon layer with a thickness smaller than the critical thickness, epitaxially grown on the (001) surface of a relaxed $Si_{1-x}Ge_x$ buffer layer. The silicon layer is under biaxial tensile strain with an increased in-plane lattice constant $a_{\parallel}$ which is equal to that of the underly-

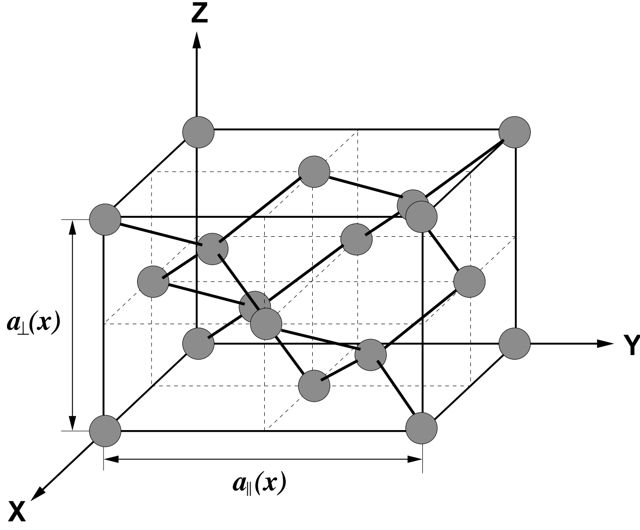

Figure 1: Crystal model for biaxial tensile strained silicon.

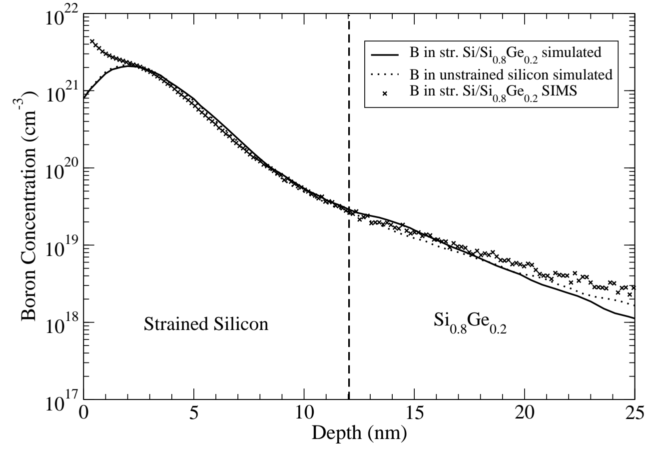

Figure 2: Simulated 400eV boron implant profile in a 12nm thick strained silicon layer compared to SIMS measurement.

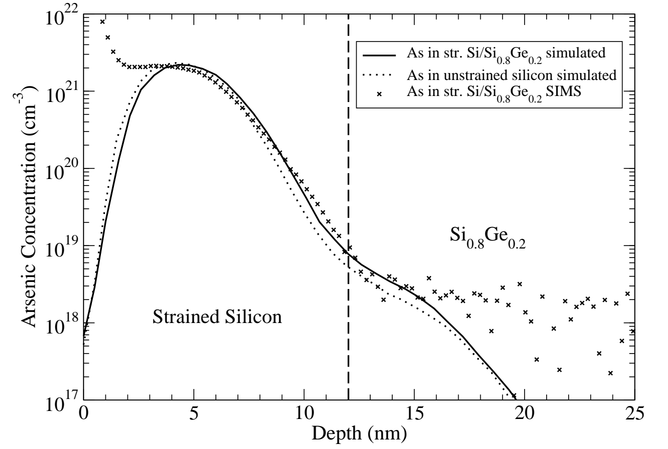

Figure 3: Simulated 2keV arsenic implant profile in strained silicon compared to SIMS data.

ing $Si_{1-x}Ge_x$ layer. The lattice parameter of $Si_{1-x}Ge_x$ crystals depends on the germanium fraction x and can be calculated by a parabolic relation, which approximates experimental data with a maximum deviation of about 10^{-3} Å [7],

$$a_\parallel(x) \;=\; 0.02733\;x^2 \;+\; 0.1992\;x \;+\; 5.431 \quad (\text{Å}). \qquad (1)$$

The out-of-plane silicon lattice constant $a_\perp$, in the direction perpendicular to the interface plane, is reduced according to the continuum elastic theory [8],

$$a_\perp(x) \;=\; a_{\mathrm{Si}}\left[1 \;-\; \frac{2C_{12}}{C_{11}}\left(\frac{a_\parallel(x)}{a_{\mathrm{Si}}} - 1\right)\right] \quad (\text{Å}),$$

$$a_\perp(x) < a_{\mathrm{Si}} < a_\parallel(x) \quad \text{for} \quad 0 < x < 1, \qquad (2)$$

where a_{Si} is the lattice constant of unstrained silicon, and C_{11}, C_{12} are the elastic constants of silicon. The in-plain strain $\varepsilon_\parallel$ and the perpendicular strain $\varepsilon_\perp$ are then defined by

$$\varepsilon_\parallel(x) \;=\; \frac{a_\parallel(x) - a_{\mathrm{Si}}}{a_{\mathrm{Si}}} \quad \text{and} \quad \varepsilon_\perp(x) \;=\; \frac{a_\perp(x) - a_{\mathrm{Si}}}{a_{\mathrm{Si}}}. \qquad (3)$$

Figure 1 shows the strained unit cell with the edge lengths $a_\parallel$ and $a_\perp$, which is used for the Monte Carlo simulation of ion implantation in strained silicon targets. While the simulated ion moves through a strained silicon region, the strained crystal model from Figure 1 is build up around the actual ion position for searching the next collision partner. It turned out that the displacement energy of 15 eV used for unstrained silicon can be applied for strained silicon layers too.

Due to the fact that the strained silicon lattice system is coherently aligned to the $Si_{1-x}Ge_x$ virtual substrate lattice, channeling ions can pass the interface between these two layers without being interrupted. While the implantation profiles in strained and unstrained silicon have only a small difference at a given implantation energy, the penetration depth of ion implanted dopants in relaxed $Si_{1-x}Ge_x$ is significantly reduced with increasing germanium fraction x [9]. The larger nuclear and electronic stopping power for incoming ions in $Si_{1-x}Ge_x$ compared to pure silicon targets is caused by the heavier and electron-rich germanium atoms in the alloy. Thus the underlying $Si_{1-x}Ge_x$ layer helps to reduce the tail region of implanted doping profiles in such a layered wafer structure.

III. Ultra-Shallow Junction Formation

We study the implantation of boron as a p-type and arsenic as an n-type dopant in a silicon cap layer with a thickness of 12 nm on a thick $Si_{0.8}Ge_{0.2}$ layer. Figure 2 shows the simulated and experimental doping profile of a boron implantation with an energy of 400 eV and a dose of $10^{15}\ \mathrm{cm}^{-2}$. Figure 3 shows the arsenic implantation performed with an energy of 2 keV and the same dose. The presented doping profiles demonstrate highly doped source/drain extension implants under the sidewall spacer, where lightly doped drain (LDD) structures used to be in previous devices.

Figure 2 depicts that the comparison of the simulated boron profiles in strained and unstrained silicon are almost identically distributed, and the simulation agrees well with the SIMS data. It is not possible to characterize arsenic concentration profiles in $Si_{1-x}Ge_x$ by SIMS analysis with a resolution larger than about three orders-of-magnitude due to the similar atomic masses of arsenic and germanium [10]. As shown in Figure 3 the Monte Carlo simulation can help to get a realistic continuation of the doping profile below the arsenic detection limit. It can be speculated that the discrepancy between the predicted and measured doping profiles near the wafer surface may also arise from a measurement error in this region. However, the simulation results in Figure 3 demonstrate that the arsenic distribution in strained silicon has a slightly deeper penetration compared to unstrained silicon which can be explained by a stress-induced volume dilation of the material. Strained silicon on $Si_{0.8}Ge_{0.2}$ has a strain $\varepsilon_{\|}(0.2) \approx 0.75\%$ and approximately 99% of the atomic density of unstrained silicon.

The applicability of strained silicon on relaxed $Si_{1-x}Ge_x$ buffer layers for MOS device fabrication requires that as-implanted ultra-shallow junction depths do not change during rapid thermal annealing (RTA). P. Kohli and R. Wise analyzed the Spike-, Flash-, and Impulse-RTA techniques with regard to their suitability for ultra-shallow junction formation. They found a very limited diffusion for implanted boron and arsenic distributions in strained silicon on $Si_{0.8}Ge_{0.2}$ by applying the Flash-assist RTA technique [11].

IV. Three-Dimensional MOSFET Application

The formation of ultra-shallow source/drain and extension regions is demonstrated on a three-dimensional 65nm gate-length MOS device presented in Figure 4. The device structure was generated with the three-dimensional solid modeler Laygrid [12]. The three-dimensional device geometry is modeled in terms of horizontal layers which include parts of different material segments. The material properties of each segment have to be specified too. Figure 4 shows that the simulation domain includes the 12nm thick strained silicon layer and a 620nm thick relaxed $Si_{0.8}Ge_{0.2}$ virtual substrate block. The oxidized wafer surface provides a gate oxide thickness of 2nm. The simulated high-performance MOS device is isolated by employing a shallow trench isolation (STI) scheme. This MOS structure can be used for strained silicon n- and p-MOSFETs depending on the implanted dopant species. Using scaling considerations, a source/drain vertical junction depth around 25nm is recommended for fabrication of such a 65nm gate MOS transistor.

In the first ion implantation step the arsenic source/drain extensions were implanted with an energy of 2 keV and a dose of $10^{15}\ \mathrm{cm}^{-2}$. Figure 5 shows the three-dimensional Monte Carlo simulation result after smoothing the arsenic distribution. Figure 6 depicts that an anisotropic grid refinement was applied locally in order to optimize the unstructured grid for the intended shallow source/drain regions and to keep the overall

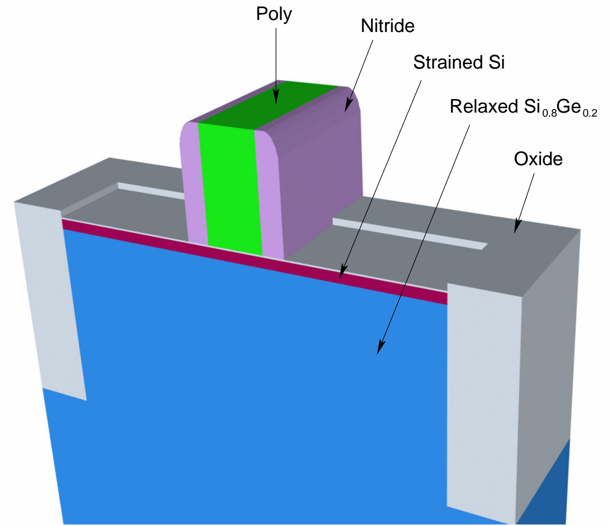

Figure 4: Structure of a half of a high-performance 65nm gate strained $Si/Si_{0.8}Ge_{0.2}$ MOSFET with an STI isolation scheme.

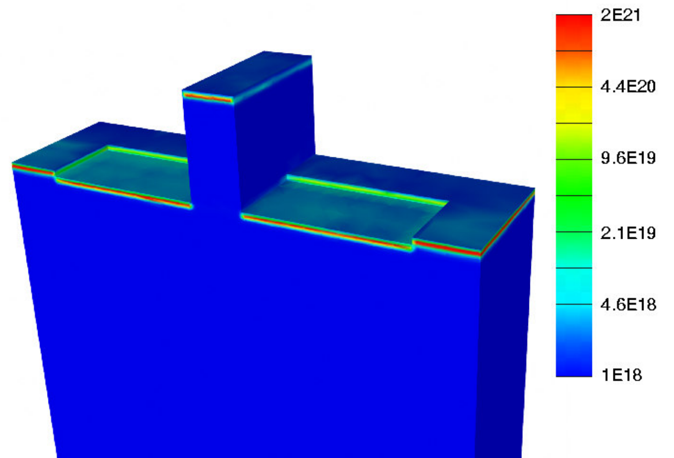

Figure 5: Simulated arsenic distribution in the n-MOS structure after performing the 2keV source/drain extension implant.

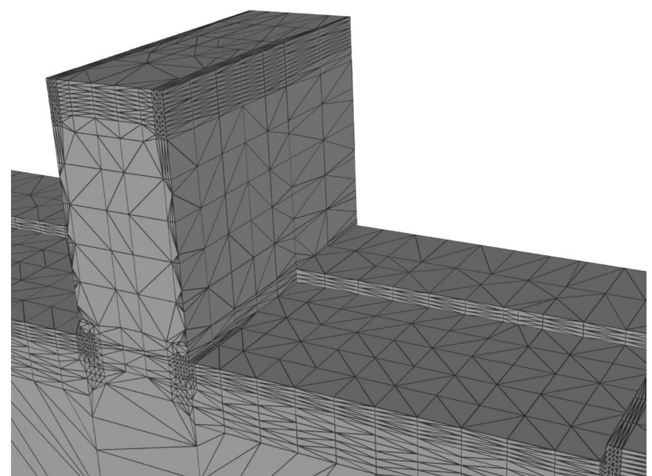

Figure 6: Unstructured destination grid used for the smoothing of the Monte Carlo result in the structure without sidewall spacer.

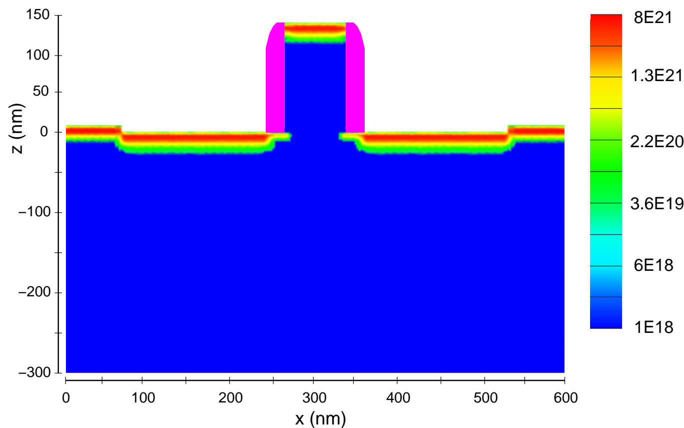

Figure 7: Simulated cross-section of the strained n-MOSFET after performing of the 6keV arsenic source/drain implant.

grid below 20 000 points. The grid refinement was performed with the three-dimensional grid generator DELINK [13]. The meshing strategy of DELINK follows the concept of advancing Delaunay methods and produces tetrahedral grid elements. For the implantation simulation of the source/drain extensions, the sidewall-spacer segment was cut off in the device structure by changing the material property from "nitride" to "air". After performing the Monte Carlo implantation step on the internal orhogonal grid, the resulting arsenic concentrations are smoothed and translated from the internal grid of the simulator to the unstructured destination grid.

In the subsequent arsenic implantation step the actual source/drain regions are formed using an energy of 6 keV and a dose of $5 \cdot 10^{15}$ cm^{-2}. Figure 7 shows the simulated cross-section along the channel of the strained n-MOSFET after performing of the source/drain implants. In this application, the Monte Carlo simulation was carried out with $2 \cdot 10^7$ initial ions per implantation step to achieve a low statistical fluctuation of the predicted doping profiles.

V. Conclusion

Strained silicon provides an attractive platform for building high-speed CMOS devices due to the enhanced carrier mobility compared to bulk silicon. The global stress approach allows to adjust the biaxial tensile strain in the silicon layer on top of a relaxed $Si_{1-x}Ge_x$ buffer layer by altering the germanium content. The presented Monte Carlo simulation study demonstrates the formation of ultra-shallow junctions by ion implantation processes in a strained $Si/Si_{0.8}Ge_{0.2}$ layered target system. A good agreement between the simulated boron and arsenic profiles and the corresponding SIMS data was found at the used very low implantation energies. The strain of $\varepsilon_{\parallel}(x = 0.2) \approx 0.75\%$ reduces the atomic density to approximately 99% of unstrained silicon. While the reduced density has almost no impact on boron profiles, the arsenic-implanted junction depth in strained silicon lies about 1nm deeper than in unstrained silicon. The simulation of a two-step arsenic implantation sequence into a three-dimensional 65nm gate-length strained silicon MOS structure with STI isolation was performed with 2 keV and 6 keV, respectively. The final simulation result demonstrates that the required source/drain junction depth of 25nm for fabrication of such a transistor is met.

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