The Impact of Layout on Stress-Enhanced Transistor Performance

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***Abstract* – This paper studies the sensitivity of stress-enhanced transistor performance to layout variations. Stress simulations and mobility models are calibrated and verified for test structures with SiGe source/drain as a stressor. The role of STI on the stress transfer is explored. The numerical results show that variations of 15% in drive currents and of 44% in hole mobility due to layout induced stress variations can occur in the cases studied. These deviations need to be taken into account in circuit design or to be compensated via layout modification.**

I. Introduction

The stress generated by shallow-trench isolation (STI) can alter the drive current of NMOS and PMOS transistors by up to 20% depending on the length of diffusion (LOD) [1]. As a consequence, the drive current of a transistor is not only related to the parameters of the gate such as the gate length L and width W but also to the exact layout of the individual transistor. As dimensions shrink even this model is not adequate as the stress becomes dependent on the width of the STI surrounding the transistor. The performance of the transistor is therefore related to the surrounding layout. A similar problem arises with the intentional application of stress by deposited SiGe layers [2-4]. There has been limited study of the sensitivity of the performance enhancement to layout variations [5]. This paper analyzes in more detail the impact of layout on SiGe stress-enhanced PMOSFET performance. Results from numerical simulation are compared with measurements on test structures. Calibrated models are applied to complex layouts from cell libraries.

II. Experimental and simulation details

The PMOS transistors with SiGe source/drain (S/D) were fabricated using the process flow described in [4]. Simulations were performed using Taurus-Process and Taurus-Device 2D/3D TCAD tools that contain an extensive set of stress-related features [6]. We used a model for the stress-induced enhancement of the low-field hole mobility that was extracted for compressive uniaxial stress up a level of 1.5GPa [7].

The test structures consisted of two types of transistors that are common to chip layouts, namely isolated and nested transistors. The isolated transistor was surrounded by STI, whereas the nested transistors were bounded by multiple polysilicon gates and doped SiGe source and drains. The characteristic dimensions are the channel length L and width W, the source and drain length Ls/d, and the STI width. Figure 1 shows the simulated 2D cross-section of a typical isolated 35nm PMOS transistor, and Figure 2 shows a typical nested 35nm PMOS. The corresponding layouts are shown in the figures as the top inserts. The white lines shown in the silicon regions in both figures represent the simulated P/N junctions.

Two main types of stress are generated in the transistors at the end of process flow: the thermal mismatch stress and the lattice mismatch stress. The thermal mismatch stress results from the thermal expansion coefficient difference between silicon and STI. The compressive thermal mismatch stress in the STI can reach several hundreds mega Pascal near the interface. The lattice mismatch stress is due to the difference in lattice constants between silicon and SiGe. The compressive lattice mismatch stress in SiGe near interface approaches 2 GPa with about 20% germanium content.

The thermal and lattice mismatch stresses are redistributed to reach stress equilibrium. The redistribution process involves local deformations to transfer stress from high concentration regions to low concentration regions. Normal stress and displacement continuities across region interfaces are imposed in the numerical simulations. As a result of the rebalance process, stresses are induced in the channel region.

The magnitude of the balanced stress field decays with distance from the stressors. The magnitude reflects the contribution from multiple stressors. Therefore, stress in the transistor channel depends on the characteristic lengths such as channel length L, channel width W, Ls/d, and STI width.

III. Results

The simulated distributions of the stress component along the channel direction for the isolated and nested transistors with 0.4μm Ls/d are shown in Figure 3 and Figure 4, respectively. It is interesting to note that the

STI next to SiGe in the isolated transistor serves as a stress relaxer for the SiGe, in contrast to standard transistors (no SiGe) where the STI serves as the sole stressor. Whether the STI serves as a stressor or relaxer depends on the relative magnitude of the stresses in STI and in the surrounding regions. With some of the stress being released to STI, less stress in SiGe is available for transfer to the channel for the isolated transistor. As a consequence, the channel stress is significantly lower in the isolated PMOS than in the nested PMOS for the same characteristic dimensions.

Figure 5 shows measured and simulated stress-induced mobility enhancements as a function of Ls/d. The mobility enhancement increases with Ls/d due to the increasing size of SiGe stressor. At small Ls/d, transistors with nested gates exhibit higher mobility enhancement than the isolated transistors due to the absence of STI relaxer. For large Ls/d cases, (Ls/d >1 μm), the mobility enhancements saturate at the same level for both isolated and nested transistors. When the Ls/d is scaled down to 200 nm, the minimum size for the 90 nm technology node, the mobility enhancement is 30% less than the saturation value. There is a small but noticeable effect of the width of the transistor. As the width increases the stress increases and reaches the saturation level as shown in Figure 6.

IV. Consequences for real layouts

More complicated layouts encountered in typical CMOS chips were simulated using the calibrated models. Figure 7 shows a top view of the longitudinal stress distribution in the channels of five PMOSFETs that are part of a library cell for the 45 nm technology node. Due to the shape of the diffusion area and the relative placement of the gates, the compressive longitudinal stress varies by a factor of three at different locations in the cell. In transistor 1, the stress varies across the width of the channel. It is low in the bottom part because of the narrow diffusion region on the right hand side and reaches a maximum in the upper part where the SiGe islands extend for a longer distance on the right hand side. The stress is close to maximum for transistors 2, 3 and 4 and then falls off for transistor 5 which has a narrow SiGe region on its right side

The drive current is estimated from the average mobility in the channel. The simulated performances of the transistors at different locations within the cell are compared in Figure 8. The net result is that the actual drive current of specific transistors in this layout can deviate from the drive current assuming uniform stress by up to 15%. This deviation needs to be taken into account either in circuit design or the layout needs to be modified to ensure that the circuit performs as intended

The case of CMOS inverters in isolated and dense environments, shown in Fig. 9, illustrates the errors that can arise if the layout is not carefully considered. The amount of STI surrounding each transistor varies greatly between the isolated and dense layouts. Figure 10 shows an inverter pulled from each of the isolated and dense layouts. The PMOS transistors are modeled with recessed SiGe S/D while the NMOS transistors contain no explicitly engineered stressors. Figure 10 also shows the stress-induced mobility enhancement for each of the transistors averaged over the width of the transistors. For PMOS, the transistor in the dense environment maintains a large mobility enhancement from the SiGe S/D due to less stress relaxation from the smaller amount of surrounding STI. In this case, SiGe acts as a stressor and STI as a relaxer. For NMOS, however, STI acts as the sole unintentional stressor and therefore an environment with more STI (the isolated case) induces a larger stress and hence mobility change. Since the induced stress degrades NMOS, the dense environment with less stress shows less mobility degradation.

V. Summary

The impact of layout characteristic lengths on stress enhanced transistor performance is studied. The stress simulations and mobility models are calibrated and verified experimentally using test structures with simple rectangle layouts. It is identified that STI serves as a relaxer in a stress-enhanced SiGe S/D PMOS transistor but as a stressor in a standard (no SiGe) transistor. The numerical results show that the drive current deviation due to layout induced stress variation can go up to 15% for PMOS transistors in a library cell, and the mobility enhancement can differ by 44% for PMOS transistors in isolated and dense environments of a CMOS inverter.

References

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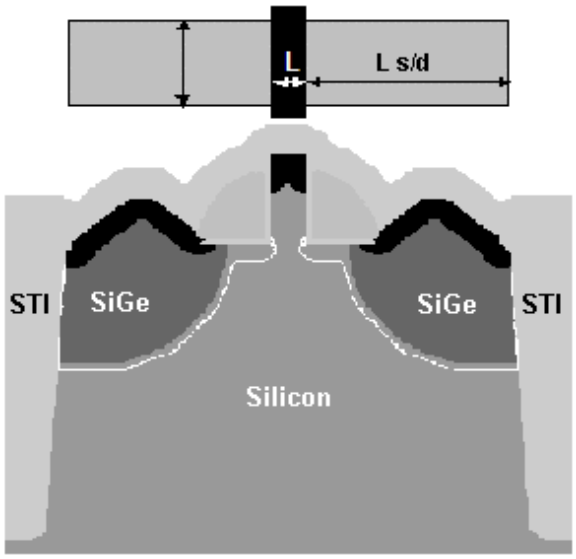

Figure 1: Simulated 2D cross-section of an isolated 35nm PMOS. Layout is shown on the top insert.

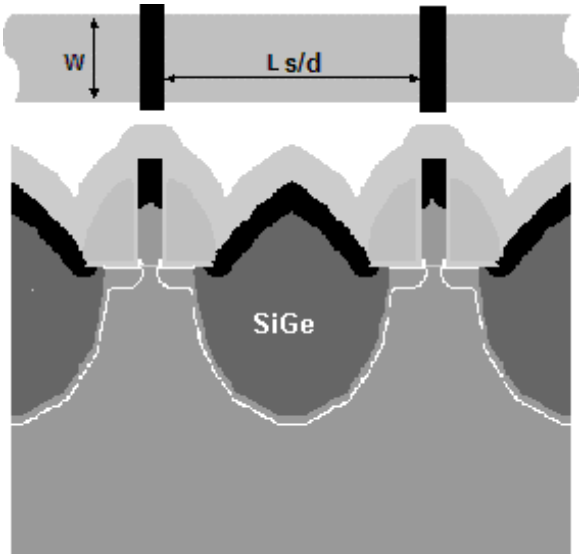

Figure 2: Simulated 2D cross-section of a nest 35nm PMOS. Layout is shown on the top insert.

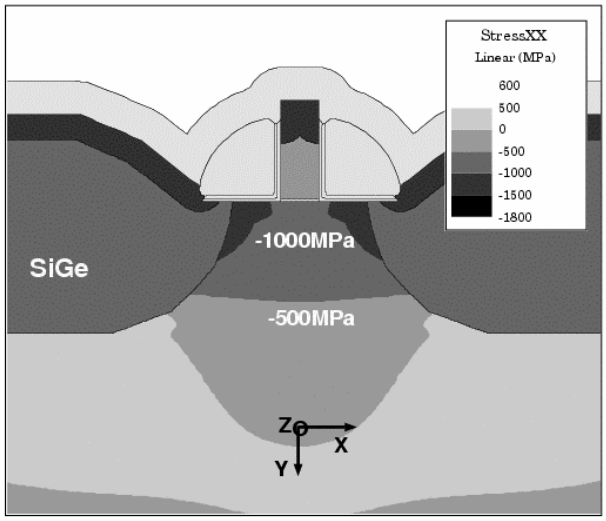

Figure 3: Simulated stress distribution of the normal stress component along the channel direction for an isolated PMOS transistor with 0.4 µm Ls/d.

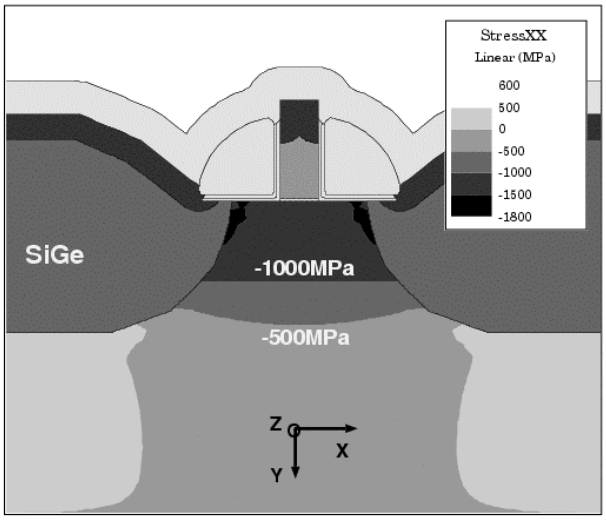

Figure 4: Simulated stress distribution of the normal stress component along the channel direction for a nested PMOS transistor with 0.4µm Ls/d.

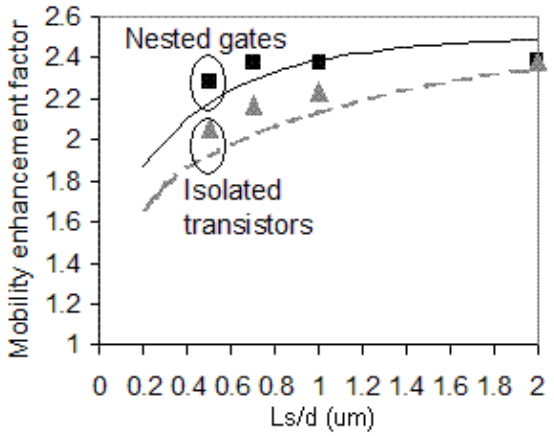

Figure 5: Mobility gain of isolated transistors and transistors with nested gates as a function of Ls/d. Measured data is shown as symbols and simulation results are shown as lines.

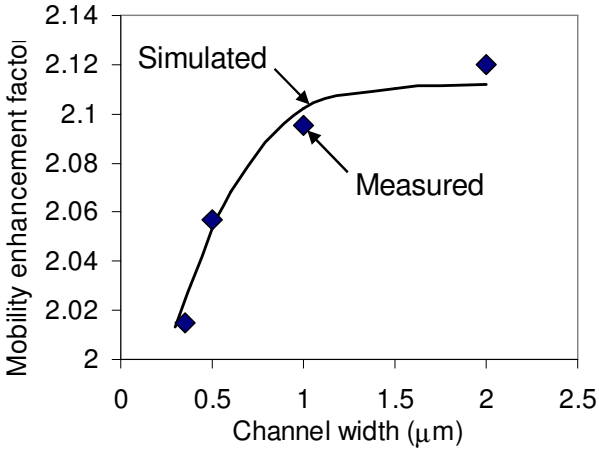

Figure 6: Mobility gain of isolated transistors as a function of channel width. Measured data is shown as symbols, and simulation results are shown as lines.

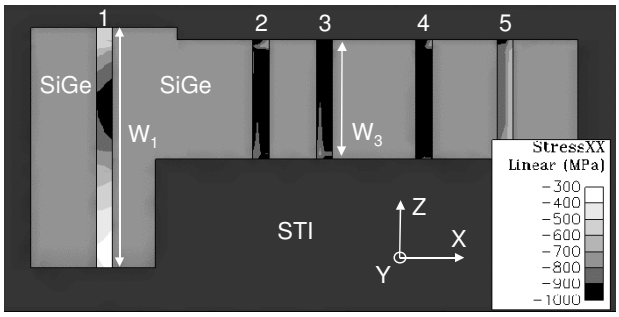

Figure 7: PMOS transistors from a library cell for the 45 nm technology node. Transistor #1 is supposed to have drain current twice as big as the other transistors. Simulated longitudinal stress distribution is shown as a top view of the 3D simulation domain.

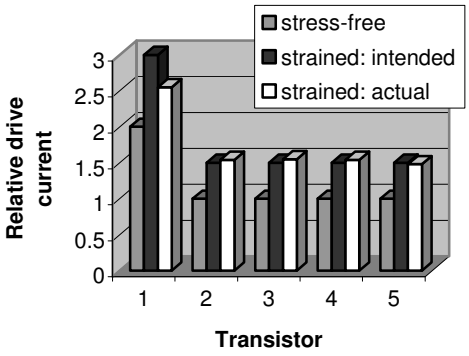

Figure 8: Comparison of the intended relative transistor strength and the actual transistor strength including the non-uniform stress distribution.

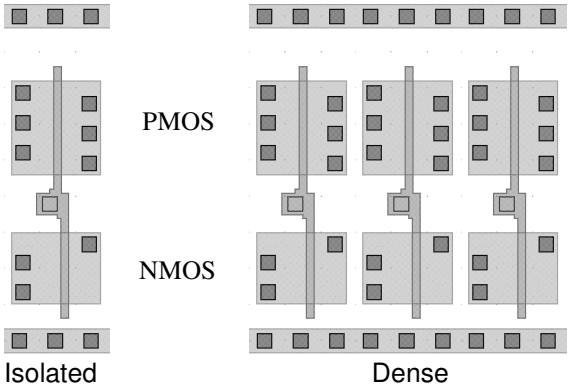

Figure 9: Layout for inverters in isolated and dense environments.

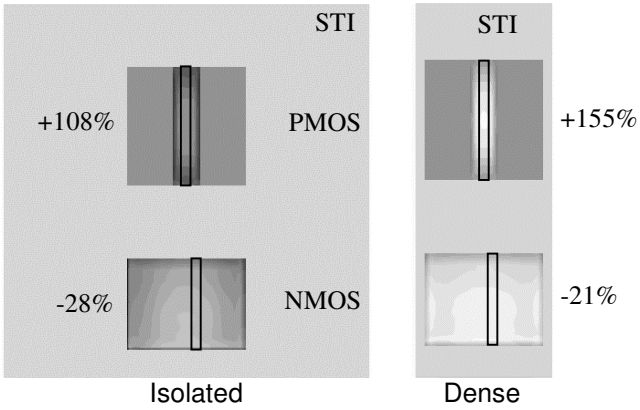

Figure 10: Mobility variation across silicon for NMOS and PMOS transistors in inverters placed in isolated and dense environments. Gate locations are outlined. Also marked is the average low-field mobility stress-enhancement of each transistor.