Phenomenological model for "stress memorization" effect from a capped-poly process

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***Abstract*- NMOSFET drive current improvement by a disposable stressor or a capped-poly process has been reported recently in the literature[1]. The retained drive current gain even after the removal of the stressor film is attributed to a stress "memorization" effect. A phenomenological model and numerical simulations showing the memorized stress are reported for the first time in this paper. An irreversible shape change of the polysilicon gate during the process is simulated by a plastic deformation model and the final resulting channel stress and associated Ids gain are analyzed.**

I. INTRODUCTION

Stress "memorization" from a capped poly process has been reported recently [1]. In the process, certain stressor (typically nitride or oxide) materials are deposited on top of polysilicon gates and subsequently removed after a thermal anneal. Since the stressor film no longer exists in the final structure, the drive current gain is believed to come from stress "memorized" in the polysilicon. Although re-crystallization of the amorphized polysilicon during subsequent anneal and structural deformation of the polysilicon were discussed to be the possible causes of the memorized stress, the exact mechanism of how the stress is "memorized" has not yet been clearly described. We have developed a phenomenological model based on the structural deformation of the polysilicon through a transition from the elastic to the plastic states during thermal treatment. While we do not model the various complex physical mechanisms of the polysilicon structural deformation, which probably involve grain boundary dynamics, we show that this simplified model does capture some of the important experimental trends of Idsat gain and its dependence on capped poly thickness. This model can be a helpful guide for further technology development at 65 nm and beyond utilizing the stress "memorization" technique.

II. MODEL DESCRIPTION

A schematic of the simulation structure is shown in Fig 1. As noted above, the polysilicon is modeled as a temperature-dependent elasto-plastic material. An extensive calibration methodology was carried out to calibrate the coefficients used for material properties of the various materials in the simulation structure. Nano indentation and wafer warpage measurements were made on samples where various film stacks had been deposited on unpatterned wafers. For coefficients where experimental data were not available for calibration, the best available values from literature were taken [2].

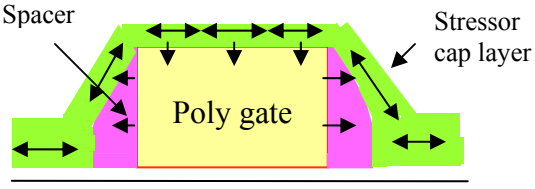


Fig 1: Schematic of the stress "memorization" process. The stressor nitride cap layer is removed subsequent to the source drain anneal.

III. MODEL DISCUSSION

The simulation procedure is described as follows:

(1) The initial stress is first solved at room temperature.

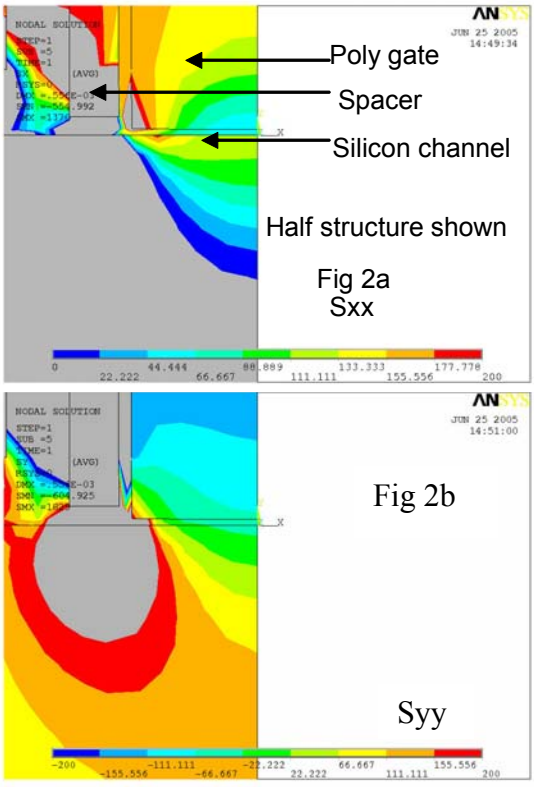
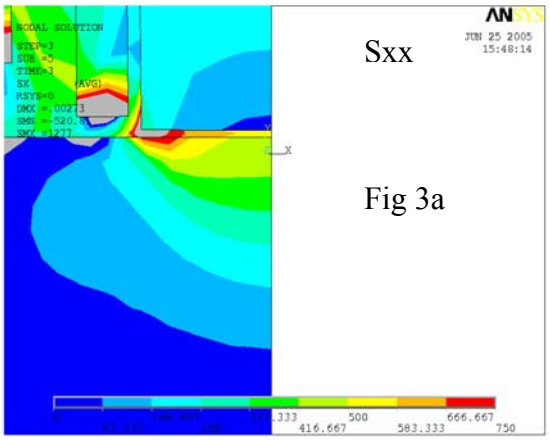
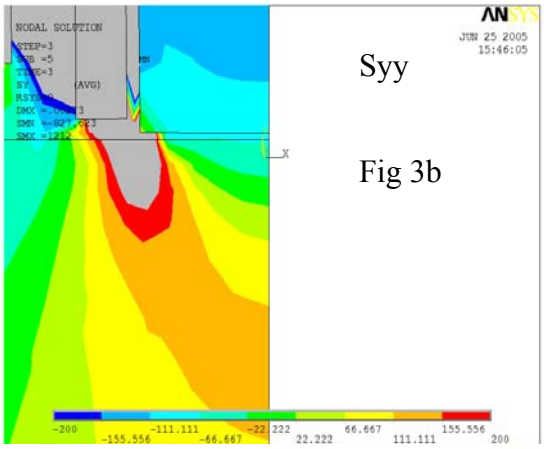


Fig 2: (a) Lateral tensile stress (Sxx) and (b) Vertical compressive stress (Syy) before the ramp to high temperature. Gray areas represent stress values outside of plotted range.

The contour plots of lateral and vertical stress components, Sxx and Syy, are shown in Fig 2. The resulting stress at this step is mainly due to the initial stress of the spacer materials. The initial stress values of the spacer materials used in the simulations are derived from wafer warpage measurements of as-deposited films on blanket silicon wafers.





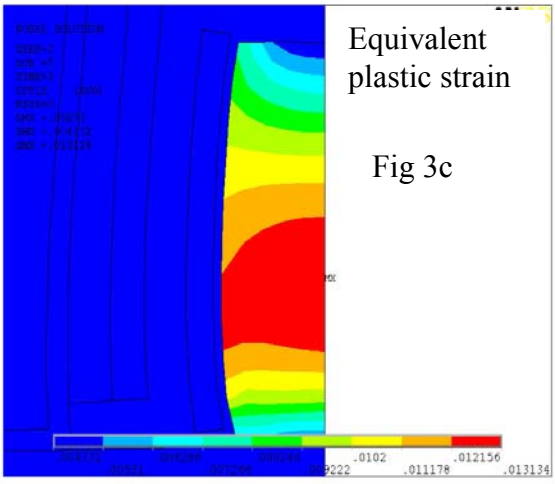


Fig 3a-c: Lateral tensile stress (Sxx), vertical compressive stress (Syy) and equivalent plastic strain at peak temperature. Gray areas represent stress values outside of plotted range. In 3c, the deformation is intentionally exaggerated 15X to show lateral expansion and vertical compression of the poly.

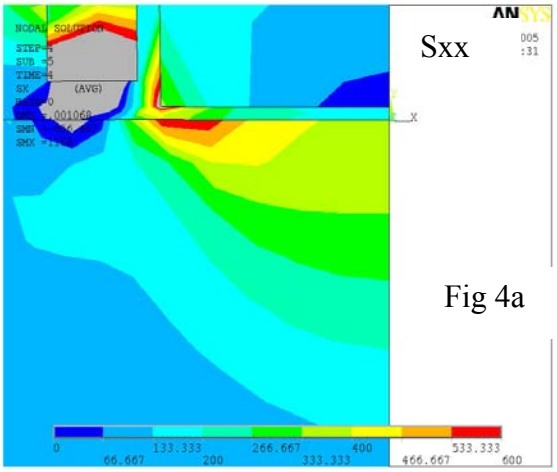
(2) The stress is solved where temperature of the structure is increased to the peak temperature of the anneal (> 1000^{O}C).

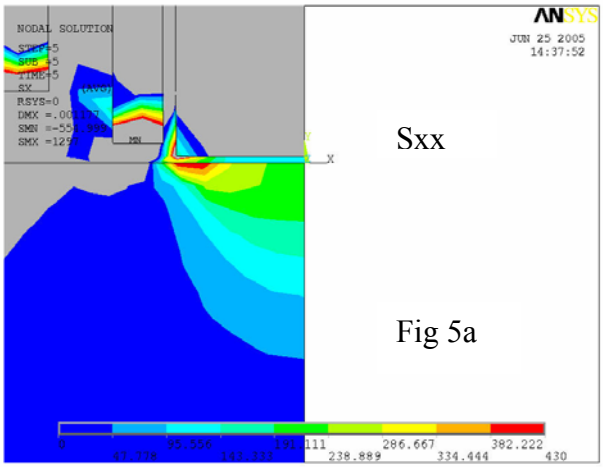
During this step, the intrinsic stress of the cap nitride film is modified to a certain value. Based on experimental observations, it is believed that the intrinsic stress of the cap nitride film increases dramatically during high temperature anneals. This increase is caused by certain nitride material property changes for which very limited information is available. This intrinsic value at peak temperature is consistent with measured stress value of 800MPa where the cap nitride film is annealed and then cooled back down to room temperature.

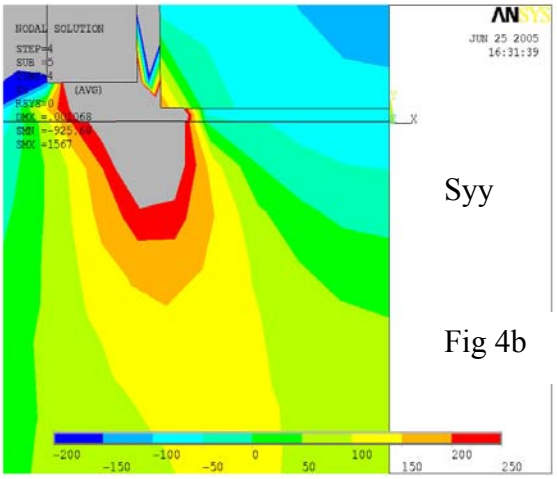
The contour plots of lateral and vertical stress components, Sxx and Syy at peak temperature are shown in Fig 3. An elasto-plastic model is used to describe the polysilicon gate. That is, the polysilicon is elastic upto the yielding point for a particular temperature and then is plastic beyond the yielding point. In order to capture the temperature dependent behavior of the polysilicon which becomes easier to deform with increasing temperature, temperature dependent parameters are used. The yielding stress of polysilicon is modeled as a decreasing function of temperature. The temperature dependence of the yielding stress is calibrated to independent wafer warpage measurements made on films deposited on blanket wafers. As seen in Fig 3, both Sxx and Syy are larger than their room temperature values due to the thermal mismatch between various materials. The simulations show that plastic strain is induced in the polysilicon during the high temperature anneal as shown in Fig 3c. It is also noted that the deformation of the polysilicon is such that it is expanded in the lateral (X) direction and compressed in the vertical (Y) direction.

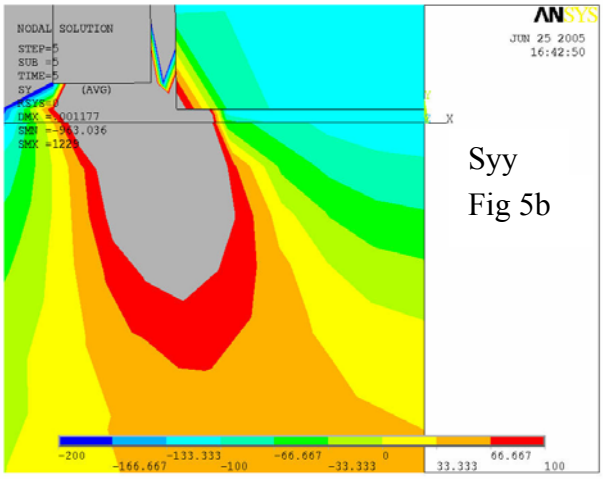
(3) The temperature is decreased to room temperature and the stress and strain in the structure are solved again. Sxx, Syy and the plastic strain at this step are shown in Fig 4. During the cooling process, the plastic strain in the polysilicon is mostly retained and the surrounding structure elastically conforms to the polysilicon.

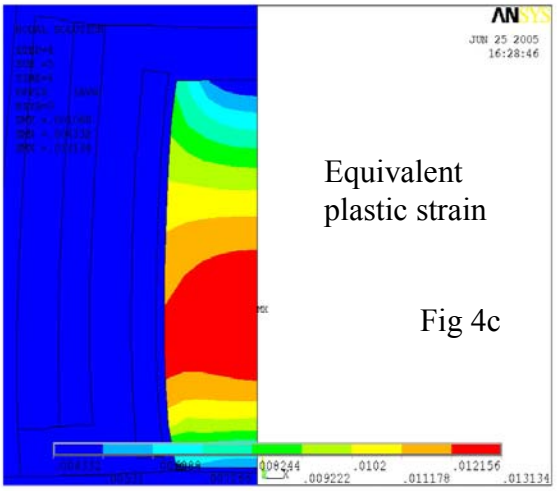
(4) Finally, the nitride stressor film is removed and the stress and strain are re-solved. Sxx, Syy and the equivalent plastic strain in the final structure are shown in Fig 5. As can be seen from Fig 5, the polysilicon retains its plastic deformation and a lateral tensile stress is induced or memorized in the MOSFET channel.











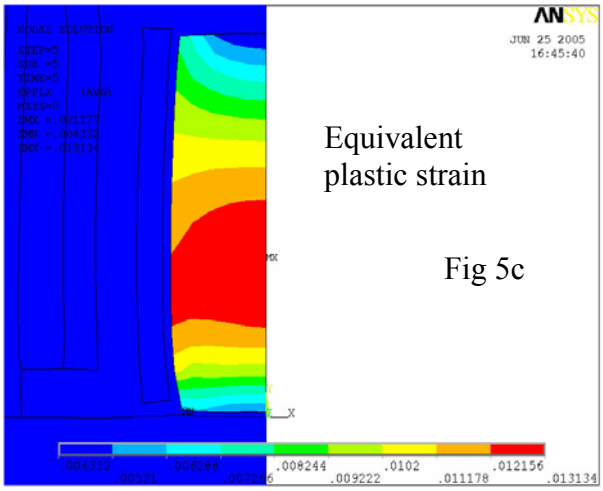


Fig 4: Sxx, Syy and equivalent plastic strain after cool down to room temp. Gray areas represent stress values outside of plotted range. In 4c, the deformation of poly is intentionally exaggerated 15X to show lateral expansion and vertical compression of the poly.

Fig 5a-c: Sxx, Syy and equivalent plastic strain after stripping the nitride. Gray areas represent stress values outside of plotted range. Note that the nitride is stripped and deformation is exaggerated 15X in 5c.

For a 400A nitride stressor film with an initial tensile stress of ~800 Mpa, the simulated final stress in the channel region is ~220 MPa tensile in the lateral (channel) direction and ~120 MPa compressive in the vertical direction. Compared to CESL (contact etch stop layer) induced stress where the stressor film remains intact, the disposable stressor or capped-poly process does not induce a large vertical compressive stress which also contributes to NMOS drive current improvement. The exact amount of resulting vertical stress also depends on how the surrounding materials react to stress at high temperatures. For instance, the nitride materials used in the spacer have an initial tensile stress which will modulate the extent of vertical compressive stress transferred to the polysilicon. Device simulations performed with the stress fields included showed a Ids performance gain of ~4% for capped poly nitride thickness between 200-600A. In cases where higher performance gain has been reported [1], we believe that part of the gain can also be due to an increase in channel profile retrograde which can be confirmed by SCM measurements.

IV. CONCLUSION

A phenomenological model has been developed to explain the stress "memorization" effect seen in the disposable stressor process. The memorized stress is simulated and associated Idsat gain is analyzed.

V. REFERENCES

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