A Unified Statistical Model for Inter-Die and Intra-Die Process Variation

Ji-Seong Doh, Dae-Wook Kim, Sang-Hoon Lee, Jong-Bae Lee, Young-kwan Park, Moon-Hyun Yoo, and Jeong-Taek Kong
CAE Team, Memory Division, Semiconductor Business, Samsung Electronics co., LTD.
San #24 Nongseo-Ri, Giheung-eup, Yongin-City, Gyeonggi-Do, 449-711, Korea (E-mail:js.doh@samsung.com)

Abstract *– An efficient characterization technique with the spatial correlation matrix from electrical device parameters such as threshold voltage and saturation current accounting for inter- and intra-die variations is demonstrated. Then, a unified statistical model based on the correlation matrix is developed and implemented to the SPICE simulator to predict the distribution of circuit performance. In order to verify our model, test chips which consist of transistors and ring oscillators were fabricated using a 130nm CMOS technology. Simulated delay/skew variations of ring oscillators agree well with the measurement of test chips, maintaining a reasonable accuracy of 85 %. Especially, we show that as the distance of the two ring oscillators becomes larger, the timing skew between them becomes bigger. Moreover, the sensitivity analysis for the performance of simple analog and digital circuit, is performed in terms of inter- and intra-die variation.*

1. INTRODUCTION

The fluctuation of device characteristics caused by process variation has considerably increased in nanometer technologies. Process variations can be classified into inter- and intra-die. Inter-die variation which comes from lot-to-lot, wafer-to-wafer, and within wafer affects every device on a single chip equally. On the other hand, intra-die variation refers to device characteristics that vary from device to device within the same die.

As a device scales down, intra-die variation has become as important as inter-die variation when analyzing circuit performance and predicting the yield of a chip [1, 2]. With rising concerns of intra-die variation, some of these investigations which modeled process variations and performed timing analysis have been proposed [2-5]. Especially, gate length variation which depends on their local layout patterns is modeled and simulated with modified design templates [5]. Although this approach includes pattern-dependent effects, it does not account for distance-dependent correlations [6], where devices that are close to each other have a higher correlation than devices that are placed further apart. In addition, some of work which accounts for both inter- and intra-die variation was reported [7]. While the previously reported modeling techniques were based on a correlation matrix, these methods cannot be practically expanded to prediction of the distribution of the circuit performance due to time-consuming and difficulty in measuring SPICE model parameters such as mobility and substrate doping.

In this paper, a unified statistical model accounting both inter- and intra-die variations is developed, and implemented into a conventional SPICE circuit simulator. Especially, it is demonstrated that the correlation matrix preserving the relation between the devices on a chip is characterized from test chips, and easily translated to the SPICE model using the ET-based SPICE modeling method [9].

2. MODELING OF VARIABILITIES

Fig. 1 shows the key concept of a characterization technique capturing both inter- and intra-die variation. Due to the process variations, the scatter-diagram of closely adjacent identical devices on a chip, which is characterized from electrical device parameters measured repeatedly on several wafers, is expressed as the correlated sets of device parameters such as threshold voltage (Vth) and saturation current (Idsat) instead of using SPICE model parameters. The correlation coefficient shown in Fig. 1(a) can be newly defined, based on Vth and Idsat, as follows,

Ⅰ) $\rho_{ij} = 1$ if only inter-die variation.
Ⅱ) $\rho_{ij} = 0$ if only intra-die variation.
Ⅲ) $0 < \rho_{ij} < 1$ if both intra- and inter-die variation.

Since inter-die variation caused by the process temperature, equipments properties, wafer polishing and wafer placement affects every device on a single chip equally [2], the correlation coefficient value has 1 in case that inter-die variation only exists (case Ⅰ). On the other hand, intra-die variation caused by the optical proximity effect, dopant fluctuation and line edge roughness (LER) has the intrinsic statistical nature of the same devices on chip [6]. Thus, the electrical parameters of those can be treated as independent variables (case Ⅱ). In addition, the correlation value varies from 0 to 1 in case that both inter- and intra-die variations exist (case Ⅲ).

Correlation can be expanded to long distance between identical devices on a chip, and represented as the function of distance between the devices on a chip. It is

reported that the distance-dependent device variation is caused by gradient effects such as etch loading effect, photo resist thickness non-uniformity, etc [2][6-7]. Finally, the correlation matrix which can account for the relation of every device is obtained, as shown in Fig. 1(b).

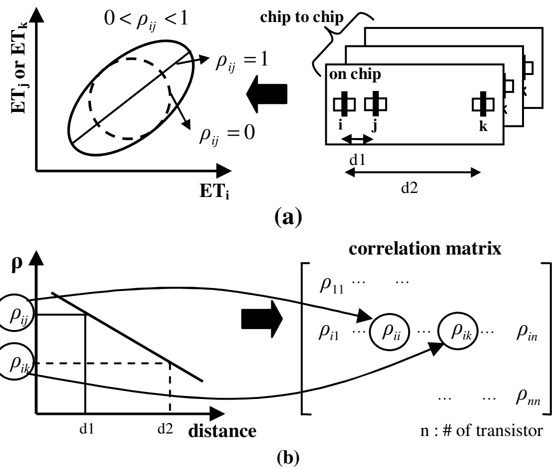

Fig. 1. (a) The correlation between electrical parameters, (b) A method mapped into the correlation matrix with the spatial correlation parameter. (ρ_{ij} : correlation value of i_{th} device and j_{th} device and d1 is less than d2 respectively). The Correlation value for a short distance is higher than that for long distance.

In order to explain capturing the correlation matrix from electrical device parameters obtained from test chips, containing hundreds of nMOS/pMOS and ring oscillators, was designed and manufactured using 130nm CMOS technology. As shown in Fig. 2, the test chip is composed with 4 x 5 test modules. As shown in Fig. 3(a), electrical device parameters between the module (M1) and (M2) that are close to each other have higher correlation coefficients than those between the module (M1) and (M7). In addition, it is shown that the spatial correlation is modeled as the first polynomial function of the distance between devices, in Fig. 3(b).

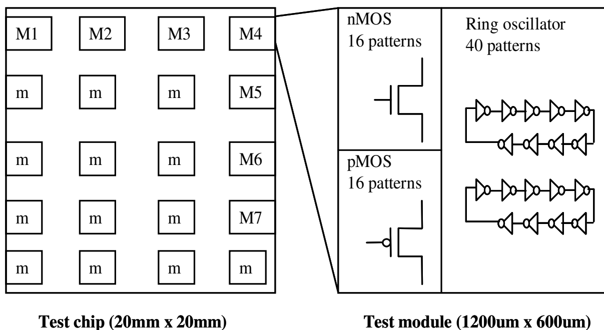

Fig. 2. The architecture of the 130nm test structure for verifying the modeling accuracy. 40 patterns of ring oscillators are positioned in a module with 16 patterns of nMOS & pMOS transistors.

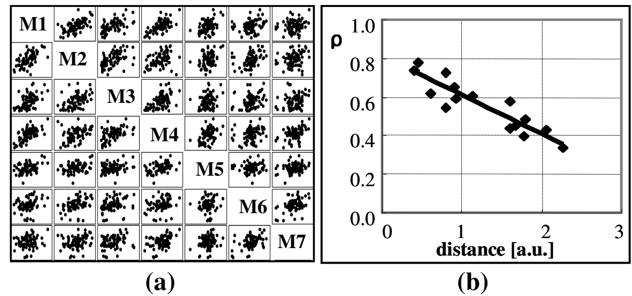

Fig. 3. (a) Scatter plots show the correlation between measured nMOS saturation currents within test chip and (b) modeled as the first polynomial function of the distance between measured Ids of devices.

Fig. 4 shows an overview of a unified statistical model to map inter- and intra-die variations into the circuit performance. Since the circuit performance is influenced directly by the threshold voltage Vth and the saturation current Idsat of devices, we characterize the correlation matrix of electrical device parameters including μ, σ and ρ from the test chip. Then, a new statistical model is performed to predict the distribution of circuit performance using the correlation matrix accounting for inter- and intra-die variation. In this model, two statistical methods are used. First, statistical netlists preserving the relation of the electrical parameters of each device in the netlist are generated using a principal component analysis (PCA) [8]. Secondly, the ET based model is used to easily transform electrical device parameters into the SPICE model [9].

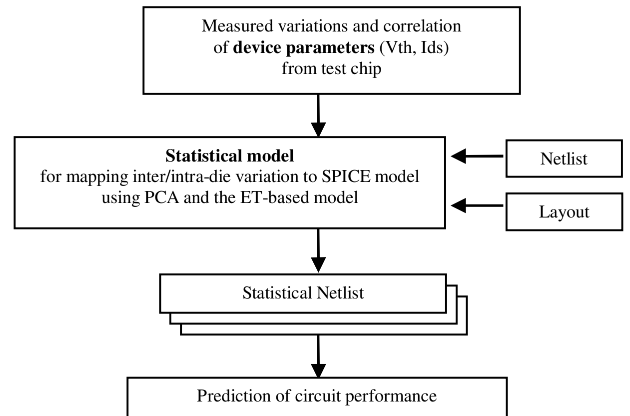

Fig. 4. The flowchart of the proposed method.

3. EXPERIMENTAL RESULTS

To evaluate the accuracy of the proposed model, electrical device parameters and ring oscillator delay, were compared with correlation data measured from test chip. Fig. 5 (a) and (b) show that the correlation of the simulated Idsat results agree well with those of the

measured Idsat in case of short and long distances between devices. As show in Fig. 5(c) and (d), the simulation results of the ring oscillator delay agree well with measurement. Simulated ring oscillator with delay and skew show less than 15% errors as shown in Fig. 5 (e).

Fig. 6 shows that the variation of the delay skew of two ring oscillators tends to be larger as the distance between them increases and our model represents this tendency. We applied the model to separating the effect of inter- and intra-die variations for the distribution of circuit performance, as shown in Fig. 7. The gain of OP-AMP is affected by a great portion of intra-die variation, but the ring oscillator delay is affected by both of them.

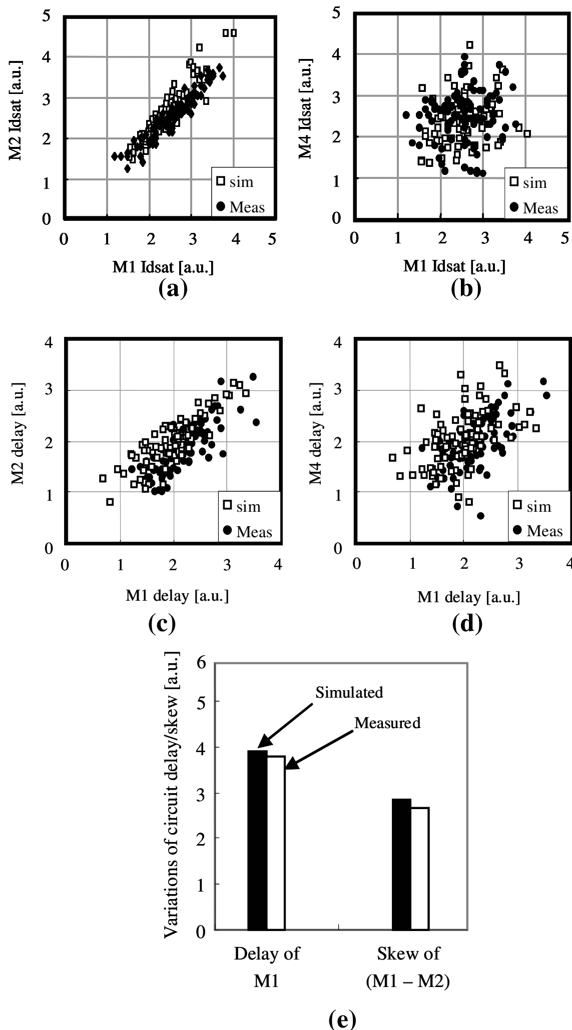

Fig. 5. The comparison of simulation results with measurement. Idsat for short distance (a) is highly correlated than those for long distance (b). (c) The comparison of the simulation result for delay and skew of ring oscillators with the measurement. Ring oscillator delay and skew show less than 15% error (M1, M2 and M4 were shown in Fig. 2).

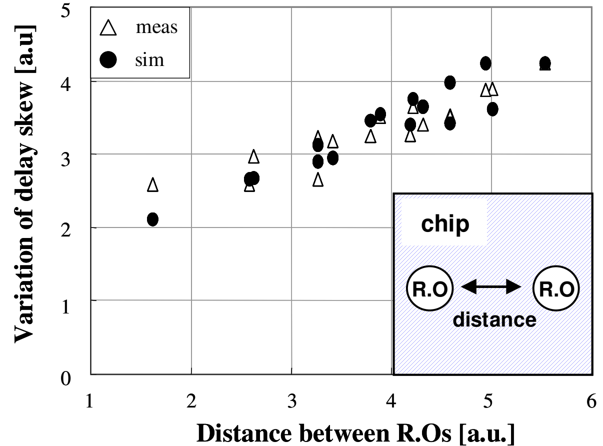

Fig. 6. The variation of the delay skew of the two ring oscillators within the test chip tends to be larger as the distance between them increases. The simulated results from our model agree well with the measurement of test chip.

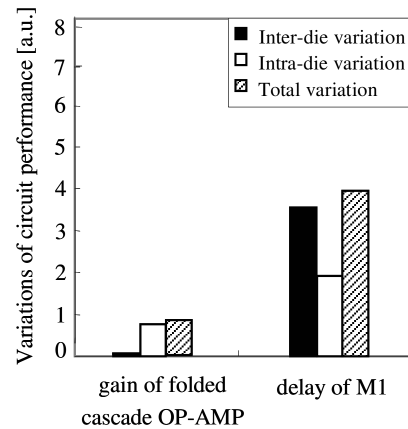

Fig. 7. The comparison between inter- and intra-die variations for the gain of OP-AMP and the delay of the ring oscillator. It means that the model can accurately predict the distribution of analog circuits as well as digital circuits.

4. CONCLUSIONS

In this paper, an efficient characterization technique for the spatial correlation matrix preserving inter- and intra-die variation was demonstrated. Then we proposed a unified statistical model which was able to consider both inter- and intra-die variation by using the correlation matrix. It was shown that the error is less than 15% in terms of delay/skew variation of ring oscillators between the simulated results obtained from a proposed model and measured data. Our model predicts that the variation of the delay skew of two ring oscillators tends to be larger as the distance between them increases, which was verified by the measurement.

For the first time, we show quantitatively that a spatial correlation between electrical device parameters within test chips fabricated the 130nm CMOS technology. It is observed that the analog circuits are much more sensitive to the intra-die variation than the inter-die variation whereas the digital circuits are sensitive to both.

5. REFERENCES

[1] Sani R.Nassif, "Within-Chip Variability Analysis, " *in Proc. IEDM*, Dec. 1998.

[2] K. A. Bowman, and J. D. Meindl, "Impact of within-die parameter fluctuations on future maximum clock," *in Proc. CICC*, May 2001.

[3] A. Agarwal, D. Blaauw, V. Zolotov, S. Sundareswaran, Min Zhao, K. Gala and R. Panda, "Statistical delay computation considering spatial correlations," *in Proc. DAC*, Jan. 2003.

[4] K. Okada, K. Yamaoka, and H. Onodera, "A statistical gate delay model for intra-chip and inter-chip variabilities" *in Proc. DAC,* Jan. 2003.

[5] M. Orshansky, L. Milor, Pinhong Chen, K. Keutzer, and Chenming Hu, "Impact of spatial Intrachip gate Length Variability on the Performance of High-Speed Digital Circuits," *IEEE Trans. Computer-Aided Design*, Vol.21, NO.5, May 2002.

[6] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Wlbers, “Matching properties of MOS transistors,” *IEEE Journal of Solid-State Circuits*, Vol. 24., Oct. 1989.

[7] S. Zanella, A. Nardi, A. Neviani, M. Quarantelli, S. Saxena, and C. Guardiani, “Analysis of the impact of process variations on clock skew,*” IEEE Tran. Semiconductor Manufacturing,* Vol. 13, Nov. 2000.

[8] S. H. Lee, C. H. Choi, J. T. Kong, J. K. Park, C. H. Choi, W. S. Lee, and J. H. Yoo, "An efficient statistical analysis methodology and its application to high-density DRAMs," in Proc. IEEE/ACM Int. Conf. CAD, pp. 459-464, Nov. 1997.

[9] S. H. Lee, D. Y. Lee, T. J. Kwon, J. H. Lee, Y. K. Park, B. S. Kim, and J. T. Kong, “An efficient statistical model using electrical tests for GHz CMOS devices,” in Proc. International Workshop on Statistical Modeling, pp. 72-75, June 2000.