Integrated Simulation Flow for Self-Consistent Manufacturability and Circuit Performance Evaluation

A. Shibkov, V. Axelrad
SEQUOIA Design Systems, Woodside, CA, USA
valerya@sequoiadesignsystems.com

***Abstract* - In this work we present an application of a novel DFM (Design For Manufacturability) simulation flow, which self-consistently predicts the impact of the manufacturing process on electrical circuit behavior. We apply our methodology to the design of a 2x2 AND-OR standard cell to show its effectiveness. We show that process distortions significantly impact both DC and transient circuit behavior, and have to be considered for accurate timing analysis, prediction of IDDQ and other circuit characteristics. Intrinsic process variability and process excursions cause additional deviation from design intent and therefore performance issues and potential yield losses. This work extends and generalizes concepts introduced in [1-2] and presents an integrated implementation of a self-consistent simulation flow [3] which provides unique insight into process-design interactions.**

I. Introduction

Circuit simulation is an indispensable tool in the design of integrated circuits. However, as MOSFET process technology continues to advance into the deep submicron, the accuracy of circuit simulation using common circuit simulation tools in combination with standard compact device models such as BSIM3/4 greatly diminishes. This loss of accuracy occurs because the commonly used SPICE models were constructed to represent transistors with simple rectangular gates and fail to accurately capture characteristics of complex transistor geometry.

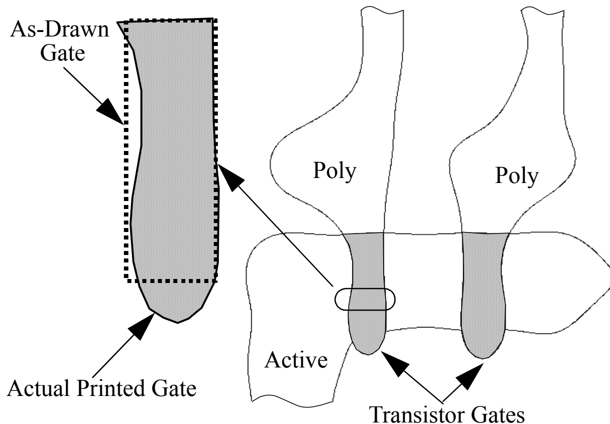

Fig. 1 Typical lithography distortions: A MOSFET gate manufactured using typical litho process has complex non-rectangular shape. Its geometry can no longer be characterized by a single pair of L and W values.

Fig. 1 shows the extent of lithography distortions typical for 90nm technology at nominal process conditions. Transistor gates are no longer rectangular. Significant distortion in linear dimensions occurs within a single gate. As a result, the MOSFET can no longer be characterized by a single pair of L and W values. This renders common compact circuit models inaccurate. We address this problem by constructing a sub-circuit model for each MOSFET consisting of several transistors with different geometries connected in parallel. This approach is illustrated in Fig. 2.

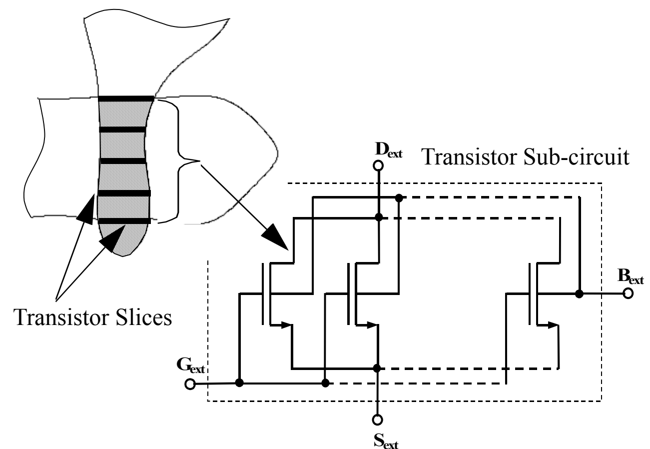

Fig. 2 Non-rectangular MOSFETs are divided into a number of narrow slices. Each slice is assigned L and W values extracted from lithography simulation results and becomes a new transistor in the sub-circuit representation of the original MOSFET.

Original transistor gates are divided into narrower slices. Each slice is modeled as a separate MOSFET with unique L and W. A number of slices are used to construct the new sub-circuit model for each original MOSFET. Such subcircuits constitute quasi 3-D transistor models which provide a significantly more accurate description of the actual non-ideal device behavior and are compatible with regular SPICE simulators and compact transistor models. Transistor

statements in the original netlists are then replaced with new subcircuit models. The new netlists are simulated using standard SPICE-type circuit simulators and compact models thus seamlessly fitting into the standard design flow.

II. DC characteristics and IDDQ

To show the impact of litho distortions on the performance of a complete circuit, we use the layout of a 2x2 AND-OR cell shown in Fig. 3 which contains 10 transistors. This layout creates a relatively irregular neighborhood for different devices which is reflected in the simulated shape of poly gates as shown in Fig. 3. Lithography simulation

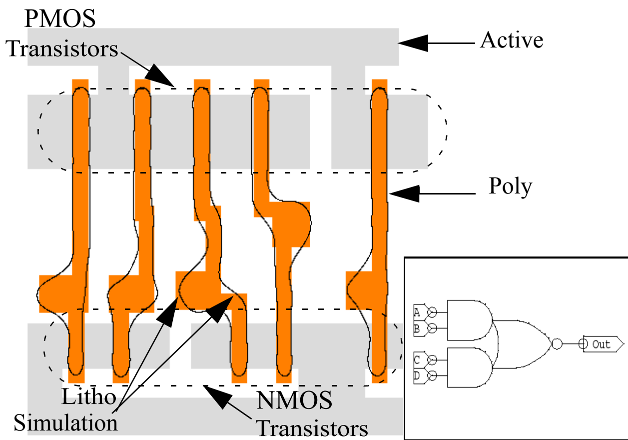

Fig. 3 Layout of the 2x2 AND-OR standard cell showing original Poly and Active layer polygons and Poly gate outlines produced by litho simulation.

results show that printed poly gate contours not only deviate substantially from the drawn poly, but also vary based on the device location as a result of proximity effects. This neighborhood-dependent distortion of poly gates affects device characteristics and has to be taken into account for accurate prediction of electrical circuit performance.

Fig. 4 compares I-V characteristics of the MOSFETs with simulated realistic shapes, modeled using our sub-circuit approach, versus an idealized transistor with rectangular geometry. Characteristics of realistic non-rectangular devices significantly differ from those of the ideal device with both layout-dependent (Fig. 4a) and process-dependent (Fig. 4b) components playing a significant role. Most noticeably, realistic device shapes result in significantly higher off current due to the presence of short gate segments caused by non-ideal lithography. It is worth pointing out that regular 2-D compact device models can not be used in conjunction with "average" gate length to describe devices with complex gate shapes. The highly nonlinear effects of gate length on various device characteristics would result in 2-D model failing to accurately describe complete transistor I-V curve using a single "average L" parameter value. A com-

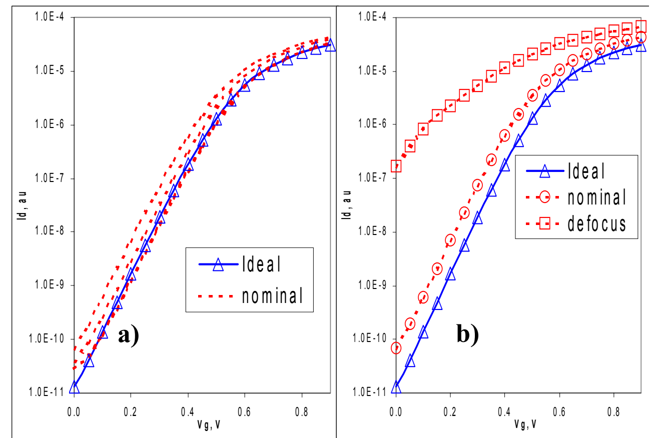

Fig. 4 Comparison of saturation current-voltage characteristics of the ideal rectangular MOSFET and its sub-circuit representation created based on the lithography simulation results. Fig. 4a shows the spread between 5 NMOS devices (nominal litho process) from layout in Fig. 3 compared to the ideal device. Fig. 4b compares characteristics of the ideal device and one of the printed devices for nominal conditions and 0.1 μm defocus.

plex distorted gate shape makes these MOSFETs essentially three-dimensional, making traditional compact device models used in circuit simulation highly inaccurate. Fig. 5 shows the length distribution of transistor slices (as-drawn gate length is 90nm) after lithography simulation of the layout in Fig. 3 using typical 90nm-node nominal process conditions. These distributions indicate the presence of both long and short gate slices with PMOS gates printing consistently wider than NMOS gates. Impact of this intra-gate poly CD

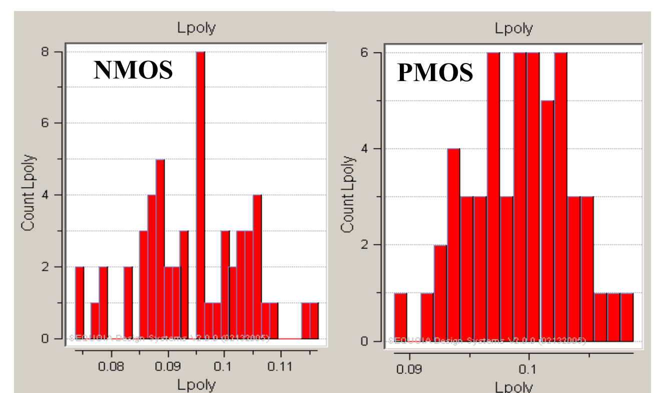

Fig. 5 Length distribution of NMOS and PMOS slices. Both distributions are wide and show presence of short Lpoly segments which create "leaky" areas and increase IDDQ of the circuit.

variability caused by process-layout interaction on IDDQ (circuit stand-by current) of 2x2 AND-OR gate is shown in

Fig. 6. Simulated IDDQ is significantly higher than that predicted by idealized models even for nominal process conditions. When intrinsic process variation it considered, IDDQ increases further. This is shown in Fig. 6 for a defocus of

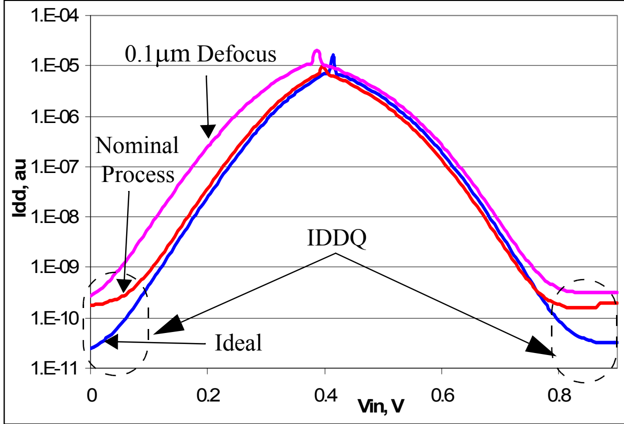

Fig. 6 Dependence of Idd of 2x2 AND-OR gate on input voltage Vin with all inputs driven. IDDQ is much higher than that predicted using traditional simulation. 0.1μm defocus changes switching characteristic and causes significant shift in IDDQ.

0.1μm, which is just one of the components of inevitable process variability. Accurate prediction of IDDQ of circuits in a design for realistic process condition is of critical importance as IDDQ is one of the acceptance tests used in manufacturing and too high IDDQ would result in rejection of otherwise functional parts.

III. Transient Characteristics and Timing

Transient circuit performance is also strongly affected by process-design interactions. To illustrate the impact of process-layout interaction on circuit performance we constructed 5 Ring Oscillator (RO) circuits using 5 separate inverter gates found on the cell layout (Fig. 3). This approach allowed us to avoid confounding of the results by competing effects in a more complex circuit and simplify interpretation of the results.

Transient simulation results for all 5 Ring Oscillator (RO) circuits are shown in Fig. 7. RO frequencies show a significant spread indicating strong mismatch in gate propagation delay caused by process-layout interaction even for nominal process conditions. The difference in propagation delay between the fastest and the slowest gates amounts to approximately 25% which can easily lead to parametric failures in digital circuits. Normal process variability such as defocus and misalignment would further increase deviation of actual circuit behavior from that of the idealized circuit, thus making standard circuit simulation techniques highly

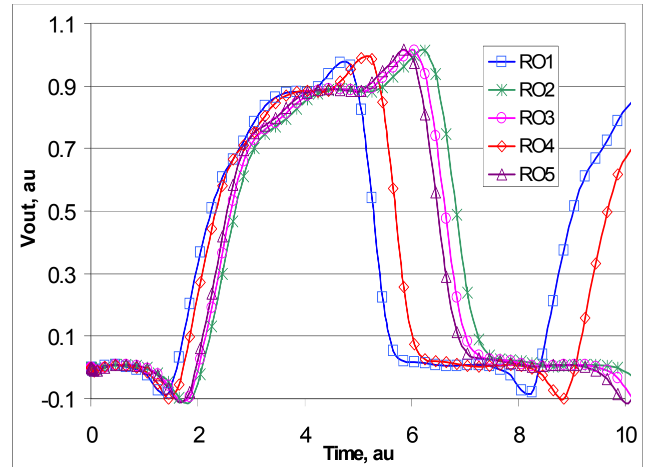

Fig. 7 Simulated ring oscillator waveforms (nominal process conditions) obtained for 5 inverter gates found in the cell layout (Fig. 3). Impact of layout-dependent design-process interaction on local gate level is shown.

inaccurate in predicting circuit performance of as-manufactured circuits.

The impact of this layout-dependent process-induced mismatch of device characteristics could be even more pronounced in analog circuits, such as differential amplifiers which rely on close matching of device characteristics for their operation. In order for a circuit to behave predictably in an actual design, impact of process-layout interaction should be taken into account during the design stage. Our approach readily lends itself to easy integration into both digital and analog design flows.

IV. Traditional OPC and true DFM

An argument could be made that Optical Proximity Correction (OPC) might fix the problems related to process-design interactions. However, in a standard flow, OPC is performed on the final design layout just prior to mask manufacturing, when much of the original design intent is lost. Electrical simulations in the standard flow are carried out using idealized transistor models, using as-drawn transistor geometries, factoring in a few worst/best case process conditions. This implies that electrical simulations in this case are only accurate if OPC succeeds to completely eliminate process distortion effects. This is clearly not possible even at nominal process conditions. Accurate incorporation of process variation is not possible in this approach.

Conventional OPC tools attempt to make all layout polygons geometrically as close as possible to the original drawn polygons without regard to which polygons or even sections of polygons could impact electrical circuit performance if not reproduced correctly. This standard approach ignores a

significant amount of a priori information, and produces complex and expensive masks without necessarily addressing electrical performance variability to full extent. Subtle process-design interactions are not considered in the standard flow and therefore cannot be compensated for, limiting the usefulness of Optical Proximity Correction (OPC).

On the other hand, the simulation approach presented in this paper predicts electrical performance of circuits under specific layout and process configurations. A model-based automatic correction of process distortion based on our simulation approach seamlessly incorporates the electrical impact of process proximity and process variation. As a result, OPC is introduced at the design stage [5], thus creating a true Design-for-Manufacturing (DFM) flow.

V. Conclusions

We have demonstrated a novel simulation approach, which for the first time allows to study design-process interactions with a high degree of accuracy while being compatible with standard SPICE-type circuit simulators and compact device models. We show that design-process interactions can greatly influence all aspects of circuit operation and thus have to be considered as an integral part of the design flow. We illustrate critical importance of process-design interactions using the layout of a simple 2x2 AND-OR standard cell. Our methodology is general and can be easily applied to evaluate performance and manufacturability of virtually any analog, digital or mixed-signal design. Simulation times including litho simulation and model generation are on the order of seconds for the shown example.

References

[1] V. Axelrad, N. Cobb, M. O'Brien, V. Boksha, T. Do, T. Donnelly, Y. Granik, E. Sahouria, A. Balasinski, “Efficient Full-Chip Yield Analysis Methodology for OPC-Corrected VLSI Designs,” ISQED 2000, March 20-22, 2000, San Jose, California

[2] V. Axelrad and A. Shibkov, “Integrated DFM and Electrical Validation of an SRAM Cell,” SPIE 2004.

[3] SEQUOIA *Cell Designer Manual*, SEQUOIA Design Systems, 1998-2005

[4] V. Axelrad, A. Shibkov, G. Hill, Hung-Jen Lin, C. Tabery, D. White, V. Boksha, R. Thilmany, “A Novel Design-Process Optimization Technique Based on Self-Consistent Electrical Performance Evaluation,“ SPIE 2005, 27 February–4 March, 2005, San Jose, California

[5] V. Axelrad, A. Shibkov, V. Boksha, “Integrated scheme for yield improvement by self-consistent minimization of IC design and process interactions,” United States Patent Application 20050114822