Compact Modeling of Source-Side Injection Programming for 90nm-Node AG-AND Flash Memory

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***Abstract*— A compact model of source-side injection programming for AG-AND flash memory is presented. The lucky-electron model is used to formulate the hot electron injection current for programming. The lateral electric field is estimated using the pseudo-two-dimensional model considering the offset length between the assist-gate and the floating-gate. The proposed model is verified with device simulation and measurement results of 90nm-node AG-AND flash memory.**

I. Introduction

Significant market growth of mobile devices such as digital cameras and cellular phones has led to an increasing demand for higher speed and larger capacity flash memories. AG-AND flash memory[1][2] has two main competitive advantages: high programming speed and high density. High programming speed is achieved by utilizing an assist gate (AG) as the select gate (SG) for source-side injection (SSI) programming[3], while high density is achieved by assist gates being used in the formation of the bit line (BL) under them.

In the SSI programming, hot carriers created in the channel between SG and floating-gate (FG) are injected into the source side of the FG. Higher programming efficiency compared to conventional channel hot electron CHE programming is achieved by controlling the SG voltage and the FG voltage independently. The SG voltage is kept low to maximize the hot carrier generation rate, while the FG voltage is kept high to enhance injection probability.

In order to enable adequate optimization of flash memory cells, a reliable programming model is indispensable. Houdt *et al.*[4] simulated SSI programming characteristics with the lucky-electron model (LEM)[5], [6]. The peak lateral channel electric field E_m was treated as a fitting parameter in their work. Guan *et al.*[7] proposed a model for the electric field E_m which is proportional to the potential difference between FG and SG.

In this work, the pseudo-two-dimensional model[8] is extended to express the field E_m, which is used in the gate current formula based on the LEM. The proposed model is verified with device simulation and measurement results of 90nm-node AG-AND flash memory under various bias conditions.

II. Modeling

At SSI programming of AG-AND flash memory, channel electrons flow under the AGs and a selected word line (WL), as shown in Fig. 1. The inversion layers formed under the FGs on the left and right sides of AG1 are regarded as virtual source and drain for AG1, respectively, because the semiconductor surface under AG0, AG2, and the FGs under the selected WL is strongly inverted while the surface under AG1 is weakly inverted. The lateral electric field in the channel is the highest between AG1 and FG on the drain side (hereafter called the "offset region"). The generated hot electrons in the offset region are injected into the FG.

The LEM[5], [6] is used to estimate the injection rate of hot electrons into the gate electrode due to its simplicity and reasonable agreement with experimental results. The LEM starts from the assumption that the probability for an electron to be injected into the gate electrode is the product of the probability of the following independent events[6]: 1. the electron gains energy which is equal to or larger than the Si-SiO_2 energy barrier height from the lateral electric field, 2. the electron reaches the interface without suffering any collisions, and 3. the electron is not scattered back into the semiconductor in the oxide image-potential well. A further assumption that the injection probability is mainly determined by the first event lead to a gate current formula of[4] $I_\mathrm{gs} = I_\mathrm{ds} c_0 (\lambda E_\mathrm{m}/\Phi_\mathrm{b})^2 \exp(-\Phi_\mathrm{b}/(\lambda E_\mathrm{m}))$, in which E_m is the peak lateral electric field, λ is the electron mean free path, Φ_b is the effective Si-SiO_2 interface barrier height, I_ds is the drain current, and c_0 is the fitting parameter.

The peak lateral channel electric field E_m in the offset region will be formulated using the pseudo-two-dimensional model[8]. According to the pseudo-two-dimensional model, the channel potential and the lateral electric field in the velocity saturation region of MOSFETs are proportional to $\exp(x/L_\mathrm{c})$ with the characteristic length L_c. The velocity saturation region under AG1, which is labeled as "VSR1"

in Fig. 2, extends to the offset region because the electric field from the gate extends to the offset region. In the rest of the offset region, which is labeled as "VSR2" in Fig. 2, the lateral electric field remains constant $E_{\rm m}$ owing to a negligible vertical electric field. Defining $V_{\rm vdint}$ as the channel potential at the boundary between VSR1 and VSR2, the maximum electric field in VSR1 is expressed as $E_{\rm m} = ((V_{\rm vdint} - V_{\rm vs}) - V_{\rm dsat})/L_{\rm c}$, with drain saturation voltage $V_{\rm dsat} = (V_{\rm gs} - V_{\rm th})E_{\rm sat}L_{\rm ag1}/((V_{\rm gs} - V_{\rm th}) + E_{\rm sat}L_{\rm ag1})$ [8] and virtual source voltage $V_{\rm vs}$. The electric field in VSR2 is expressed as $E_{\rm m} = (V_{\rm vd} - V_{\rm vdint})/L_{\rm ofeff}$, where $V_{\rm vd}$ is the virtual drain voltage and $L_{\rm ofeff} = L_{\rm of} - L_{\rm fr}$. As a result, the maximum field at the offset region is formulated as

$$E_{\rm m} = ((V_{\rm vd} - V_{\rm vs}) - V_{\rm dsat})/(L_{\rm c} + L_{\rm ofeff}). \quad (1)$$

The extension length is estimated by the ratio of fringing capacitance $C_{\rm fr}$[9] and gate dielectric capacitance $C_{\rm ox}$ as $L_{\rm fr} \sim C_{\rm fr}/C_{\rm ox} = t_{\rm ox}(2/\pi)\log(1 + H_{\rm ag}/t_{\rm ox}) = 1.4t_{\rm ox}$.

The proposed model for $E_{\rm m}$ described by Eq. (1) is verified using device simulation. In the VSR1, the lateral field obtained by numerical simulation increases exponentially with the characteristic length $L_{\rm c} = 15{\rm nm}$, as shown in Fig. 3. The characteristic length $L_{\rm c}$ is shorter than that for typical MOSFETs, because $L_{\rm c}$ is proportional to the square root of the drain junction depth[8] and the depth of the virtual drain formed by the inversion layer is much shallower than the typical junction depth formed by the diffusion layer. In the VSR2, the lateral field remains constant, which agrees with the proposed model. The maximum electric field $E_{\rm m}$ at various drain and gate voltages calculated by this model agrees with the device simulation results, as shown in Fig. 4.

The effective barrier height $\Phi_{\rm b}$ has been found to be $\Phi_{\rm b} = \Phi_{\rm b0} - \beta\sqrt{E_{\rm ox}} - \theta E_{\rm ox}^{2/3}$[6]. The first term $\Phi_{\rm b0} = 3.2{\rm eV}$ is the Si-SiO_2 interface barrier. The second term represents the barrier lowering effect due to the image field, where $\beta = 2.59 \times 10^{-4}{\rm V}^{1/2}{\rm cm}^{1/2}$. The last term accounts for the probability of tunneling, where $\theta = 4 \times 10^{-5}{\rm V}^{1/3}{\rm cm}^{2/3}$. The vertical electric field in the oxide under FG $E_{\rm ox}$ is $(V_{\rm fg} - V_{\rm vd} - V_{\rm FB} - 2\phi_{\rm F})/t_{\rm oxfg}$, where $V_{\rm FB}$ is the flat-band voltage, and $\phi_{\rm F}$ is the Fermi potential.

III. Results and Discussion

Simulation was carried out on 90nm-node AG-AND flash memory with the proposed model. The AG-AND flash memory cell string is expressed by the equivalent circuit of Fig. 5. BSIM4[10] is used for the MOSFETs in the equivalent circuit. The gate current $I_{\rm gs}$ is inserted between the source and FG of each memory cell. Capacitances between FG and WL ($C_{\rm ono}$) and FG and AG (not shown in Fig. 5) are extracted from three-dimensional device simulation results. The mean free path for the LEM is set to $\lambda = 4{\rm nm}$ to fit measured programming characteristics. The value is close to the theoretical value of 5nm obtained by Monte Carlo simulation[11].

Simulated voltage and current transients at SSI programming are shown in Fig. 6. With the increase of the AG1 voltage, both the drain current $I_{\rm ds}$ and the gate current $I_{\rm gs}$ increase. The programming efficiency ($I_{\rm gs}/I_{\rm ds}$) exceeds 10^{-3} at the maximum gate current. As the programming proceeds, the FG voltage drops and the $I_{\rm gs}$ decreases, because the effective barrier height $\Phi_{\rm b}$ increases.

The simulated programming characteristics agree with measured data in the wide range of $V_{\rm ag1}$, as shown in Fig. 7. As $V_{\rm ag1}$ increases from 0V to 0.8V, both $I_{\rm ds}$ and $I_{\rm gs}$ increase and programming becomes faster, which is confirmed in Fig. 8. Beyond 0.8V, the programming speed is almost independent of $V_{\rm ag1}$, because programming occurs during ramping up and down, which is also confirmed in Fig. 8.

IV. Conclusion

A compact model of source-side injection programming for AG-AND flash memory has been presented. The hot electron injection current has been formulated using the LEM. The lateral electric field has been estimated using the pseudo-two-dimensional model considering the offset length between the assist-gate and the floating-gate. The proposed model has been verified with device simulation and measurement results of 90nm-node AG-AND flash memory.

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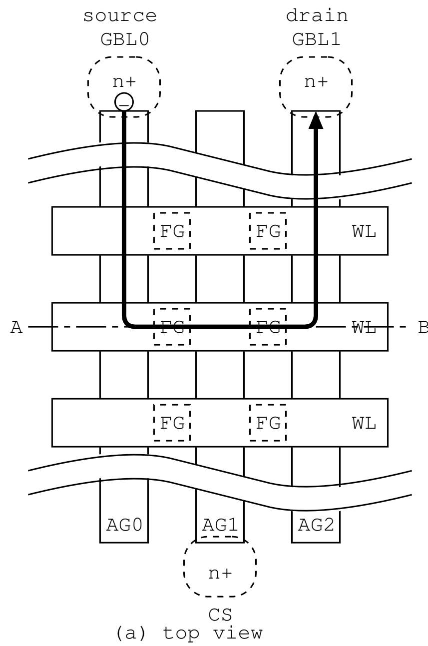


Fig. 1. Schematic of memory cell array of AG-AND flash memory.

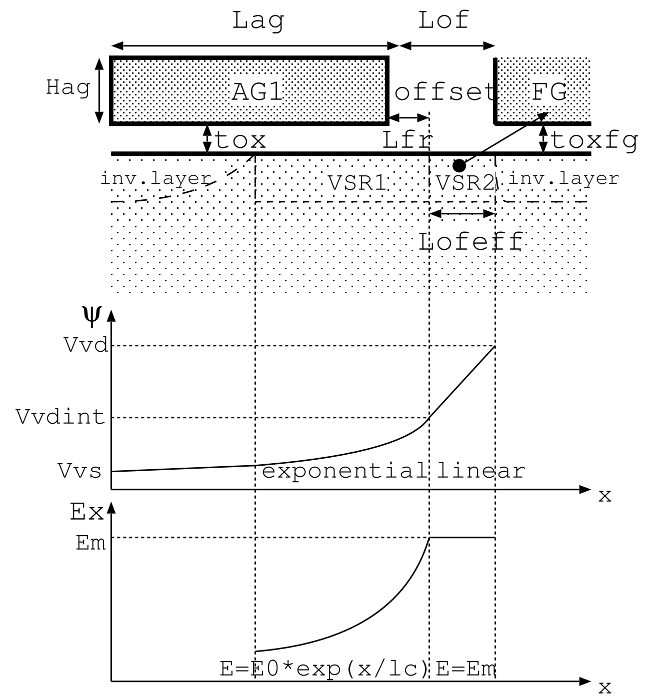


Fig. 2. Schematic of channel potential and electric field. The velocity saturation region (VSR) is divided into two regions, VSR1 and VSR2.

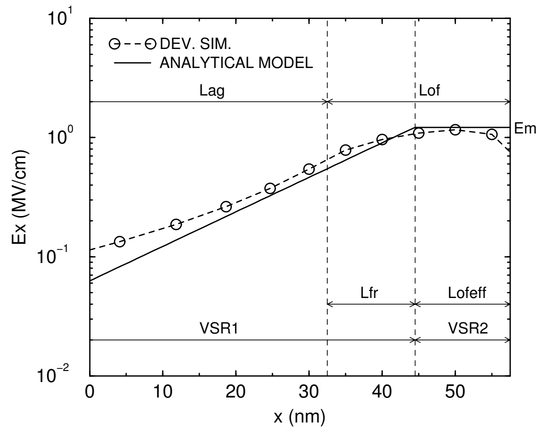


Fig. 3. Lateral channel electric field distribution at Si-SiO_2 interface.

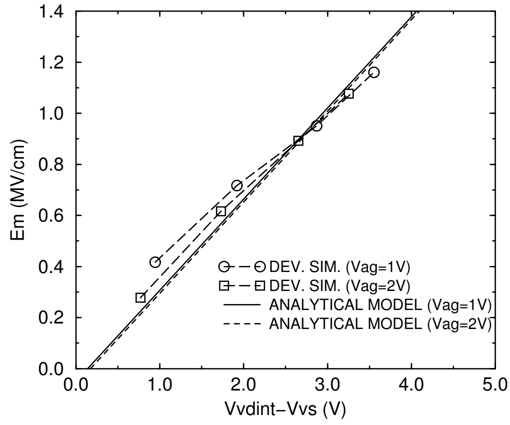
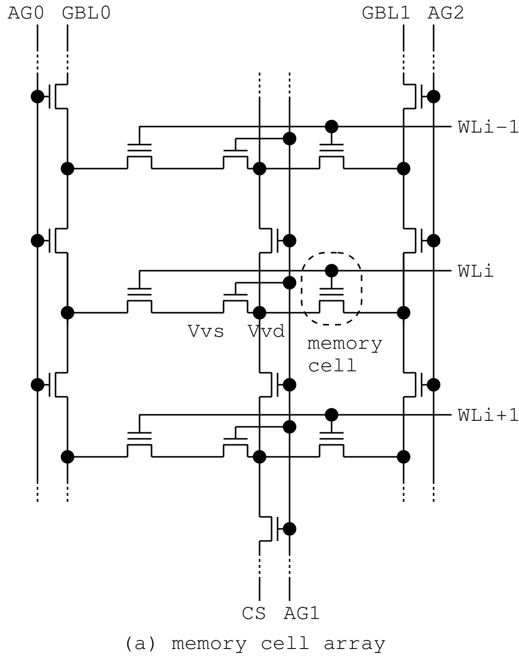


Fig. 4. Maximum lateral channel electric field at Si-SiO$_2$ interface as a function of internal virtual drain-source voltage $V_{\rm vdint} - V_{\rm vs}$. $V_{\rm vdint}$ is the channel potential at the boundary of VSR1 and VSR2.



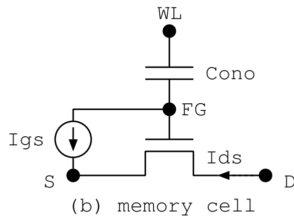


Fig. 5. Equivalent circuit of AG-AND flash memory cell array. Capacitance between FG and AG (not shown) is also included in the equivalent circuit. The CS node is floating under the programming conditions shown in Figs. 6–8.

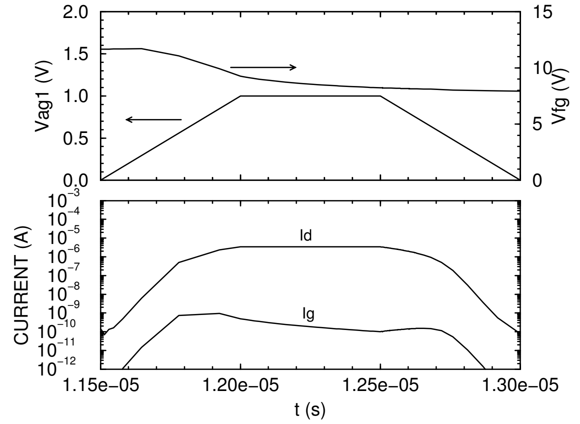


Fig. 6. Simulated voltage and current transients at SSI programming. Voltages of nodes AG0, AG2, and GBL0 are 5V, 8V, and 0V, respectively.

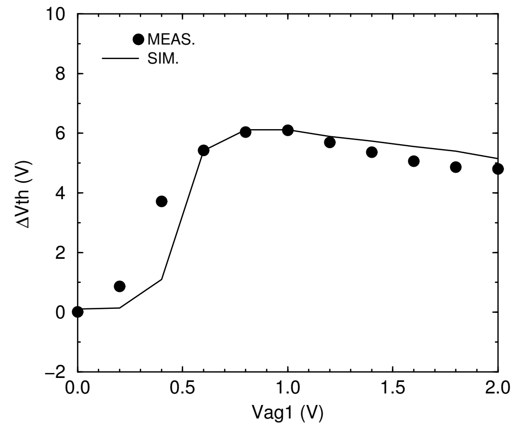


Fig. 7. Measured and simulated SSI programming characteristics.

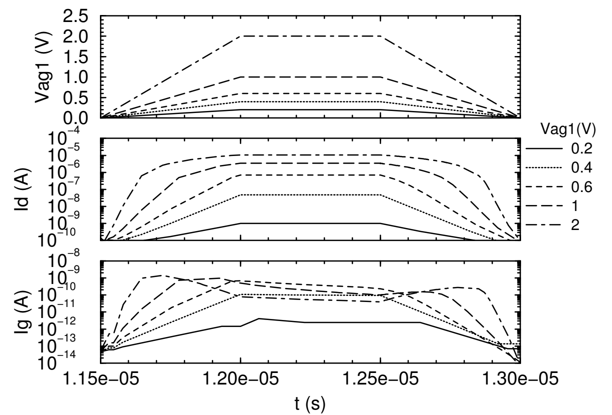


Fig. 8. Simulated voltage and current transients for several AG1 voltages at SSI programming. Voltages of nodes AG0, AG2, and GBL0 are 5V, 8V, and 0V, respectively.