Measurement and Simulation of Interconnect Inductance in 90 nm and Beyond

Xiaoning Qi, Alex Gyure, Yansheng Luo, Sam C. Lo, Mahmoud Shahram, and Kishore Singhal

Direct Silicon Access Lab, Synopsys Inc.
700 E. Middlefield Road, Mountain View, CA 94043, USA
E-mail: xiaoning.qi@synopsys.com

***Abstract* - The on-chip inductance impact on signal integrity has been a problem for designs in deep-submicron technologies. The impact increases clock skew, max-timing and noise levels of bus signals. In this paper, circuit macro-models are benchmarked against test chip measurement in a 90 nm technology. Circuit simulations show the inductive impact on clock skew (e.g., 11ps in 2GHz clock frequency), signal delay (e.g., 11% max-timing push-out) and noise levels (e.g., 13%VDD). In addition, the inductive impact on signal integrity in the presence of process variations is evaluated. Finally, inductive impact in 65nm and 45 nm technologies is simulated, which indicates that the inductance impact will not diminish as technology scales.**

I. INTRODUCTION

The inductive impact on timing and noise of ultra-high frequency designs has been a challenge for technologies below 0.25 μm [1]-[5]. The inductance impact increases clock skew, max-timing of bus signals, and noise levels of bus signal and power/ground grids. In nanometer technologies, interconnects become more resistive and capacitive due to smaller wire widths and pitches, which may potentially alleviate the inductance effects. However, faster signal rise and fall times inevitably increase *di/dt* and inductive effects. Evaluation of the inductive impact in the 90 nm technology and beyond is necessary for a proper understanding of signal and power grid integrity for high performance chip designs. In addition, process variation is becoming a major issue for nano-meter technologies [6]-[8]. Intra-die and inter-die device and interconnect variations add another dimension to clock and signal timing uncertainties, and it is worth investigating the inductive impact on signal integrity in the presence of process variations.

In this paper, measurement and simulation data are presented for a test chip in a 90 nm technology. Interconnect *RLC* extraction and circuit macro-models are benchmarked against the measurement data. Circuit simulations show that the inductive impact on clock skew and signal timing are not alleviated relative to the 130 nm technology, and that impact on noise becomes even larger. Inductance impact is also evaluated with interconnect process variations, which reveals that inductance impact dominates the process variation impact. Finally, inductance impact on signal timing in future technologies (65 nm and 45nm) are studied based on the 2004 International Technology Roadmap for Semiconductors (ITRS'04) [8]. Results predict that the inductance impact is still significant as technology scales. In this paper, inductance impact on power grids and device process variations are not discussed. The paper is organized as the following. Measurement and simulation of a test chip in a 90 nm technology is outlined in Section II. Inductance impacts on signal delay and noise with interconnect process variations are simulated in Section III. Section IV presents the inductance impact in future technologies, and Section V summarizes the paper.

II. MEASUREMENT AND SIMULATION OF TEST STRUCTURES IN A 90 nm TECHNOLOGY

A. Test Structures and Measurement Data

A test chip was designed and manufactured in a 90 nm process technology. Four on-chip interconnect structures include a signal wire with symmetric 2-return, 8-return, 16-return and 32-return ground wires in M9. The purpose of the structures is to analyze frequency dependence of return currents and wire inductance, and to calibrate *RLC* extraction/simulation. Fig. 1 shows one of the test structures with eight ground wires as current return paths. On-wafer testing was performed using a network analyzer to extract *S*-parameters of the test structures. An open structure is also measured so that *S*-parameters are de-embedded from environmental parasitic elements. In Fig. 2, the measured *S*-parameters with

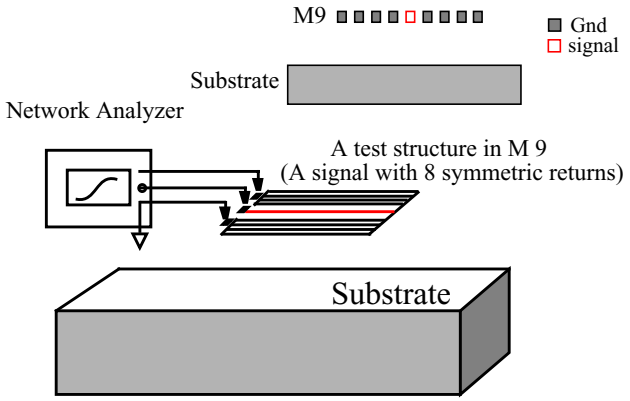

Fig. 1. A test structure in M9 and network analyzer to measure the *S*-parameters. *S*-parameters can be converted to Y-parameters. Inductance and resistance can also be extracted from S-parameters.

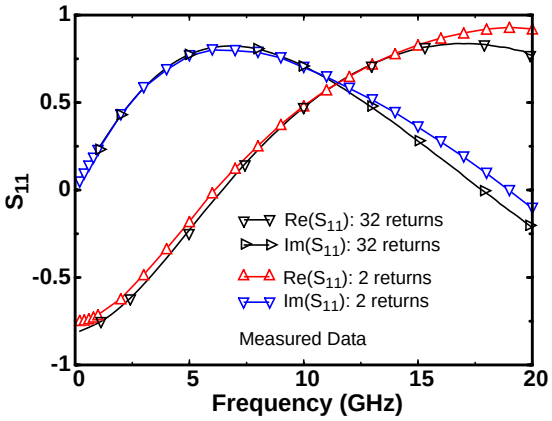

Fig. 2. Measured data: de-embedded real and imaginary parts of S_{11} for the 32-return structure and the 2-return structure (M9: width and spacing are 10 μm).

the 32-return paths and the 2-return paths are plotted. It can be seen from the plot that the imaginary and real parts of the *S*-parameters have differences at low and high frequencies, primarily due to skin and proximity effects. At low frequencies, currents tend to spread out and return from multiple ground wires to minimize overall resistance. At high frequencies, currents tend to return from nearest return ground wires to minimize inductance loop. Both skin and proximity effects result from eddy currents [9]. In addition, it is easier to see the low frequency difference in a converted Y-parameters plot, shown in Fig. 3. The 32-return structure is less resistive and more inductive at low frequencies, and converges to the 2-return structure at 3 GHz. In order to reduce inductance effect at high frequencies and to reduce resistance at low frequencies, it is beneficial to have multiple ground wires or ground grid structures in chip designs.

B. RLC Extraction of Test Structures

Test structures are used to validate simulated resistance, inductance and capacitance, and circuit macro-models to be used in circuit simulations. Simulated resistance, inductance and capacitance are extracted using RAPHAEL. Wire *RLC* circuit macro-models, namely π-models, are built, and their *S*-parameters are compared with measured data. The wire

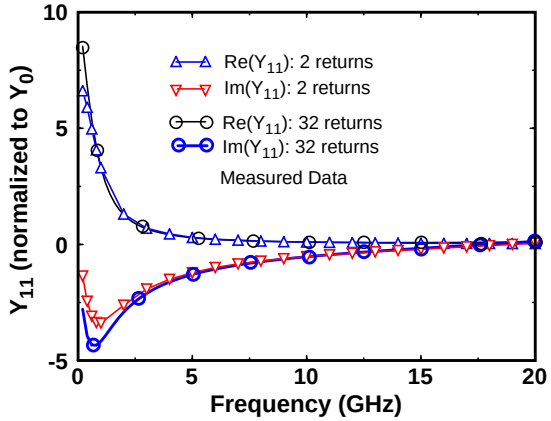

Fig. 3. Converted Y-parameters from measured data: the 32-return structure is less resistive and more inductive at low frequencies because of more parallel returns and a larger loop.

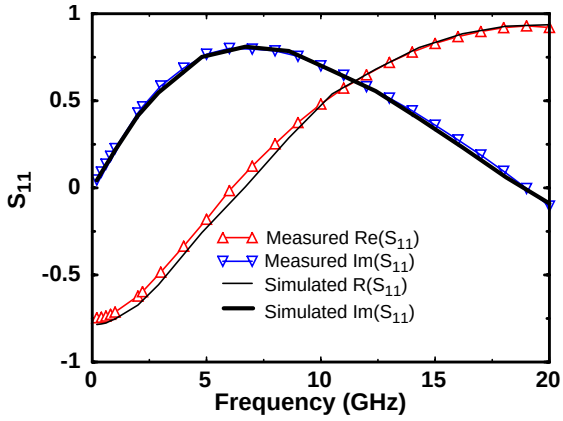

Fig. 4. The measured data and simulation are in very good agreement (the 2-return structure). The substrate is included in *RLC* extraction.

model includes wire resistance, self- and mutual inductance of all wires, and self- and coupling capacitance of all wires. Substrate is also included in *RLC* extraction so that wire capacitance to substrate and any return currents through the substrate are included. HSPICE is used to simulate the *S*-parameters of the circuit model of test structures. In Fig. 4, simulated *S*-parameters and measured data match very well up to 20 GHz with relative errors less than 5%. It validates the circuit macro-models and simulated *RLC* values. These accurate models make it possible to study the inductive impact on circuit design (e.g., signal integrity) and establish design guidelines to deal with inductive impacts on timing and noise for interconnects in the 90 nm technology.

III. SIMULATION FOR INDUCTIVE IMPACTS AND PROCESS VARIATIONS IN 90 nm TECHNOLOGY

A. Signal Integrity Analysis for Clock and Bus Signals

To investigate inductive impact on timing and noise in the 90 nm technology, clock and bus signals are studied. A major concern for clocks in digital circuits is uncertainty or skew. Clock signals are usually shielded with two or more ground wires. The co-planar waveguide is a commonly used configuration. An approximation can be made to assume that clock current returns only through the two co-planar ground wires. However, if some parallel bus signals happen to run nearby, inductive couplings between bus and clock signals can cause extra clock uncertainties due to the transitions of bus signals. Fig. 5 illustrates a co-planar waveguide clock that happens to have seven parallel bus signals running below. HSPICE time domain simulations using validated circuit models show that there is significant clock variation due to inductance, i.e., 11 ps for a 2 GHz clock. For a 2 GHz clock, the clock skew budget is typically 30 ps, which means 11ps clock uncertainty from inductive coupling would be a serious problem for clock distribution. In the simulation, a large driver is used for the clock wire in M6 to generate the 2GHz clock frequency, while smaller drivers are usually used for bus signals. The clock timing is measured at the

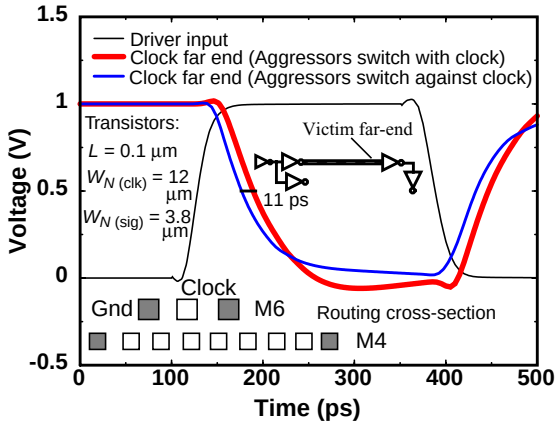

Fig. 5. A 2 GHz clock signal in M6 has a variation of 11 ps due to inductive impact from M4 parallel routing bus signals. Wires are 1.5 mm long.

clock far-end with two bus switching directions -- bus signals simultaneously switching with the clock (slowing down the clock due to inductance) and bus signals simultaneously switching against the clock (speeding up the clock due to inductance). It is obvious that more shielding wires are needed in M4 to better isolate the clock signal from bus signals in order to reduce inductance impact.

Inductive impact on noise and delay is also an issue for bus signals since they could switch simultaneously, thus maximizing inductive impact. For bus signals, an inductive noise of 13% VDD in the victim signal is observed. This is mainly because the wire pitches are smaller and gates switch faster in 90 nm. If the nearest two neighbors of the victim switch against other aggressors, the capacitive and inductive noise can superimpose to produce yet larger noise. The noise is measured at the far-end of a victim signal (M6) with seven bus signals switching in M6, see Fig. 6. In addition, inductive couplings among bus signals can also make the stage delay of a bus victim signal larger. The stage delay is the delay from the input of a victim driver to the input of a victim receiver. The push-out is defined as (*RLC*_stage_delay - *RC*_stage_delay)/*RC*_stage_delay. The max-timing delay push-out can be obtained when all aggressors switch with the victim signal simultaneously. For typical bus structures in the 90 nm technology (e.g., a fully-shielded 16-bit bus), the max-timing push-out is about 11%. Circuit designers need to account for this extra delay due to inductance effect.

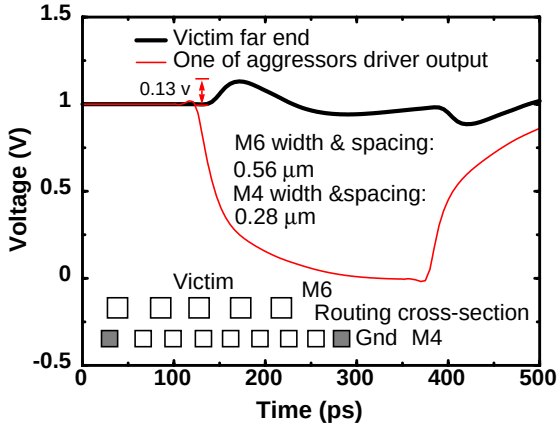

Fig. 6. A signal in M6 has pure inductive noise of 0.13 v when seven aggressors switch below at the same time. If nearest neighbors of the victim switch down, totally noise can be larger.

B. Inductance Impact in the Presence of Process Variations

Process variations become increasingly important in the 90 nm technology and beyond, which may have an impact on signal and power integrity [10]. Inductance is a weak function of wire geometry as shown in the following simple analytical formula for self-inductance of a rectangular cross-section wire,

$$L_{self} = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{(w+t)} + \frac{1}{2}\right] \qquad (1)$$

where l, w, and t are wire length, width and thickness, respectively. μ_0 is the permeability. Taking the derivative with respect to width, w,

$$\frac{\partial L_{self}}{\partial w} = \frac{-\mu_0 l}{2\pi(w+t)} \qquad (2)$$

For a 1000 µm long wire with width and thickness of 1µm respectively, the variation is 0.1 nH/µm of width. For example, if there is 50% width reduction, there will be only about 3.4% inductance increase. However, if the clock wire width reduces, and results in 10% of capacitance reduction and 10% resistance increase, the clock variation can increase by 18% due to the inductive impact based on the simulation of test structures in Fig. 5. This is due to the fact that reduced capacitance actually magnifies inductance impact.

IV. INDUCTIVE IMPACTS IN FUTURE TECHNOLOGIES

For technologies below 0.25 µm, the inductance impact increases clock skew, max-timing and noise levels of bus signals. In the nanometer technologies, interconnects become more resistive and capacitive due to smaller wire widths and pitches, which may alleviate inductive impact. However, faster signal rise and fall times increase *di/dt* and inductive effects. It is important to evaluate the inductive impact on signal and power grid integrity for high performance chip designs in 90 nm technology and beyond.

Following a similar methodology to that used in [2] which predicted the inductive effect down to the 130 nm technology node, simulations are performed for 130 nm, 90 nm and 65 nm and 45 nm technology nodes (ITRS'04). Fig. 7 shows the *RC* and *LC* delay estimation of a co-planar clock wire in M8 for the 90 nm node. In the wire length range of 2.5 mm (*Len1*) to 9.5 mm (*Len2*), it illustrates that *RC* delay estimation is faster than the speed of light, which is not physical. It simply means that inductance needs to be included in the wire model, otherwise the wire delay will be underestimated. For wire length smaller than 2.5 mm, gate delay dominates. However, studies show that inductance is needed for bus noise analysis for any wire length longer than 500 µm [10]. Based on published data and the data in ITRS'04, *RLC* extractions are performed to calculate *Len1* and *Len2* for

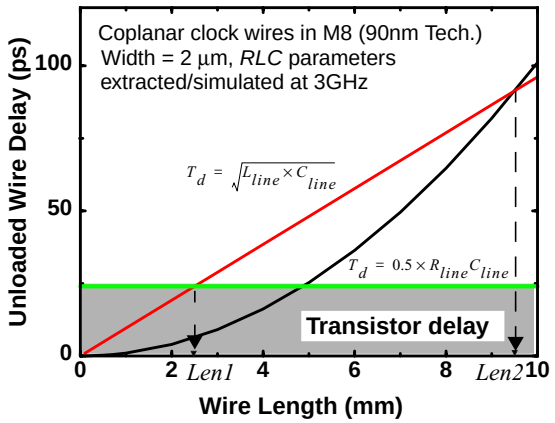

Fig. 7. For the 90 nm technology, in the range of 2.5 mm to 9.5 mm wire length, *RC* delay estimations underestimate wire delays.

130nm, 90nm, 65nm and 45nm technology nodes. Fig. 8 plots *Len1* and *Len2* which predicts the wire range where delay will be underestimated if inductance effects are not included in timing analysis. This range for future technologies, shown in Fig. 8, indicates that inductive impact will not diminish as technology scales. Table I lists the related process data used to extract the resistance, inductance and capacitance in various technologies.

V. CONCLUSIONS

In this paper, it is shown through measurement and simulation that there is significant impact due to inductance on timing and noise in the 90 nm technology and beyond. The extracted *RLC* interconnect circuit models are benchmarked against measured data from a test chip. Circuit simulations using these models reveal significant inductive impact on clock skew, bus signal noise and max-timing. In addition, inductance impact with process variations is evaluated. Finally, inductance impact on delay for future technologies are predicted based on the extraction and calculation of process data from ITRS'04. The analysis shows that inductive impact on interconnect delay and cross-talk will not be alleviated in the 65nm and 45nm technologies. High performance designs need to address these issues effectively, e.g., to provide complete shielding to clocks and create inductance-aware wire classes.

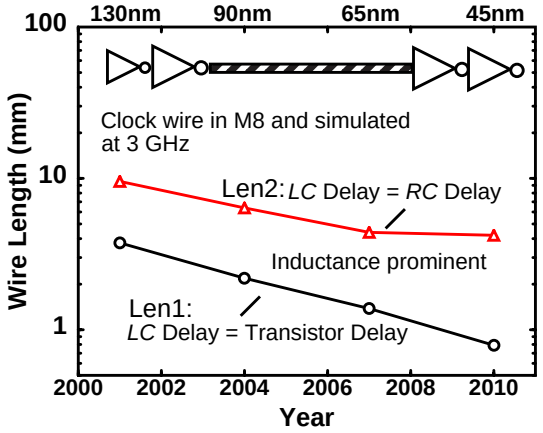

Fig. 8. For each technology node, any coplanar clock wire of length below the Len2 line and above the Len1 line will see inductance impact on delays.

TABLE I PROCESS DATA AND SIMULATED *RLC* VALUES

Year and Technology	2001 130 nm	2004 90 nm	2007 65 nm[1]	2010 45 nm[1]
NAND Switching τ	36.27 ps	23.94 ps	16.23 ps	9.88 ps
MPU[2]/ASIC M1 1/2 Pitch	150 nm	107 nm	76 nm	54 nm
ε_r	3.3	3.3	2.9	2.4
Metal Thickness	1.14 µm	0.8 µm	0.56 µm	0.39 µm
Wire C_{total}	208 fF/mm	248 fF/mm	272 fF/mm	292 fF/mm
Wire R_{sq}	2.2 µΩ-cm	2.2 µΩ-cm	2.2 µΩ-cm	2.2 µΩ-cm
Wire R @ 3 GHz	9.74 Ω/mm	13.81 Ω/mm	19.69 Ω/mm	20.24 Ω/mm
Wire Loop L @ 3 GHz	0.45 nH/mm	0.48 nH/mm	0.51 nH/mm	0.53 nH/mm

[1] From the ITRS'04. [2] MPU: for high-volume microprocessor.

REFERENCES

[1] A. Deutsch, P. W. Coteus, G. V. Kopcsay, H. H. Smith, C. W. Surovic, B. L. Krauter, D. C. Edelstein, and P. J. Restl, "On-chip wiring design challenges for gigahertz operation," *Proc. IEEE*, vol. 89, pp. 529, April 2001.

[2] P. J. Restle, "High speed interconnects: a designers perspective," *ICCAD'98 Tutorial: Interconnect in high speed designs: problems, methodologies and tools,* Nov. 1998.

[3] X. Qi, B. Kleveland, Z. Yu, S. S. Wong, R. W. Dutton, and T. Young, "On-chip inductance modeling of VLSI interconnects," *IEEE International Solid-State Circuits Conference*, pp. 172, 2000.

[4] B. Kleveland, X. Qi, L. Madden, T. Furusawa, R. W. Dutton, M. A. Horowitz, and S. S. Wong, "High-frequency characterization of on-chip digital interconnects," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 716-725, June 2002.

[5] Y. Massoud, J. Kawa, D. MacMillen, and J. White, "Modeling and analysis of differential signaling for minimizing inductive cross-talk," *Proc. of Design Automation Conference*, pp. 804-809, June, 2001.

[6] K. Bowman, S. Duvall, and J. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 2, Feb. 2002.

[7] P. Zuchowski, P. Habitz, J. Hayes, and J. Oppold, "Process and environmental variation impacts on ASIC timing," *The Tech. Digest of ICCAD'04*, pp. 336-342, Nov. 2004.

[8] Semiconductor Industry Association, "International technology roadmap for semiconductors 2004 (ITRS'04)," *http://public.itrs.net*.

[9] H. H. Skilling, "Fundamentals of Electric Waves," John Wiley & Sons, New York, NY, 1948.

[10] X. Qi, S. C. Lo, Y. Luo, A. Gyure, M. Shahram, and K. Singhal, "Simulation and analysis of inductive impact on VLSI interconnects in the presence of process variations," to appear in the *IEEE Proceedings of Custom Integrated Circuit Conference*, Sept. 2005.