Three Dimensional CMOS Image Sensor Cell Simulation and Optimization

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Abstract

In this work, we present the results of three-dimensional CMOS image sensor cell simulation. Electrical characteristics of the device are represented comprehensively. The methodology, describing saturation, charge-voltage conversion, and image lag of a CIS cell in a single simulation analysis, is expected to play a key role in future CMOS image sensor cell development.

Introduction

The analysis of CMOS Image Sensor (CIS) cell operation requires a three-dimensional study of the device. Photo-diode electron capacity requires a volume integration and voltage conversion of the floating diffusion region has many three dimensional capacitive effects that must be considered.

Previously varieties of heuristics were performed to obtain a three dimensional doping profile; some extended 1D or 2D doping profiles (simulated or measured), or assumed the doping profile follows a known distribution function and "drew" it in. Both approaches yield poor three-dimensional doping descriptions.

In this contribution, we provide simulation results and analysis done by full 3D process simulation that includes three of the four transistors and the photodiode in one three-dimensional block of virtual silicon.

With this simulation methodology, we look at CIS electron capacity (amount of electrons that the photodiode can hold), saturation (the output signal level after transfer when photo-diode is completely full before transfer), capacitance of floating diffusion area, and image lag.

Simulation Domain

Full 3D process simulation is performed on a domain that include the photodiode (PD), floating diffusion (FD), source follower amplifier (SF), the reset transistor (Rx), and the transfer transistor (Tx), and a layer of metal that connect FD, SF and Rx, see Fig. 1 for simulation domain and Fig. 2 for simulation flow.

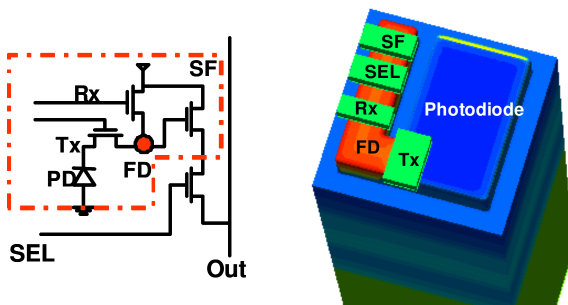

Fig. 1 a): Simulation domain (dotted box). Includes all of CIS APS cell minus the selection transistor. b): A mock 3D CIS device similar to ones that were used in this work.

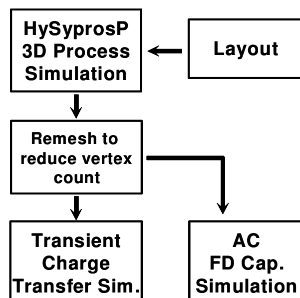

Fig. 2. a) Simulation flow: extract mask from layout, process sim. (HySyprosP), remesh (noffset3D), devie simulation (DESSIS). b) an example of resulting 3D CIS structure.

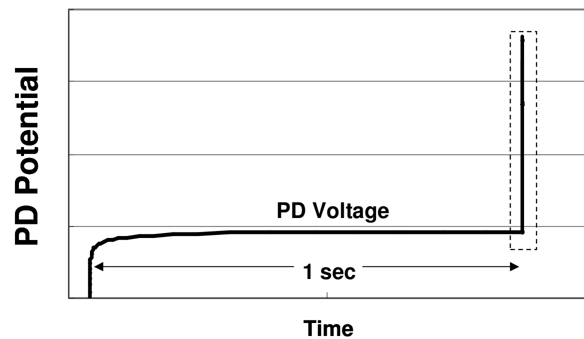

Fig. 3 a) Time evolution of the photodiode potential prior to electron transfer, 1 second is allowed for excess electrons in the photodiode to drain out.

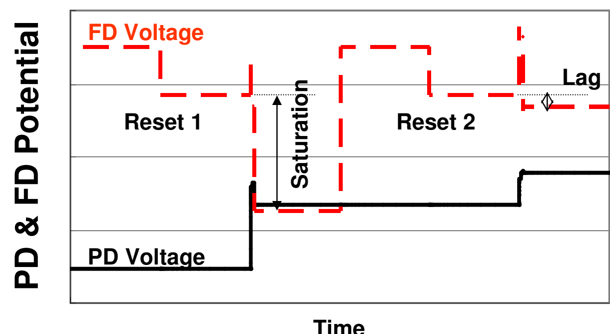

Fig. 3 b) Time evolution of the FD and PD potentials during primary (saturation), and secondary (lag) electron transfer, representing in detail the events that are transpiring in the dotted box in Fig. 3 a).

AC Analysis

Floating diffusion capacitance is an important characteristic determining charge to voltage conversion of CIS. AC analysis on the floating diffusion is performed, and the total value of capacitance is found to be in good agreement with the experimental measurement (Table 1).

Table 1. Normalized floating diffusion capacitance.

Normalized C_{FD}	
Measure	Simulation
1.00	0.97~1.05

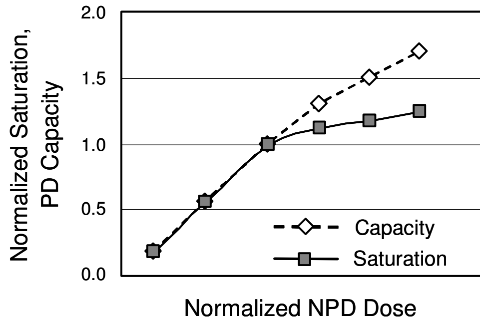

Fig. 4. Electron capacity of photodiode and saturation as functions of NPD implantation dose, Saturation shows a 2 state behavior suggesting lag

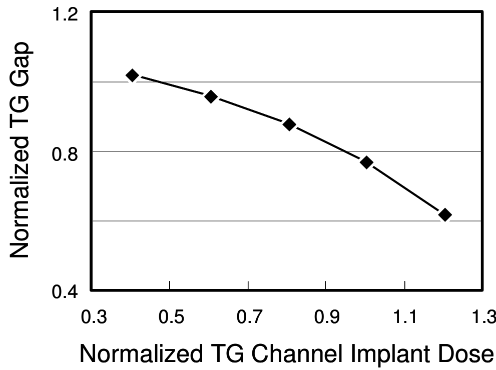

Fig. 5. TG gap as a function of TG channel implantation dose. Less p-type doping present, greater the opening under TG.

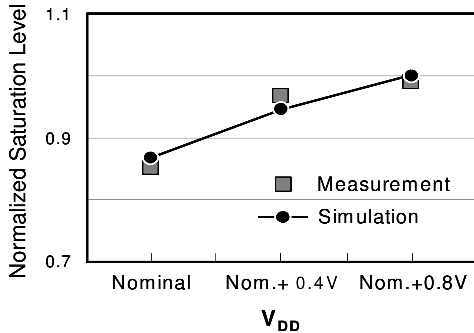

Fig. 6. Change of the saturation level for various V_{DD}. Significant Additional output suggests incomplete transfer of PD electrons

The contributions of metal interconnect to floating diffusion capacitance take a significant portion of the total capacitance and all relevant metallic layers must be included in the simulation to obtain accurate results.

Transient Charge Transfer Simulation

A. Nominal Condition

Given an initial condition where the photodiode is completely filled with electrons, the Tx and Rx are operated to mimic CIS cell operation. The time evolution of floating diffusion and photodiode voltage can be seen in Fig. 3a and Fig. 3b.

Table 2. Saturation condition output level.

	Measured	Simulated
Saturation (discretization level)	729	693

Saturation level depends on a few factors; 1) total electron capacity, 2) FD capacitance, and 3) Tx gap - the amount of lowering of potential barrier between PD and FD when Tx gate is biased high. The first item depends on the net doping in PD and under Tx, this is not measurable, see Fig. 4 for simulated results. The second is looked into via the previous AC analysis. Third item depends on net doping between PD and Tx channel surface, and can change drastically by varying the p-type implantation dose around Tx (Fig. 5).

The above are three dimensional effects that require precise three dimensional doping descriptions for a quantitatively accurate simulation results.

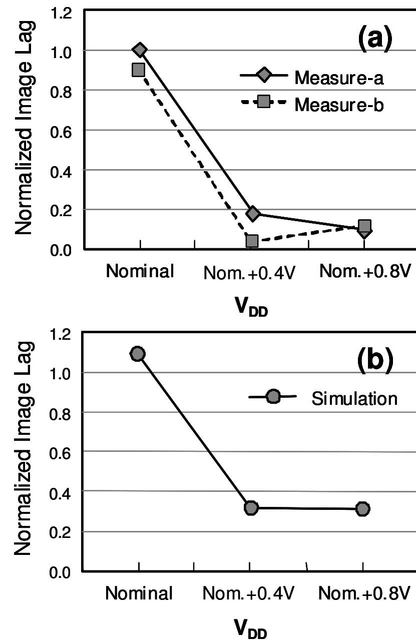

Fig. 7. Comparison between (a) measured and (b) simulated image lags. Simulation and experiments are done by operating CIS twice without supplying addition electrons to PD between the two operations, i.e. 2nd operation done under no illumination.

Vast majority of the electrons in PD drift out almost immediately after Tx lowers the potential barrier between PD and FD, see Fig. 8a. If Tx gap does not open sufficiently to allow full emptying of PD, there is a charge neutral region at the bottom of PD where the gradient of electron quasi Fermi level is very small. Electrons diffuse out very slowly from this region, which is the cause of image lag, see Fig. 8b.

B. Image Lag Simulation

The amount of electrons still left in PD after a charge transfer to FD cannot be measured directly. However, one could simply operate the CIS twice starting from a full PD with no additional optical illumination. The voltage output can be easily measured and an identical operation can be performed virtually in simulation.

When V_{DD} was changed from its nominal value in increments of 0.4V, simulations were able to describe the additional output signal from higher V_{DD} with good accuracy, see Fig. 6.

Simulations were also able to describe the voltage outputs from secondary transfers (Fig. 7a and Fig. 7b), satisfactorily reproducing the image lag phenomenon in transient detail.

C. PD Implant Dose Optimization

With the knowledge that the CIS cell had some image lag problem a simulation split was made over the photodiode N-type (NPD) implantation dose to determine the dose at which image lag disappears.

A clear two state behavior was found where in one state the dose is sufficiently low and all the additional dose is translated into output saturation level, in the other state additional dose show a reduced increase in output saturation level.

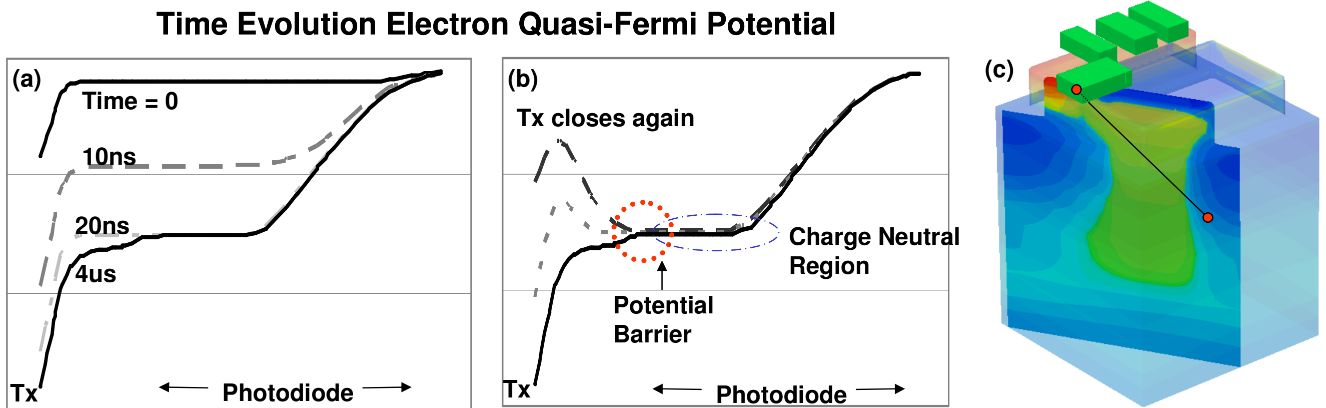

Fig. 8. Spatial plot of electron quasi Fermi potential for various time steps in CIS operation. Figures show the electrons being drained out of PD region graphically during main transfer (a) showing saturation, and secondary transfer (b) showing lag. The spatial location of (a) and (b) is noted in (c) by the line

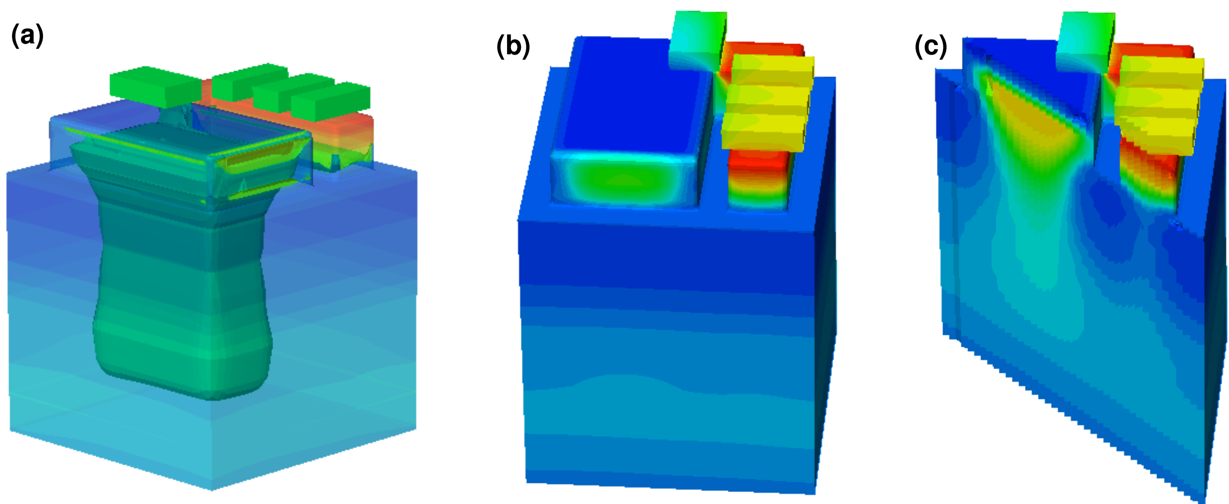

Fig. 9. Visualization of 3D mock CIS similar to ones used in this work: a) Photodiode shape (junction iso-surface), b) electrostatic potential at the exterior, and c) electrostatic potential at the interior.

Without giving up too much in saturation level or total electrons transferred, one could find a lag free process, as shown in Fig. 4, which is the dose at which behavioral change occurs.

Conclusions

In conclusion, three dimensional comprehensive simulation of CIS cell's electrical behavior is performed, including AC analysis of FD, electron capacity of PD, transient charge transfer simulation, and image lag simulation. Image lag mechanism is discussed, and simulation based optimization is performed over NPD dose. Overall, simulation results closely reproduce those of experiments.

References

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