ESD Protection Design Optimization Using a Mixed-Mode Simulation and Its Impact on ESD Protection Design of Power Bus Line Resistance

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Abstract **- This paper presents a new optimization method of ESD protection design using a mixed-mode ESD simulation with a calibrated model based on DC and TLP characteristics. As a result, the influence of power bus line resistance on ESD protection design is clarified using the calibrated model for each device used in ESD protection circuit. ESD surge flows into an internal circuit easily as the value of the power bus line resistance increases even if the ESD tolerance of a power clamp element is high enough.**

I. Introduction

In order to check ESD protection capability, the transmission line pulsing (TLP) measurement is widely used as standard approach [1]. TLP measurement provides insight into ESD failure threshold and I-V characteristics during a short time that self-heating does not cause. Although it is possible to check the ESD operation of each device using by TLP measurement, investigation of ESD operation on the circuit network considering current path to clamp ESD current is difficult. The combined use of a TLP measurement and simulation for data complement and the physical analysis is necessary for optimization of ESD protection design.

In this paper, we describe optimization method of ESD protection design based on the combined use of TLP measurement and simulation. We investigate influence of power bus line resistance on ESD protection design.

II. A New ESD Protection Design Methodology Using a Mixed-Mode Simulation

An ESD protection test circuit under our study is shown in fig. 1. pMOS triggering SCR as power clamp [2] is shown in fig.2. Fig.3 shows the conceptual figure for ESD protection design using a mixed-mode simulation [3]. The model parameters of impurity profile and carrier mobility are extracted from DC characteristics [4]. Test element group (TEG) with a series of size of the device such as channel length (L) and width (W) is prepared to obtain ESD parameters of each device used in ESD protection circuit. The ESD parameters include the breakdown voltage (V_{t1}), the holding voltage (V_{hold}), the slope of snapback characteristics (R_{on}) and the destructive current (I_{t2}). They are extracted by the TLP measurement. The other model parameters are calibrated for these ESD parameters. Calibrated model parameter set is used to optimize the circuit network. Optimization information is reflected in the layout design.

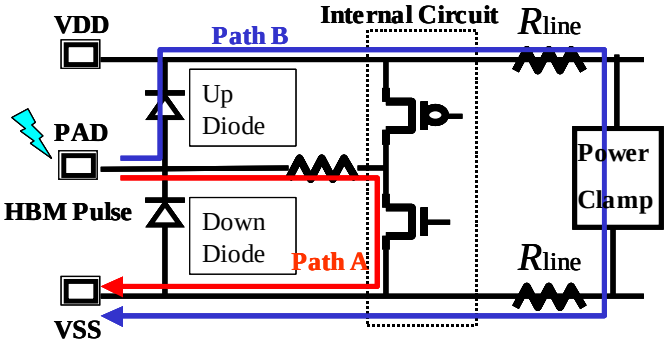


Fig.1 ESD test protection circuit diagram.

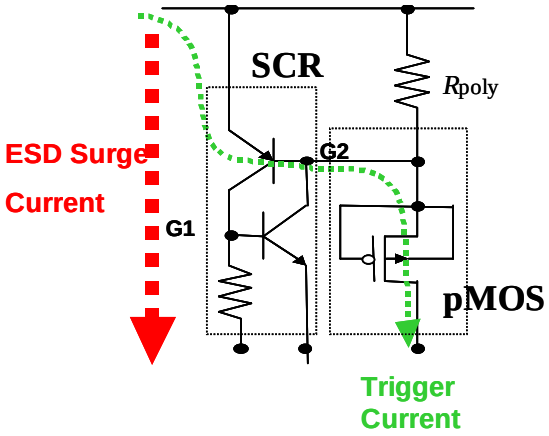


Fig.2 Circuit diagram of power clamp with pMOS triggering SCR.

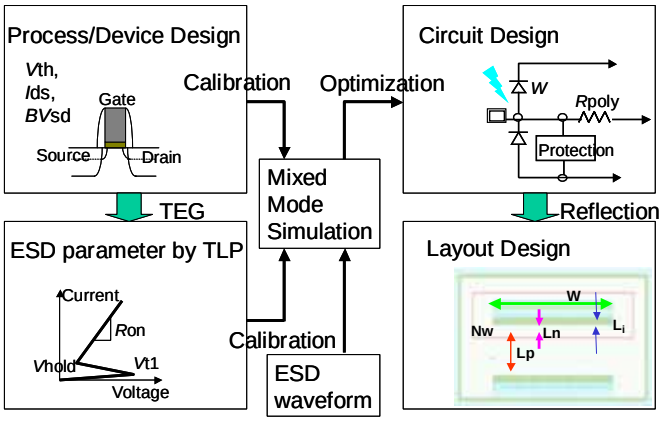


Fig.3 Conceptual figure of ESD protection design methodology.

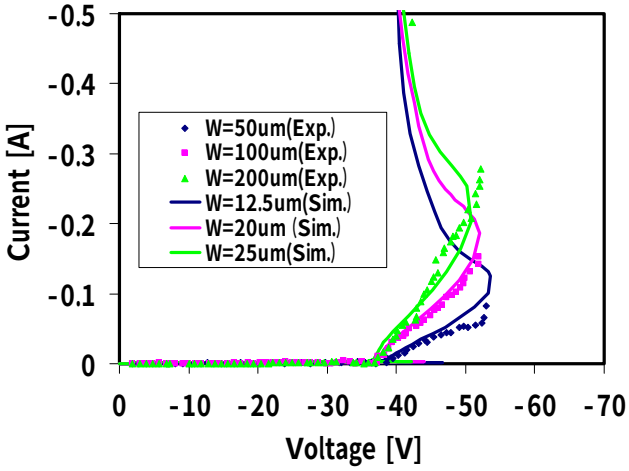
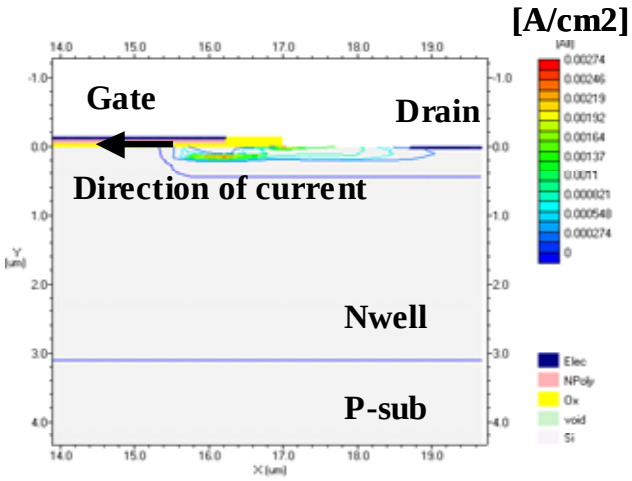
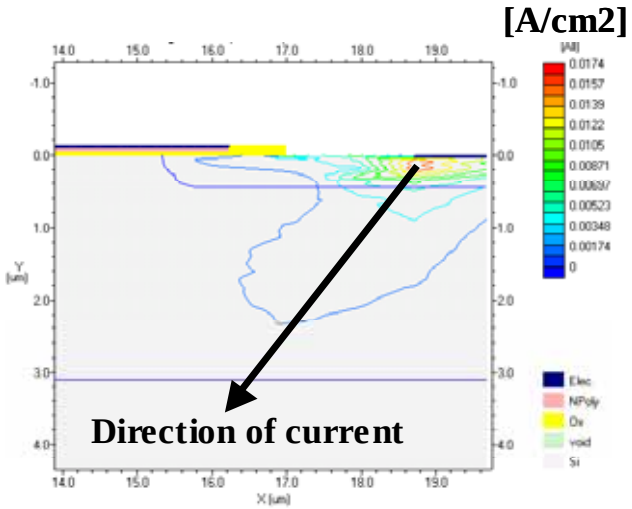


Fig.4 Snapback characteristics in pMOS.



(a) Region A



(b) Region B

Fig.5 Distribution of hole current density.

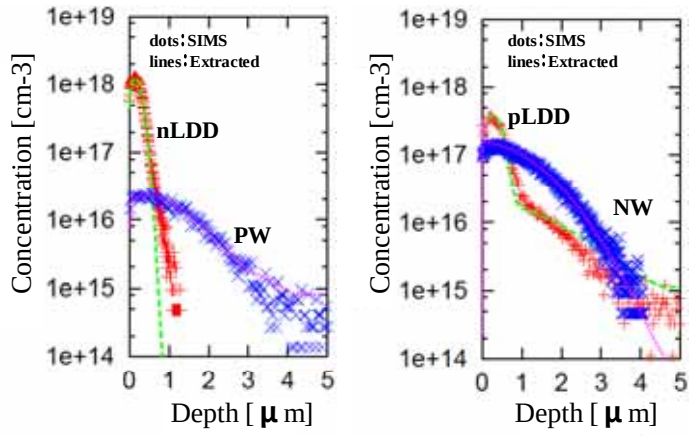


Fig.6 Impurity profiles extracted from SIMS.

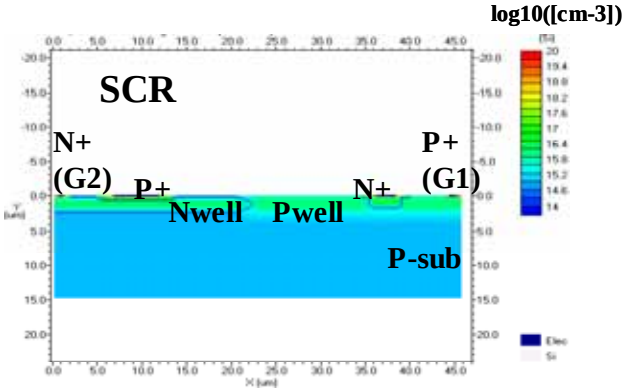


Fig.7 2D impurity profile of SCR.

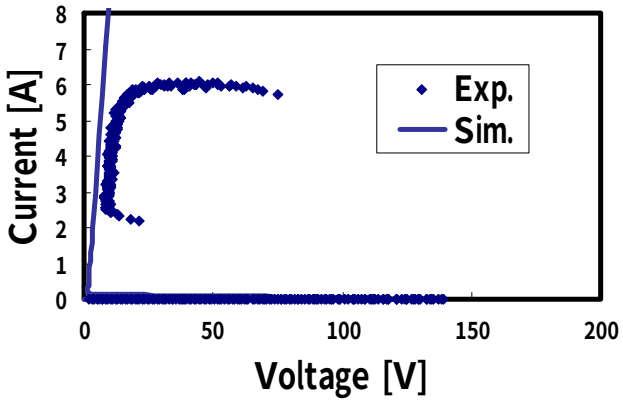


Fig.8 Comparison between TLP measurement and simulation in SCR.

III. Optimization of ESD Protection Network

In fig.1, it is required that ESD surge current flows into path B. Path B consists of the up-diode, the power bus line resistance (R_{line}), and the power clamp. Since the up-diode operates quickly at flat band voltage when ESD pulse is applied at plus, the performance of power clamp and R_{line} is a key in the ESD tolerance.

For 2D simulation, the effective channel width (W) in pMOS is smaller than actual one as shown in fig.4. This tendency is in agreement with reference [5]. In addition, although current in region A flows into lateral direction under channel region, that in region B flows into vertical direction under the drain based on bipolar operation. Therefore, the impurity profiles in deep region are important, and are extracted from SIMS (fig.6). These impurity profiles are also used for devices other than MOSFET.

SCR characteristics are important for optimization of V_{hold} and I_{t2} in power clamp, since ESD surge current flows in SCR after trigger current flows in pMOS as shown in fig.2. SCR structure is constructed from extracted depth impurity profile of fig.6 (fig.7), and the diffusion length of a transverse direction is extracted from comparison with TLP measurement (fig. 8).

Power clamp characteristics calculated using mixed-mode simulation after model parameter calibration of both trigger pMOS and SCR are in good agreement with experiments including W dependence (fig.9). Since simulation accuracy is ensured, we proceed to the investigation of the influence of R_{line} on ESD protection design.

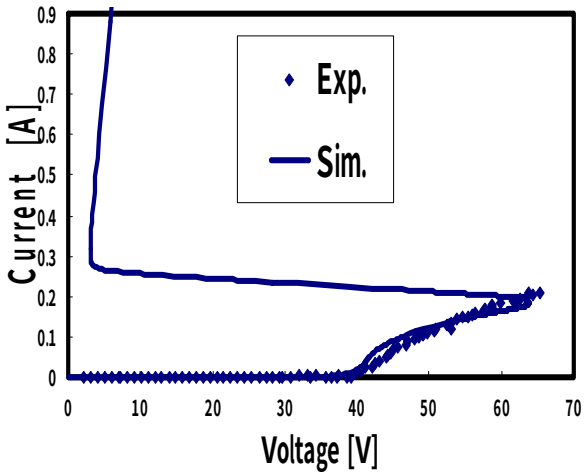
Dependence on snapback characteristics of R_{line} in the current path B in fig. 1 is shown in fig. 10. V_{t1} and R_{on} are large as R_{line} becomes large. When HBM pulses are applied, the current that flows into the internal and protection circuit is shown in figs.11 and 12, respectively. The current to internal circuit increases as R_{line} becomes large. The tendency becomes remarkable as HBM pulse increases (fig.13).

We predict that device is destructed when it reaches I_{t2} or critical power consumption. By setting up R_{line} small, ESD tolerance can be guaranteed to a higher HBM pulse. It implies that influence of power bus line resistance depending on the layout on ESD protection design cannot be ignored. ESD protection design is possible by optimizing ESD parameters for power clamp and R_{line}.

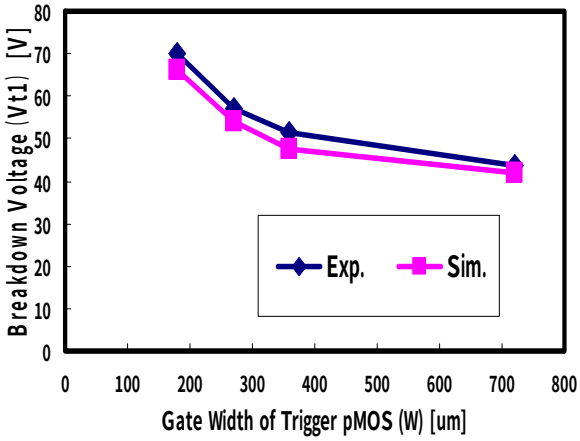
The ESD target (HBM2000V and MM200V) has been satisfied in actual circuit using our ESD protection design technique.

IV. Conclusions

We have proved usefulness of our approach by applying to optimize ESD protection circuit. As a result, it is found that the influence of power bus line resistance depending on layout on ESD protection design cannot be ignored. The mixed-mode simulation for the TLP data complement and physical analysis is indispensable to circuit network optimization of an ESD current path.



(a) Snapback characteristics



(b) Dependence on W of trigger pMOS for V_{t1}

Fig.9 Comparison between TLP measurement and simulation in power clamp.

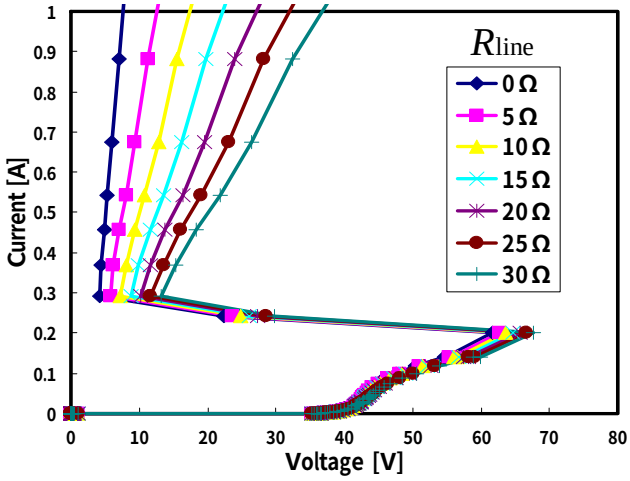


Fig.10 Dependence on snapback characteristics of R_{line} in the current path B in fig.1.

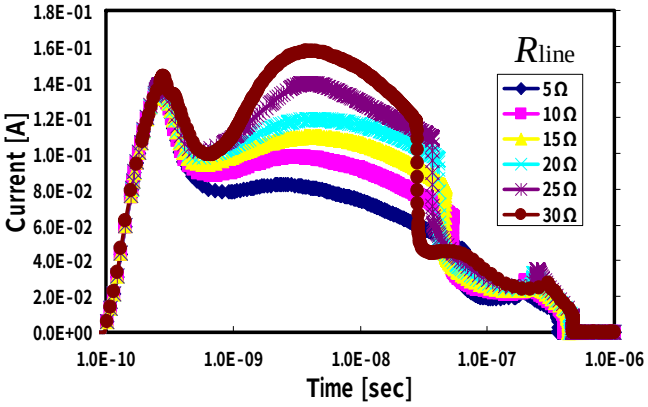


Fig.11 Current in path A for HBM+2000V.

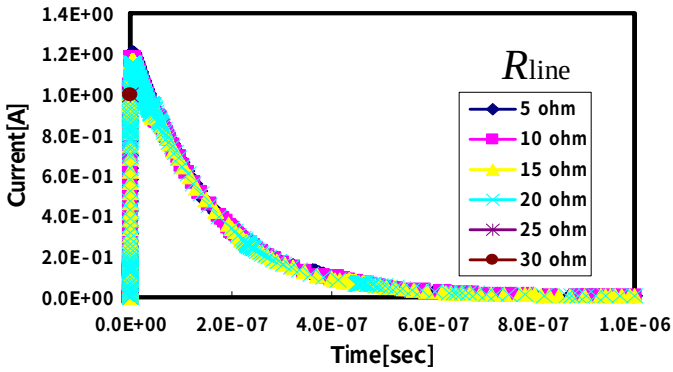


Fig.12 Current in path B for HBM+2000V.

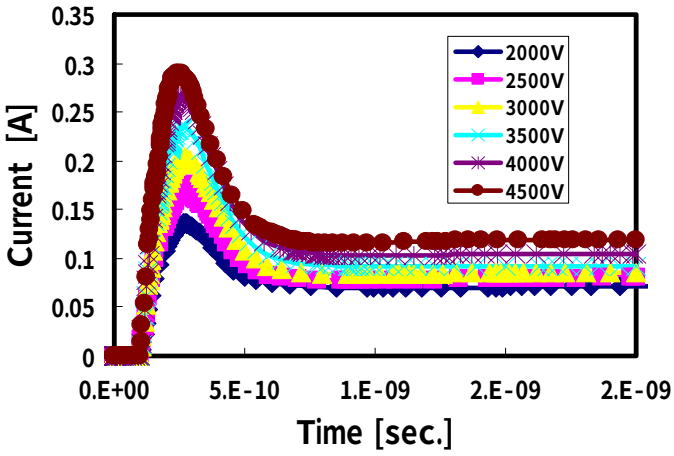


Fig.13 Current in path A (see, fig.1) with R_{line} of 5 ohm when HBM pulse increases.

References

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