An Accurate Separation of Floating-Body and Self-Heating Effects for High-Frequency Characterization of SOI MOSFET’s

Noriyuki Miura, Tadashi Chiba, and Shunsuke Baba
Semiconductor R&D Division, Oki Electric Industry Co., Ltd.
550-1 Higashi-asakawa, Hachioji, Tokyo, 193-8550, Japan
Email: miura288@oki.com

Abstract – In this paper, we present an accurate high-frequency characterization of AC output conductance method to separate SOI specific floating-body effects (FBE) and self-heating effects (SHE) from DC I-V data. In DC measurement, the transistor TEG pattern dependence is essential in view of the SOI body potential, which is confirmed by 3-dimensional device simulation. In AC measurement, the power of small-signal is the most critical issue for removing the FBE and SHE components.

I. INTRODUCTION

Silicon-on-insulator (SOI) has advantages over bulk device in simple isolation, low parasitic source/drain (S/D) capacitance, the elimination of latchup, and so on. However, the floating-body effects (FBE) and the self-heating effects (SHE) remain the critical issues for RF and/or analog applications. With the scaling towards gigahertz range, SHE is crucial even for low-power applications. Although the characterization of FBE and SHE have already reported [1][2][3][4], there are many difficulties for practical use of RF/analog design. Especially, we need careful characterization in view of physical phenomena of RF/analog transistor, which applies small-signal from gate electrode (Fig.1). In this paper, we present an accurate high-frequency characterization method to separate FBE and SHE from DC I-V data. In DC measurement, the transistor TEG pattern dependence is essential in view of the SOI body potential confirmed by 3D device simulation. In AC measurement, the power of AC-signal is critical for removing the FBE and SHE components.

II. TEG PATTERN DEPENDENCE OF DC CHARACTERISTICS

0.15um SOI MOSFETs are fabricated with the process in [5]. The commercially available UNIBOND® wafers have final silicon layer thickness (T_sil) of 40nm and buried oxide (T_box) of 200nm. In this work, we focus on the low standby-power NMOSFET (High-Vt option: Vt,saturation=0.4V). Fig.2 shows the I_DV_G and I_DV_D DC characteristics (body-floating TEG pattern), respectively. Moreover, the TEG pattern of SOI transistor is essential to FBE modeling, which treats the body current (I_B) of body-tied pattern and is extracted the body-source built-in potential lowering (ΔV_b) in BSIMSOI [3]. In practical RF/analog design, the model availability can be one of the key points in view of the pattern dependence. In order to compare with different TEG patterns (body-floating, body-tied with V_body=0V, and body-tied without biasing body-contact), the I_DV_G and I_DV_D characteristics are shown in Fig.3a and Fig.3b, respectively. Fig.4 shows the schematic of each pattern. As Fig.3a and Fig.3b shown, the drain current of body-floating pattern is higher than that of body-tied one due to higher body potential at SOI channel region. To certify the effect of the body potential, TCAD 3D device simulation results are shown in Fig.5, Fig.6 and Fig.7. Comparing between body-tied with V_body=0V and body-tied without biasing body-contact, the simulation results agree with experimental data. Thus the transistors for FBE characterization have to be the same pattern as practical high-frequency applications. The body-floating TEG is used as the device under study (DUT) for the following AC measurement.

III. CHARACTERIZATION OF AC OUTPUT CONDUCTANCE

In order to model MOSFET I-V behavior without FBE/SHE, we need to separate the effects of body-floating and lattice-heating from the MOSFET’s electrical behavior. Complex AC using LCR meter [1][2] and pulse [4] techniques have been proposed for obtaining FBE/SHE-free I-V data. However, transistor transconductance (g_m) and output resistance (R_out) are essential to RF/analog circuits design, it is important to characterize FBE/SHE under the gate bias modulation. And the LCR measurement at high frequencies (>5MHz) is not available because of equipment limitations. Fig.8 shows the measurement setup in this work. To measure the drain output conductance at higher frequencies (50-500MHz), PNA8364B Network Analyzer applies AC small-signal across the gate and drain terminals of the DUT. The DC biases of gate, drain, source and substrate are supplied by HP4156B Semiconductor Parameter Analyzer, which also simultaneously monitors the gate
and drain bias. Using extracted S-parameter, we have obtained I-V curves without FBE/SHE.

IV. AC POWER DEPENDENCE AND DISCUSSION

To characterize FBE/SHE in high-frequency region and understand the physical phenomena of SOI device, we certified the following dependences. (1) AC power (2) Gate length (3) AC frequency (4) Ambient temperature. The power dependence of AC-signal is most important for FBE characterization. Fig.10 shows the AC voltage amplitude versus AC power for 50ohm system. The large AC power case (0dBm) does not correspond to the drain current at low drain and low gate bias (Fig.9). The small AC power case (-20dBm) corresponds to DC measurement. Large-signal is not adequate to measurement for FBE characterization. It is necessary for accurate separation of FBE component to measure with low AC-power (Fig.11). It implies that the effective channel length modulation affects AC measurement due to non-quasi-static (NQS) behavior. Fig.12 and Fig.13 show the $I_DV_D$-$V_G$ characteristics of $L_{pol}=140\text{nm}$ and $L=0.5\text{um}$ transistor, respectively. As Fig.12 and Fig.13 shown, we successfully separate FBE and SHE components from DC I-V data. The AC frequency dependencies are not observed (Fig.14). It implies that removing FBE/SHE is enough in view of RF/analog transistor’s phenomena because the frequency is higher than the inverse of the time constants about lattice-heat (about 1usec [1]) and impact-ionization. The ambient temperature dependence of $I_DV_D$ is shown in Fig.15. Fig.16 shows the saturation current versus the ambient temperature comparing between DC and AC. As Fig.16 shown, we have to consider the difference of the temperature coefficients in device modeling.

V. CONCLUSION

An accurate high-frequency characterization method to separate SOI specific floating-body effects and self-heating effects from DC I-V has been presented. In DC measurement, the transistor TEG pattern dependence (floating-body and body-tied pattern) is essential in view of the SOI body potential confirmed by 3-dimensional device simulation. In AC measurement, the power of small-signal is the most critical issue due to the effective gate length modulation induced by the gate bias modulation.

REFERENCES

Fig. 3a: TEG pattern dependence of $I_DV_G$ characteristics (DC: $L=0.5\, \text{um}$, $W=5\, \text{um}$, $N_f=48$). The threshold voltage of body-tied ($V_{body}=0\, \text{V}$) is higher than that of body-floating or body-tied without biasing body-contact.

$V_D=0.05\, \text{V}$ (BT: Body no bias)
$V_D=1.0\, \text{V}$ (BT: Body floating)
$V_D=0.05\, \text{V}$ (Body-floating)
$V_D=1.0\, \text{V}$ (BT: Vbody=0V)

Drain Current [A] vs. Gate Bias [V]

Fig. 3b: TEG pattern dependence of $I_DV_D$ characteristics (DC: $L=0.5\, \text{um}$, $W=5\, \text{um}$, $N_f=48$). The drain current of body-tied ($V_{body}=0\, \text{V}$) is lower than that of body-tied without biasing body-contact due to having lower body potential at SOI region.

$V_D=0.05\, \text{V}$ (BT: Body no bias)
$V_D=1.0\, \text{V}$ (BT: Body floating)
$V_D=0.05\, \text{V}$ (Body-floating)
$V_D=1.0\, \text{V}$ (BT: Vbody=0V)

Drain Current [A] vs. Drain Bias [V]

Fig. 4: Schematic of body-tied and body-floating TEG pattern. The body-tied pattern is edgeless about channel width direction and is longer effective channel width ($W_{eff}$) than body-floating pattern.

Fig. 5: Simulated results of $I_DV_G$-$V_D$ characteristics comparing between body-tied with $V_{body}=0\, \text{V}$ and body-tied without biasing body-contact ($L=140\, \text{nm}$, $W=1\, \text{um}$: TCAD 3-D device simulation).

Fig. 6: TCAD simulated results of potential distribution ($V_D=1\, \text{V}$, $V_G=1\, \text{V}$) comparing between body-tied with $V_{body}=0\, \text{V}$ (left) and body-tied without biasing body-contact (right). Gate oxide and poly-silicon are set invisibly in the graphics.

Fig. 7: TCAD simulated results of potential ($V_D=1\, \text{V}$, $V_G=1\, \text{V}$) comparing between body-tied with $V_{body}=0\, \text{V}$ and body-tied without biasing body-contact.

Fig. 8: Measurement setup for high-frequency characterization.
**Fig. 9:** The $I_DV_D$ ($V_G=0.6V,0.8V,1.0V$) characteristics of $L=140nm$ Nfet comparing between AC ($f=100MHz$) conductance (red: power $-20dbm$, green:$-5dBm$, blue: $0dBm$) and DC (black). The power dependence is clearly observed.

**Fig. 10:** AC voltage amplitude v.s. power for 50ohm system.

**Fig. 11:** Drain current at $V_D=V_G=0.5V$ ($=Vt+0.1$) versus AC voltage amplitude. It is necessary for accurate separation of FBE component to measure with low AC-power.

**Fig. 12:** The $I_DV_D$ ($V_G=0.6V-1.0V$ step $0.1V$) characteristics of $L=140nm$ Nfet using AC (red: 100MHz/-20dBm) and DC (black). Self-heating effects (SHE) are successfully separated from FBE.

**Fig. 13:** The $I_DV_D$ ($V_G=0.6V-1.0V$ step $0.1V$) characteristics of $L=0.5um$ Nfet using AC (pink: 100MHz/-20dBm) and DC (black). Self-heating effects (SHE) are not observed because of having lower drain current.

**Fig. 14:** The frequency dependence of the $I_DV_D$ ($V_G=0.6V-1.0V$) characteristics ($L=140nm$,$AC:-20dBm$). The frequency dependences of both FBE and SHE are not observed because their time constants are larger than the inverse of the AC frequency.

**Fig. 15:** The ambient temperature dependence of the $I_DV_D-V_G$.  

**Fig. 16:** The $I_D$ versus the ambient temperature comparing between DC and AC ($100MHz$, -20dBm, $L=140nm$).