Implementation of ESD Protection in SOI Technology: A Simulation Study

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***Abstract* - Implementation of ESD protection circuits in SOI technology is well-known to be challenging due to inherent properties of SOI devices. While in comparison to bulk-Si SOI has excellent speed and power consumption features, its current handling capabilities are less impressive. This is due to thin-film current conduction properties and potential heat trapping in the thin film on top of a poor heat conductor (oxide). Design of ESD circuits in SOI is further complicated by the presence of the floating body effect, not adequately considered by conventional circuit simulators. In this work we present results of mixed-mode circuit-device simulation of ESD properties of SOI devices, including film thickness effects, heating during HBM and estimated failure current levels (It2).**

I. Snapback and Floating Body Effect

An SOI device structure, mesh and doping were generated using SEQUOIA Device Designer software [1]. Validation of simulator accuracy and calibration procedures to match simulation to experimental data have been documented previously for bulk MOS technology [3]. The device has a gate length 0.4mm, oxide thickness 150A and silicon film thickness 50nm (Fig. 1). A well-known characteristic of

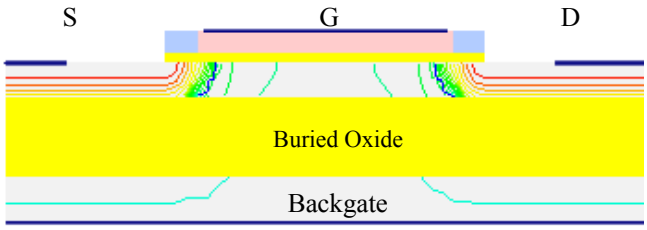

Fig. 1 SOI NFET structure used for this study. L=0.4μm, tox=150A, film thickness 50nm.

SOI devices is the floating body effect. This effect is caused by the lack of a substrate contact in an SOIFET, which can result in charge accumulation in the channel of the device (body) and a memory/hysteresis effect during transient operation. Since the body of an SOI device is floating, impact ionization which occurs in the device even well below junction breakdown voltage can cause charge accumulation in the device and thus encourage device snapback at a lower voltage.

Snapback simulation is carried out using the mixed-mode circuit shown in Fig. 2a. The circuit includes a 1kOhm series resistor at the drain to allow snapback to occur. A slow linear voltage ramp at the circuit node VIN at the rate 1e7V/s is used. Results are summarized in Fig. 3. At Vg=0V

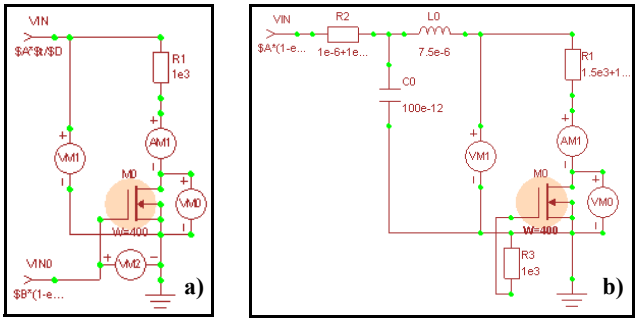

Fig. 2 Circuit for mixed-mode HBM simulation (a) and snapback simulations (b). In circuit a) resistors R1, R2 are time-dependent switches. Capacitor C0 is pre-charged to HBM voltage (2kV), then discharged into the SOIFET M0 through inductor L0 and resistor R1.

(diamonds, grounded gate configuration) this device has a triggering voltage (Vt1) or about 7.9V. With increasing gate biases (0.25V, 0.35V, 0.5V) a significant reduction in triggering voltage is observed as shown in Fig. 3, top. This sensitivity appears stronger than in a bulk-MOSFET due to the floating body effect and must be considered when gate-triggered ESD protection circuits are implemented.

However, an additional complication arises as a consequence of the limited response time of the floating body effect. The gate biase sensitivity of SOI triggering is therefore a strong function of stress speed. For fast pulses the floating body does not have sufficient time to respond. As a result, the ESD protection capability of an SOI protection device is a function of stress speed. This is shown in Fig. 3, center and bottom. For a slow stress ramp with a rise time of 0.1ms a gate potential of 0.5V results in a drastically lower triggering voltage of 2V as compared to 8V at Vg=0V. For faster stress ramps however, the triggering voltage increases. At stress rates typical for ESD events (10ns and faster) there is no appreciable reduction in Vt1 at a Vg=0.5V. We conclude therefore that for ESD protection

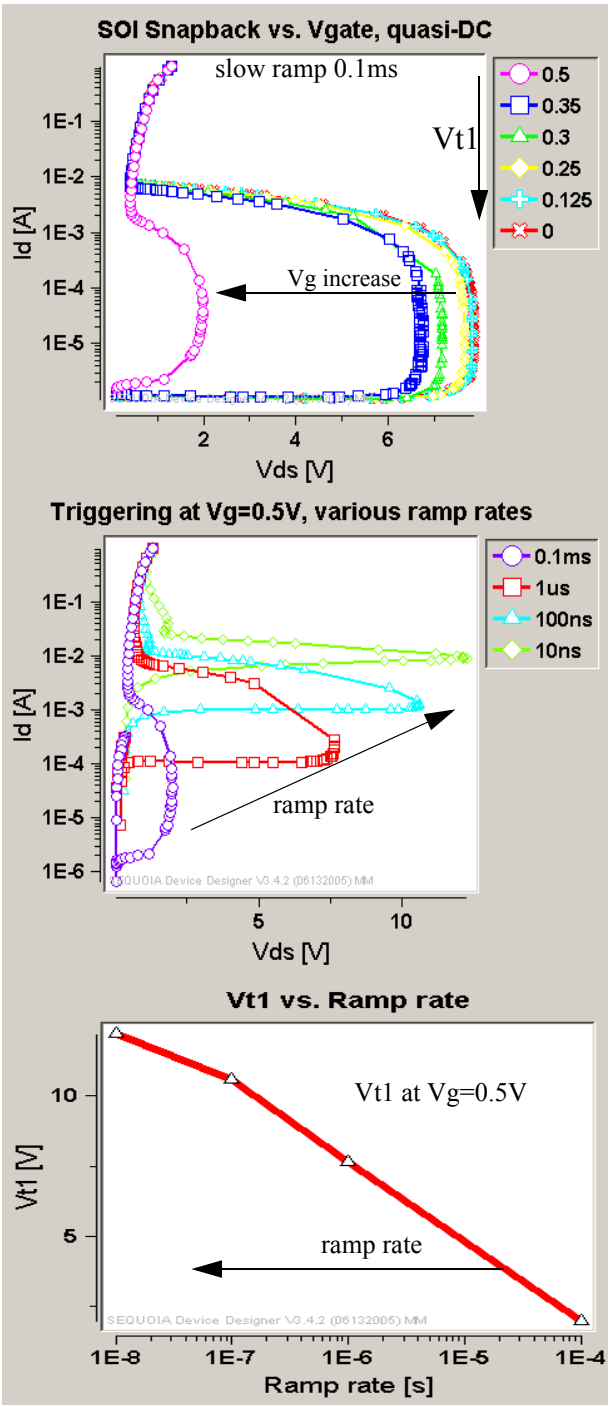

Fig. 3 SOI snapback simulation results for different gate biases. As Vg approaches threshold voltage, the floating body effect strongly reduces the triggering voltage Vt1 (top). This reduction of Vt1 is a strong function of ramp rate. At faster ramp rates, the floating body has no time to respond and triggering voltage Vt1 is higher (center and bottom).

purposes no enhancement of triggering due to floating body effect should be expected.

II. HBM ESD Discharge

Human body model simulation was carried out using the mixed-mode circuit shown in Fig. 2b. The circuit includes a pre-charged 100pF capacitor, time-dependent resistors as switches and a FEM model of the SOIFET. 2kV HBM simulation results are shown in Fig. 4. Three curves in Fig. 4 are

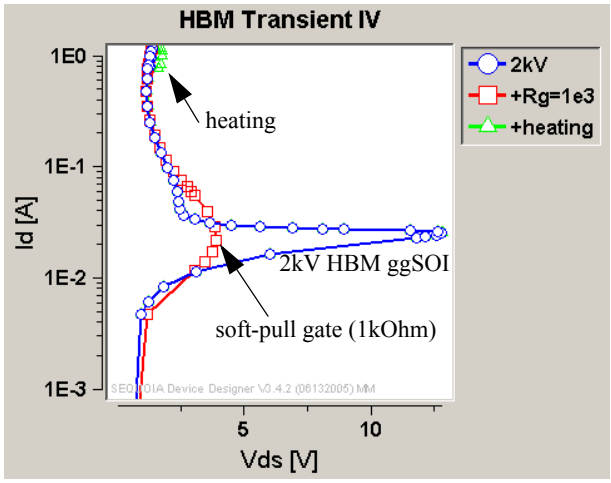

Fig. 4 2kV HBM current-voltage simulation results. The baseline simulation (grounded-gate SOI, circles) shows a transient triggering voltage of 12.8V, significantly higher than DC Vt1 of 8V (Fig. 1). A soft-pull gate ground resistor of 1kOhm allows the gate to float up during the discharge and enhances snapback (squares). Heating effects are not significant at this device width W=400µm (triangles).

for the baseline simulation (circles), soft-pull gate (squares) and self-heating (triangles). In comparison to DC IV for the grounded-gate configuration (Fig. 3, diamonds), it is noticeable that the HBM simulation shows triggering at a much higher voltage 12.8V instead of 7.9V. This is due to transient charge build-up effects described elsewhere [2], i.e. voltage overshoot observed during fast rise-time events such as HBM with an initial voltage rise time of >200V/ns. The HBM simulation result is also consistent with faster ramp rate triggering simulations shown in Fig. 3, bottom. Higher triggering voltages can be expected in SOI devices during fast stress events because the floating body cannot respond quickly enough to enhance current flow.

As was observed in the previous Section, SOI snapback may be quite sensitive to gate bias depending on bias level and stress speed. In our HBM simulation we observe a dramatically decreased Vt1 for a 1kOhm soft-pull gate configuration during HBM (squares in Fig. 4). This reduction in Vt1 is caused by a strong rise in Vg during the HBM pulse to a peak value of about 1V due to low gate capacitance in our thick oxide SOI device.

III. Self-Heating during HBM and Failure Current Estimates (It2)

Low thermal conductivity of oxide can create heat dissipation problems in SOI technologies. Due to high current densities associated with ESD events, local overheating is a potentially serious problem. We consider self-heating in simulation by including a self-consistent solution of the heat transfer equation along with Poisson's and current continuity equations. Also of crucial importance are appropriate boundary conditions. In this work we use finite thermal resistance heat sinks at the backgate (bulk heat sink) as well as source and drain electrodes (heat evacuation through metallization). Temperature distributions are shown in Fig. 5 for t=2ns and t=100ns. Early after the ESD pulse starts all temperature increase is still near the drain junction where it was generated, peak temperature is low. On the other hand,

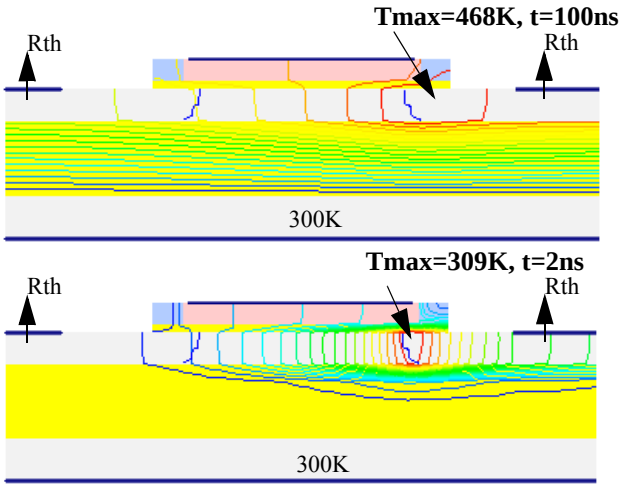

Fig. 5 Internal temperature distribution in the SOI device 2ns (bottom) and 100ns (top) after the beginning of the ESD pulse. Heat sinks with finite thermal resistances are specified at the bottom of the structure (Rth=1K/Wμm) as well as the source and drain electrodes (Rth=100K/Wμm).

100ns after pulse start there is substantial heating and heat diffusion towards the heat sinks. The effects of self-heating on the IV curve are moderate in this case of device width W=400μm.

Fig. 6, Fig. 7 show heating effects in the SOI device during 2kV HBM for a set of device widths. While device temperature peaks at 470K for W=400μm, higher values are reached with decreasing device width and increasing current density. Since aluminum fails at around 700K, we can derive estimates for device failure from this peak temperature. As a result, we obtain an estimated failure current density of about It2=1.3A/300μm=4.3mA/μm for this SOI

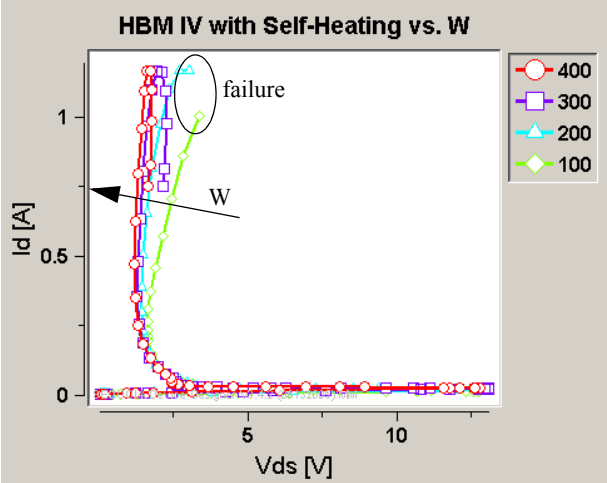

Fig. 6 Self-heating effect versus SOI device width W during 2kV HBM.

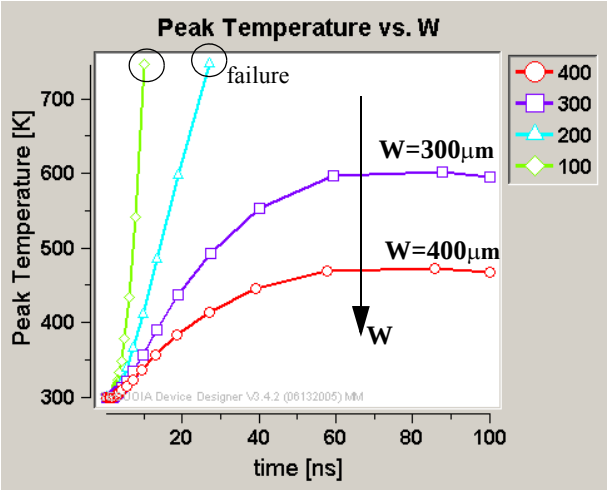

Fig. 7 SOI heating during 2kV HBM versus device width. Thermal boundary conditions as in Fig. 5 are used. Peak current handling capabillity of about 4.3mA/μm is predicted.

technology (film thickness 50nm as shown in Fig. 1). This is a reasonably good value compared to around 10mA/μm for typical bulk MOS performance. Of course, this is an upper bound for It2, since in reality other effects such as current non-uniformity, contact failure, etc. can occur at lower current levels.

Since heat evacuation through the buried oxide is poor, cooling of the device through source/drain metallization may be significant. As an experiment, we repeat the above 2kV HBM simulation summarized in Fig. 6, Fig. 7, this time with near-ideal metallization cooling. A comparison shows potentially achievable improvement in current handling

capability of the SOI device. Results are summarized in Fig. 8. An improvement of current handling capability of almost 100% is observed. The resulting second breakdown level of about 8mA/µm is close to what might be expected for a bulk MOS technology. In reality this level of cooling via metallization will be difficult to achieve and It2 values closer to Fig. 7 should be expected (4.3mA/µm).

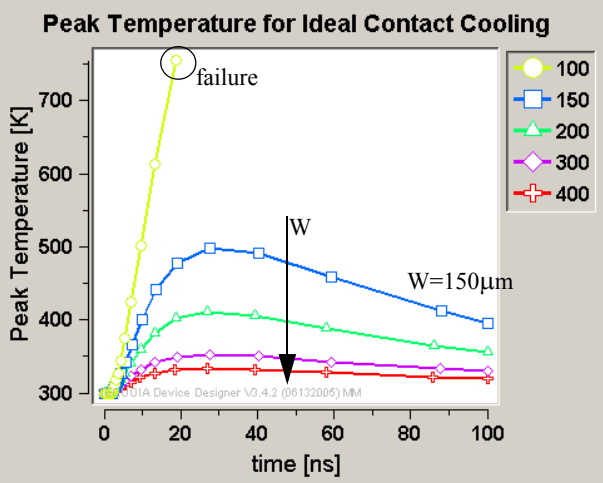

Fig. 8 Self-heating effect versus SOI device width W during 2kV HBM. Near-ideal cooling via source/drain metallization is assumed with Rth=1K/Wµm. In this case W=150µm still passes without permanent thermal damage. Therefore, a peak current handling capabillity of about 8mA/µm is predicted.

V. Conclusions

A general simulation methodology for the analysis of SOI devices under ESD conditions has been described and simulation results demonstrated. Important aspects of SOI device behavior such as floating body effect and self-heating are captured by transient mixed-mode simulation and their practical implications for ESD circuit design are discussed. Significant importance of transient effects on electrical and thermal behavior of SOI devices under ESD stress is shown. Thermal simulations are used to derive an upper bound for the second breakdown failure current It2.

References

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