Simulation Study of Reduced Self-Heating in Novel Thin-SOI Vertical Bipolar Transistors

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***Abstract* — Simulations have been performed to study the self-heating in thin-SOI, vertical bipolar transistors for the first time. Two new device structures are proposed and the simulations show that they can improve the heat dissipation significantly. By adding a heat sink connecting the collector and the substrate and/or having a thin localized BOX underneath the SOI collector, self-heating can be reduced substantially without increasing device area or degrading device performance.**

I. Introduction

SOI BiCMOS has recently gained attention as a preferred technology for RF and mixed-signal applications. It has been shown that it has better noise isolation and reduced capacitance [1-2]. In order to facilitate the integration with high-speed, thin-SOI CMOS, a SiGe-base, vertical bipolar transistor with no sub-collector and no deep-trench isolation has been proposed and demonstrated [3-4]. The device has a fully or partially depleted SOI layer as the collector and has decent device performance, especially when the substrate is biased such that an accumulation layer is formed in the collector. However, due to poor heat conductivity in the buried oxide and surrounding shallow trench isolation, self-heating can be a major concern in such thin-SOI devices. Excessive heating can be detrimental to device performance/reliability and sometimes cause permanent damage such as thermal runaway. Even though self-heating has been studied for bulk and SOI bipolar transistors, the SOI thickness was on the order of microns and the devices were still "bulk-like" [5]. They had a thick sub-collector and deep trench. In this paper, we studied the heat dissipation in thin-SOI vertical bipolar devices for the first time, and proposed a simple yet elegant solution to fix the heat problem without increasing device area or degrading device performance.

II. Device Structures and Simulation Methods

A cross-sectional schematic of a vertical npn SOI BJT is shown in Fig.1. The device is symmetric and only half of the device is shown. In order to reduce the self-heating, a heat sink can be added at no cost of device area by connecting the n+ reach-though region in the SOI collector directly to the substrate by metal or poly as depicted in Fig. 2. Another approach for improving heat dissipation is to reduce the BOX thickness. This also allows low substrate bias operations to form the accumulation layer in the collector and further enhance device performance. We have developed a process to form a localized thin BOX (<10nm) and a back electrode underneath the collector on a typical SOI wafer. Fig. 3 shows the cross-sectional scanning electron microscopy (SEM) picture. The excess poly is then planarized and removed by CMP.

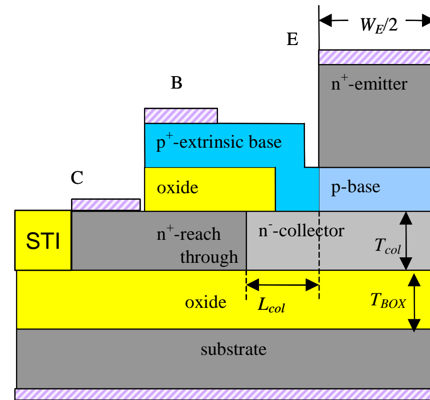

Fig. 1: Cross-sectional schematic of a vertical npn BJT on thin SOI substrate.

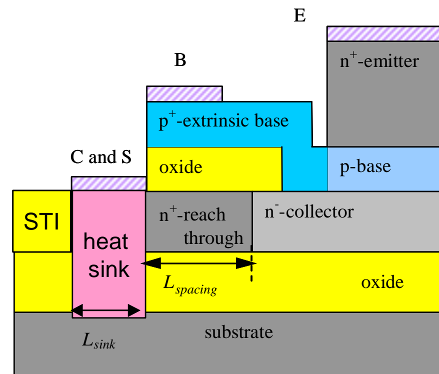

Fig. 2: Cross-sectional schematic of a vertical npn BJT on thin SOI substrate with a heat drain at the collector contact.

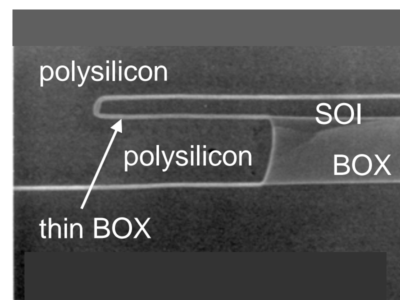

Fig. 3: Cross-sectional SEM picture of the formation of a localized thin BOX and a back electrode by a process of etch, oxidation and poly fill. The excess poly can be planarized and removed by CMP.

Two-dimensional (2D) device simulations were conducted in MEDICI [6]. The initial lattice temperature was 300 K and the thermal simulations were performed with a standard finite element method (FEM) [7]. An isothermal boundary condition was defined at the bottom of the substrate. The heat conductivities of silicon, polysilicon and tungsten were 1.2, 0.7 W/cm/K and 1.78 W/cm/K (bulk values), while they are expected to decrease as dimension scales [8]. Therefore, the actual temperature rise in the SOI BJTs can be slightly larger than our calculations. The simulated device has a single-finger, n^{++} poly emitter with width (W_E) of 100 nm, a uniform base doping profile (N_B) of 2e18 cm^{-3} and a collector doping concentration (Nc) of 1e17 cm^{-3}. The base width is 80 nm. The SOI thickness (T_{SOI}) is 100 nm and the BOX thickness (T_{BOX}) is 200 nm for the SOI devices. The spacing between the emitter and the n^{++} extrinsic collector or reach-through region (L_{col}) is 100 nm. The length of the reach-through region which is also the spacing between the heat sink and the n- collector ($L_{spacing}$) is 350 nm and the size of the heat sink (L_{sink}) is 90 nm. The Ge content is zero in the Si-base devices and linearly graded from 0 to 20% in the SiGe-base BJTs. The heat conductivity of Si was used for the SiGe-base, which makes little difference in the heat dissipation in the device.

III. Simulation Results

Fig. 4(a)-(c) show the 2D contour of power density for a SiGe-base SOI device, a Si-base SOI device and a SiGe-base bulk BJT, respectively, at a collector bias (V_{CE}) of 3 V and base bias (V_{BE}) of 0.88V. Most of the heat is generated in the SOI collector region with a hotspot at the corner of the n- collector next to the reach-through region and the BOX. This is due to the current crowding which is typical in SOI BJTs. Meanwhile, the hotspot in the bulk device is at the collector-base junction. Fig. 5 shows the vertical 1D cut of the power density across the CB junction at the center of the device. The power density in the SiGe-base SOI device is about 2.5x higher than that of the Si-base SOI device.

Fig. 6(a)-(c) show the 2D contours of the device temperature rise (ΔT) from the thermal simulations, for a SOI device, a bulk device and a SOI device width the heat sink, respectively. The power density in the device was fixed to be 1 mW/μm (device width) in all thermal simulations. This value is similar to that in the SiGe-base device. The self-heating in the SOI device is quite severe and the temperature increase (ΔT) is as high as 221 °C compared to only 15 °C in the bulk device. This is because most of the temperature drop is across the BOX layer which has a heat conductivity two orders of magnitude less than that of Si. With the heat sink, ΔT can be reduced to 55 °C in the SOI device even with the thick BOX.

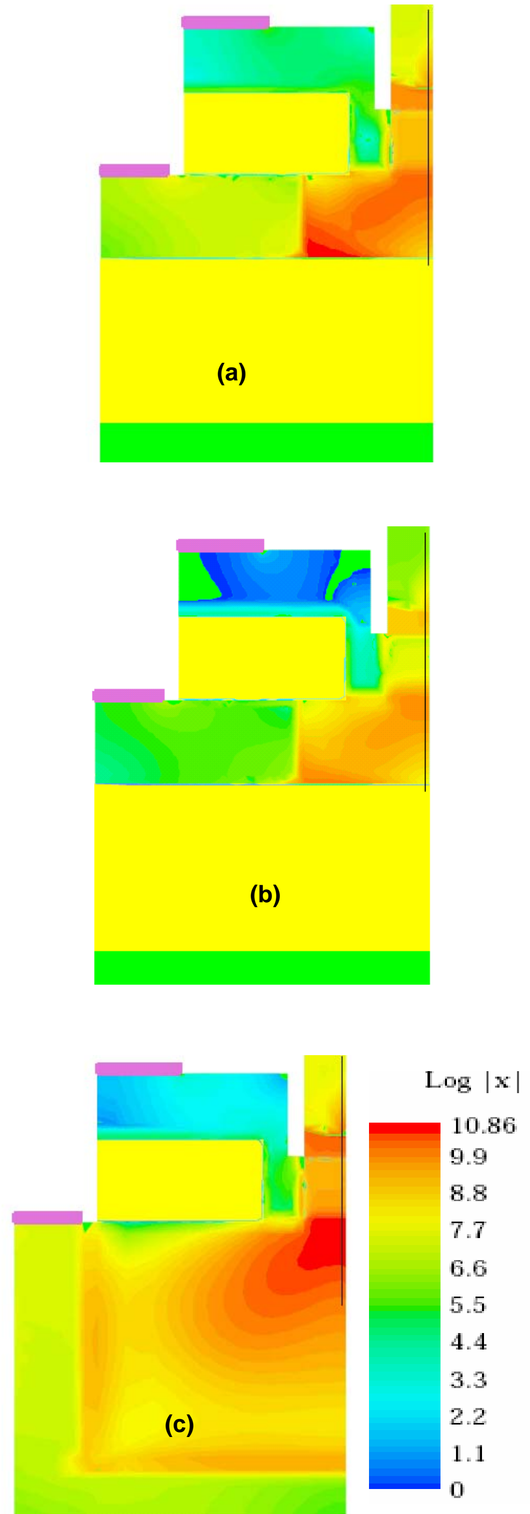

Fig. 4: 2D contours of power density for a (a) SiGe-base SOI device; (b) Si-base SOI device; and (c) SiGe-base bulk device. The unit is W/cm3.

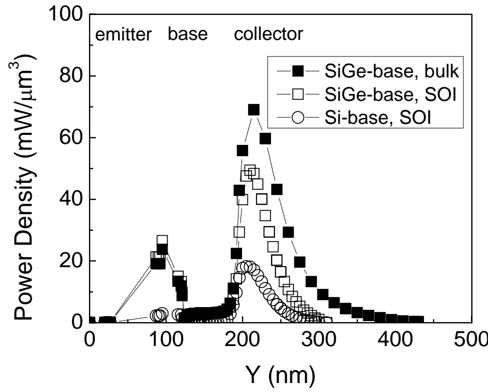

Fig. 5: 1D cut of power density at the device center for the same devices in Fig. 4.

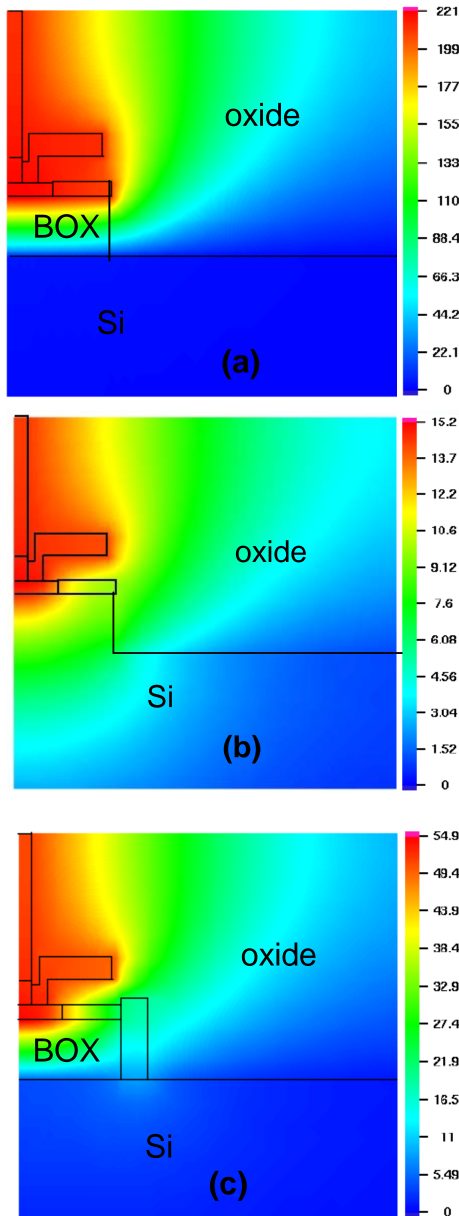

Fig. 6: 2D contours of temperature rise in a (a) SOI device without a heat sink; (b) bulk device; and (c) SOI device with a tungsten heat sink. The unit is °C.

A sensitivity analysis and device design has also been performed. Fig. 7 shows peak ΔT versus L_{sink} at a fixed $L_{spacing}$. At L_{sink} = 90 nm (contact size of the state-of-art technology), ΔT is reduced significantly by 70-75%. ΔT starts to flatten out as L_{sink} is increased, which means most of benefit can be achieved by a relatively small heat sink, which can be the size of the collector contact. Fig. 8 shows peak ΔT versus $L_{spacing}$ at a fixed L_{sink}. At a small $L_{spacing}$, it is almost a linear dependence with a steeper slope (meaning more sensitive) for tungsten than poly. At a large $L_{spacing}$, the dependency gets weakened. Fig. 9 shows the peak ΔT versus device width (W) at L_{sink} = 90 nm and $L_{spacing}$= 350 nm. Without the heat sink, ΔT rises rapidly at a small W, and starts to saturate at a large W. This is because the characteristics of heat dissipation change from 3D to 2D as device width increases, which results in a higher thermal resistance. On the other hand, with the heat sink, ΔT is much lower and not sensitive to device width. This indicates that the heat sink is very effective and can be used in large-width device for high current applications.

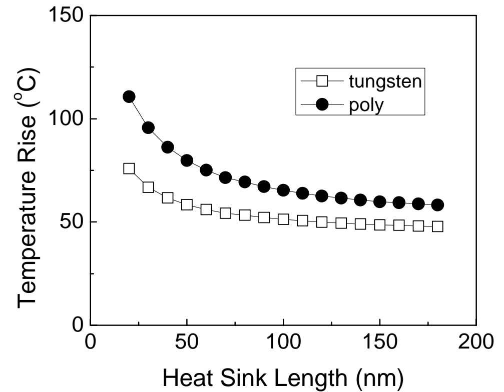

Fig. 7: Temperature rise vs. heat sink length with $L_{spacing}$ = 350 nm for devices with W = 1 μm and T_{BOX} = 200 nm.

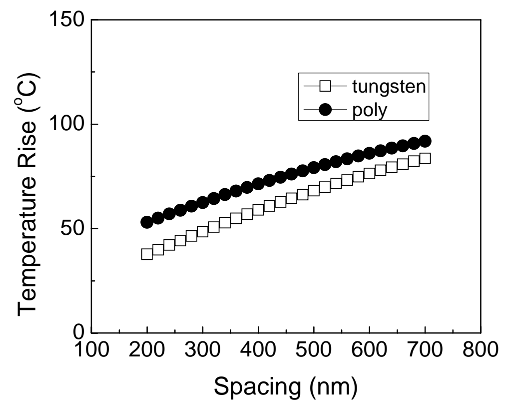

Fig. 8: Temperature rise vs. spacing between the heat sink and the n-collector for L_{sink} = 90 nm. W = 1 μm and T_{BOX} = 200 nm.

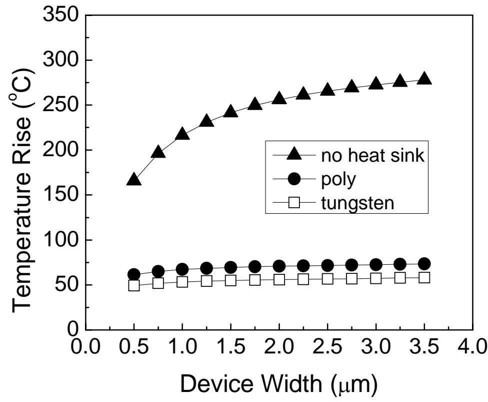

Fig. 9: Temperature rise vs. device width for $L_{spacing}$ = 350 nm, L_{sink} = 90 nm and T_{BOX} = 200 nm.

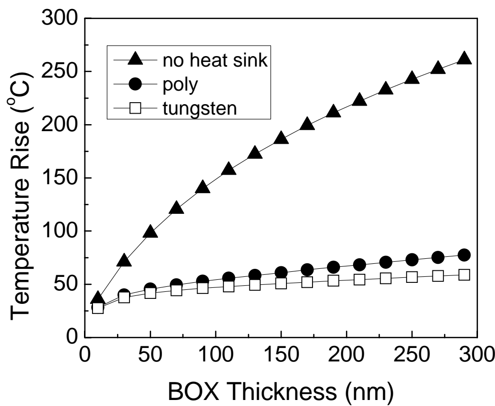

Fig. 10: Temperature rise vs. BOX thickness for devices width $L_{spacing}$ = 350 nm, L_{sink} = 90 nm and device width of 1 μm.

Fig. 10 shows the peak ΔT versus BOX thickness (T_{BOX}) at L_{sink} = 90 nm, $L_{spacing}$= 350 nm and W = 1μm. ΔT is reduced from 261 °C to 35 °C as T_{BOX} is reduced from 300 nm to 10 nm in the device even without the heat sink. The effect of reducing T_{BOX} to 10 nm is almost equivalent to using a heat sink of 30 nm at $L_{spacing}$= 350 nm. With the heat sink, ΔT is insensitive to T_{BOX}, again demonstrating the effectiveness of the heat sink.

IV. Conclusions

Device and thermal simulations have been performed to study the heat dissipation in thin-SOI, vertical bipolar transistors. Two novel device structures are proposed. By adding a heat sink connecting the collector and the substrate and/or having a thin localized BOX underneath the SOI collector, the heat dissipation is significantly improved without increasing device area or degrading device performance. The CMOS-compatible process facilitates direct integration with current high-performance SOI CMOS technology.

Acknowledgement

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