Device Behavior Modeling for Carbon Nanotube Silicon-On-Insulator MOSFETs

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***Abstract* – We offer a methodology for the numerical analysis of carbon nanotube (CNT) embedded silicon-on-insulator (SOI) MOSFETs. We examine CNT-SOI-MOSFETs that have a planar sheet of single-walled zig-zag semiconducting CNTs embedded along the channel direction, as shown in Fig. 1. To obtain device performance details including current-voltage characteristics, we employ a quantum based device solver [1] along with a Monte Carlo simulator [2]. Our calculated results show that replacing the silicon with CNTs in the channel may significantly improve device performance. The CNT-SOI-MOSFET with the smallest diameter tube may surpass other configurations of CNT-SOI-MOSFETs and conventional SOI-MOSFET in performance if fabricated successfully with the same channel thickness. In addition, under certain conditions the CNT-SOI-MOSFETs show negative differential resistance.**

I. INTRODUCTION

Carbon nanotubes (CNTs) are among the candidates for use in future electronic devices due to their advantageous structural and electrical properties [1-6]. These properties include very high low-field mobilities, diameter and chirality dependent bandgap variations, and structural robustness in nanoscale dimensions. To understand the CNT properties and how they can affect device performance, we first need to examine their physical structure. Basically, CNTs are nanoscale hollow tubes rolled up from planar graphite sheets (graphene). Single-walled CNTs can range in diameter from a few to a hundred or so angstroms. In addition to its diameter, chirality or wrapping angle of the tube is needed to uniquely determine its electrical properties. Equivalently, a CNT can also be defined by its fundamental indices (l,m), which are the integer coefficients of the unit lattice vectors of the hexagonal graphite that specify the CNT vector around the circumference. Depending on the fundamental indices, CNTs can be metallic (l-m is a multiple of three) or semiconducting (otherwise).

In this paper, we investigate the effects of semiconducting single-walled zig-zag CNTs on electron transport in the channel of an SOI-MOSFET. For a zig-zag CNT, the fundamental index m is always equal to zero. It is semiconducting if l is not a multiple of three. It has a diameter that is linearly proportional to l with a proportionality constant approximately equal to 0.8Å. Additionally, the bandgap of semiconducting single-walled zig-zag carbon nanotubes (CNTs) are inversely proportional to l.

Here, we first discuss the energy band diagram of CNTs. We then show how we integrate the details of CNT energy dispersion curves into our device solver. We next discuss our methodology and show our calculated current-voltage characteristics.

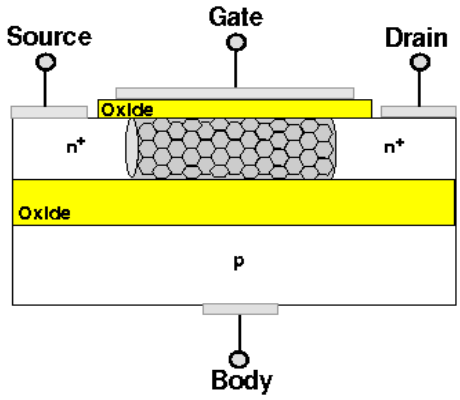

Figure 1: Simulated design of CNT-SOI-MOSFET.

II. CARBON NANOTUBE DEVICE MODEL

To account for the CNT related quantum effects, we need to determine the band-structure of the CNTs. Due to confinement introduced around the circumference when graphene is wrapped into a CNT, the bandstructure splits into a system of subbands. Each of the subbands has a characteristic effective mass, mobility and band energy minima. We determine the energy levels of CNTs by applying zone-folding methods to graphene. The following formula gives the energy dispersion for a zig-zag CNT, which has fundamental tube indices (l,0) as a function of electron momentum along the tube, k_x, and subband index, β, (a (=2.46Å) is the lattice constant of two dimensional graphite.) [5]:

$$E = \pm 3\sqrt{1 + 4\cos\left(\frac{\sqrt{3}}{2}ak_x\right)\cos\left(\frac{\pi\beta}{l}\right) + 4\cos^2\left(\frac{\pi\beta}{l}\right)} \quad \text{(eV)} \qquad (1)$$

To extract the pertinent information that can be easily integrated into our device simulator, we approximate Eqn. (1) by a quadratic energy dispersion relation. Conduction band minimum, effective mass and non-parabolicity factor for the quadratic energy dispersion relation can be calculated using Eqn. (1) for different subbands β. For a zig-zag CNT, the total number of subbands are $2l$. In accordance with this, we set the prime values of β to integers from $-l$ to l excluding one of the boundaries. For each subband, conduction band minimum and effective mass can be found by setting k_x to zero and finding the curvature around k_x=0, respectively:

$$E_\beta^l = \left(3\left|1 + 2\cos\left(\frac{\pi\beta}{l}\right)\right|\right) \quad \text{(eV)} \qquad (2)$$

$$\frac{m_\beta^{*l}}{m_o} \cong 0.0910\frac{\left(E_\beta^l \big/ 1\text{eV}\right)}{\left|\cos\left(\frac{\pi\beta}{l}\right)\right|} \qquad (3)$$

Specifically, we include the statistics of the lowest six CNT subbands that all the electron transport takes place in our simulations. Among these six subbands, pairs of two subbands have the same energy dispersion curves because $-\beta$ and β give the same cosine value. We list in Table 1 the energy band minima and the effective masses of the lowest three subbands for l=10 and l=22 tubes.

We then employ an MC simulator [2] to obtain velocity versus electric field curves. Using these curves, we derive a diameter and field dependent mobility model [1]. Our MC calculations indicate that the low field electron mobility of l=10 tube is as much as five times higher than that of silicon. The low field electron mobility of l=22 tube is even higher; it is approaching ten times that of silicon.

We next obtain momentum relaxation length versus field curves of the CNTs. Our calculations show that these curves and velocity versus field curves show similar characteristics. Momentum relaxation length versus electric field curves first increase with applied field, reach a peak and then roll off [6]. The peak values of l=10 and l=22 tubes are approximately 40nm and 100nm, respectively. To avoid ballistic transport we here simulate sufficiently long CNTs. Therefore we ensure being in the scattering limited solution domain.

After we obtain CNT characteristics, we import them into our device simulator. We treat the CNT in the device as a material with different bandstructure, intrinsic carrier concentration, electron affinity, electron mobility, etc.

Table 1: CNT Parameters.

	m^*/m_o	$E_{\min}$ (eV)	$\pm\beta$
l=10			
	0.082	0.53	7
	0.339	1.15	6
	0.208	1.85	8
l=22			
	0.040	0.24	15
	0.112	0.51	14
	0.129	0.93	16

III. QUANTUM CNT-SOI-MOSFET MODEL

We develop a two-dimensional quantum SOI-MOSFET simulator by modifying our quantum bulk device solver [1]. Our simulator is capable of obtaining coupled solution of Poisson equation along with quantum semiconductor CNT/Si electron and hole current continuity equations. We list these equations in the order mentioned at the bottom of this page in Table 2.

Table 2: Quantum CNT/Si Semiconductor Equations

$$\nabla^2\phi = -\frac{q}{\varepsilon}\left(p_{QM} - n_{QM} + D\right) \qquad (4)$$

$$\frac{\partial n_{QM}}{\partial t} = \nabla.\left(-n_{QM}\mu_n\nabla\left(\phi + \frac{1}{q}\left(\chi - \chi^{Si}\right) + \frac{kT}{q}\ln\left(\frac{n_o}{n_o^{Si}}\right) + \phi_{QM}\right) + \mu_n\frac{kT}{q}\nabla n_{QM}\right) + GR_n \qquad (5)$$

$$\frac{\partial p_{QM}}{\partial t} = \nabla.\left(p_{QM}\mu_p\nabla\left(\phi + \frac{1}{q}\left(\chi + E_G - \chi^{Si} - E_G^{Si}\right) - \frac{kT}{q}\ln\left(\frac{n_o}{n_o^{Si}}\right) - \phi_{QM}\right) + \mu_p\frac{kT}{q}\nabla p_{QM}\right) + GR_p \qquad (6)$$

Poisson equation (4) solves for the electrostatic potential, ϕ, in conjunction with quantum CNT/Si electron, n_{QM}, hole, p_{QM}, and net dopant, D, concentrations. In addition, we introduce CNT-Si electron-hole mobilities, $\mu_{n\text{-}p}$, intrinsic carrier concentration, n_o, electron-hole Shockley-Hall-Read net generation-recombination rates, $GR_{n\text{-}p}$, electron affinity, χ, bandgap, E_G, and temperature, T, along with familiar constants.

To obtain CNT-SOI-MOSFET performance details, we first solve Eqns. (4)-(6) (we solve only Eqn. (4) within the oxide) ignoring quantum effects. This gives a modified version of Eqns. (4)-(6), which can be obtained by setting ϕ_{QM} to zero in the CNT/Si electron (5) and hole (6) current continuity equations, and replacing the subscript *QM* for quantum by *CL* for classical. Solving for the classical set of equations, we resolve CNT-Si heterostructure effects including intrinsic variations of CNT/Si bandgaps and workfunctions.

We then include quantum effects to resolve carrier confinement between the gate and buried oxides. Additionally, potential wells at CNT-Si band discontinuities can significantly affect carrier transport phenomena due to confinement and band-to-band tunneling. To resolve quantum effects, we employ the density gradient theory [1, 7]. According to the theory, quantum effects can be included in the solution by an effective potential term in addition to electrostatic potential, as follows:

$$\phi_{QM} = \frac{\hbar^2}{6q\sqrt{n_{CL}}}\left[\frac{1}{m_{\parallel}}\frac{\partial^2\sqrt{n_{CL}}}{\partial x^2}+\frac{1}{m_{\perp}}\frac{\partial^2\sqrt{n_{CL}}}{\partial y^2}\right] \qquad (7)$$

We next use a combination of numerical methods to solve Eqns. (4)-(6) to obtain CNT-SOI-MOSFET device performance including current-voltage characteristics and carrier concentrations.

IV. SIMULATION RESULTS

We simulated a 0.15μm SOI-MOSFET with a roughly 0.1μm thick buried oxide. We first investigate the effects of a single planar layer of CNT sheet embedded under the gate to fully fill the channel between the two oxide layers, as shown in Fig. 1. In this case, device performance is affected by different size channel cavities in the normal direction in addition to different CNTs in the channel with varying electrical parameters. To equate the effects of channel cavity thickness on electron transport, we next embed planar sheets of different diameter CNTs into a channel with a fixed channel thickness. We decide on the channel thickness such that one layer of biggest diameter tube can fit. Therefore, we obtain comparative analyses of the electrical parameters of different size tubes on electron transport.

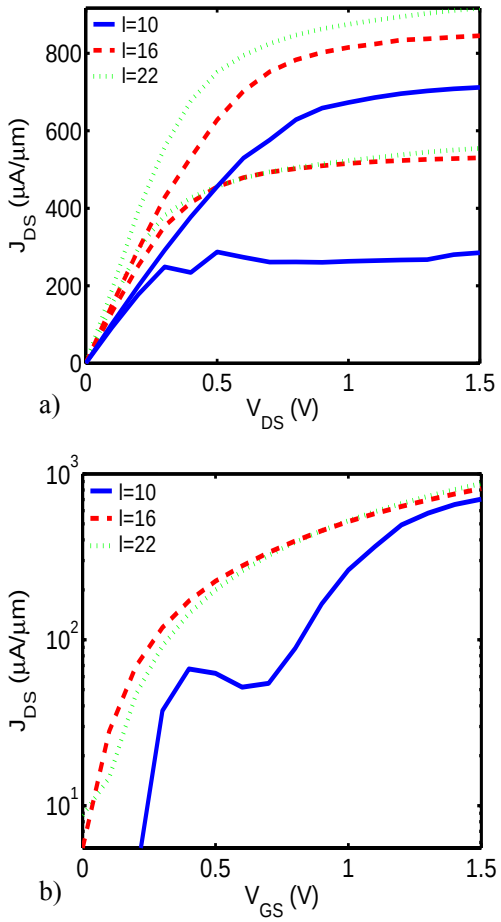

Figure 2: a) Current-voltage (V_{GS}=1.0, 1.5V) and b) subthreshold (V_{DS}=1.0V) characteristics for CNT-SOI-MOSFETs with channel thicknesses equal to the diameter of the tube embedded. (Nanometer scale diameters of *l*= 10, 16 and 22 tubes are 0.8, 1.28 and 1.76, respectively.)

In Fig. 2(a) and 2(b), we show our calculated device performance for the current-voltage and subthreshold characteristics of CNT-SOI-MOSFETs employing various size CNTs. Each CNT-SOI-MOSFET has an associated channel thickness equal to the diameter of the tube used. Among those CNT-SOI-MOSFETs, the one that embodies the biggest diameter CNT (d=1.76nm, CNT fundamental index *l*=22) outperforms other configurations by supplying more drive currents in the linear and saturation regions for two different gate biases (V_{GS}=1.0, 1.5V). It also has good subthreshold characteristics. We attribute the best device performance of *l*=22 tube embedded CT-SOI-MOSFET to higher low-field mobilities associated with bigger diameter tubes. (Low-field electron mobility of *l*=22 CNT is about twice as large as that of

the *l*=10 CNT.) In addition, the lowest diameter CNT (d=0.8nm, *l*=10), when embedded in SOI-MOSFET, shows negative differential resistance (NDR). We relate this to high mobilities, band discontinuities between the CNT and Si, and the smallest cavity formed between the buried oxides.

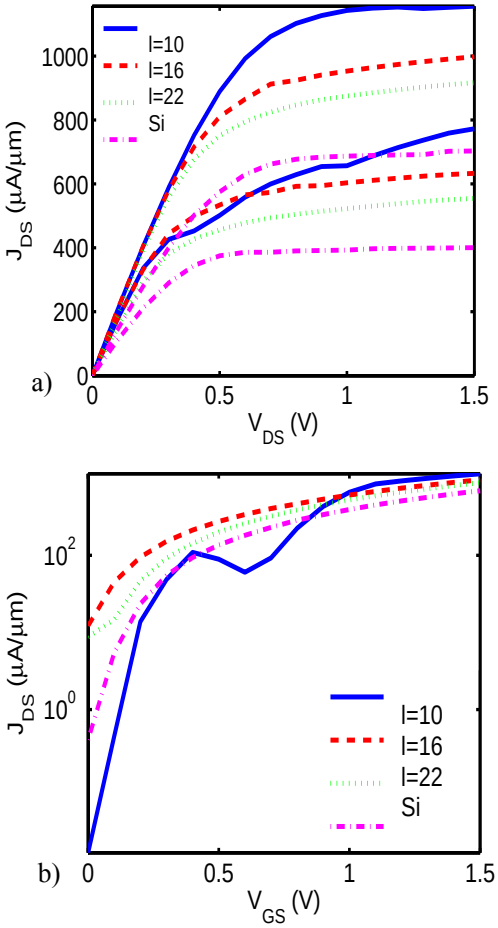

Figure 3: a) Current-voltage (V_{GS}=1.0, 1.5V) and b) subthreshold (V_{DS}=1.0V) characteristics for CNT-SOI-MOSFETs with channel thicknesses equal to 1.76nm, which is the diameter of the biggest tube. (Nanometer scale diameters of *l*= 10, 16 and 22 tubes are 0.8, 1.28 and 1.76, respectively.)

We then investigate the effects of CNTs on device performance for the same film dimensions, thereby eliminating channel film thickness as a variable on device performance. Thus we set the film thickness equal to the diameter of the biggest CNT, therefore the devices with the largest tubes only have one layer, whereas the *l*=10 and *l*=16 devices have film thickness composed of multiple CNT layers. We also simulate one conventional SOI-MOSFET with a silicon film in the channel. In Fig. 3(a), our calculated current-voltage curves show that smaller the CNT diameter, the higher the supplied current, with the conventional Si-SOI-MOSFET outperformed by others. We attribute the difference between the SOI-MOSFETs having the Si channel or the CNTs in the channel to higher mobilities associated with CNTs, and band discontinuities between the CNT and Si. Additionally, we relate the difference in the performance of SOI-MOSFETs employing CNTs mainly to the amplitude of the band discontinuities between the utilized CNT and the heavily doped Si terminals.

In Fig. 3(b), our calculated subthreshold curves for the devices in 3(a) indicate that the CNT-SOI-MOSFET with the lowest diameter tube outperforms other SOI-MOSFETs. As in 2(b), it also shows NDR. This is related to low band discontinuity between the *l*=10 tube and Si, and high electron mobility on *l*=10 tube.

V. CONCLUSION

We have developed a device simulator for modeling CNT-SOI MOSFETs. We find that among devices that have constant film thickness small diameter-CNT device yields higher transconductance. On the other hand, devices with one layer of CNTs and film thickness equal to the CNT diameter show larger diameter-CNT devices have higher transconductance.

VI. REFERENCES

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