Investigation of 6T SOI SRAM Cell Stability Including Quantum and Gate Direct Tunneling Effects by Three-dimensional Device Simulation

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Abstract - **This paper shows the impacts of the tunneling leakage current and quantum effect on Static Noise Margin (SNM) and soft error phenomenon for 6T type SOI SRAM by direct 3D process and devise simulations. Below 1.0 nm gate oxide thickness, the influence on SRAM SNM cannot be negligible. Soft error calculations for SOI SRAM cell show SOI devices are very strong for α-particle injections, but for heavy-ion injections, soft error might occur easily and both quantum and tunneling leakage current effects should be considered for accurate future scaled SRAM cell simulation.**

I. INTRODUCTION

As CMOS technology is dramatically scaled down in recent years, the operation of SRAM becomes critical issue for further scaling. Keeping enough SNM and avoiding α-particle and neutron-induced soft errors are the two key factors in reliability. In this paper, we focused on SOI devices because of its capability for scaling. The mechanism of soft error in SOI devices is different from bulk type. In bulk type, α-particles and heavy-ions from neutron-induced nuclear reaction hit the drain diffusion region and the induced charges are collected by funneling and diffusion effects. However, in SOI devices, the parasitic bipolar current causes the soft error [1] when α-particles and heavy-ions hit the channel region. SOI devices are considered to be very strong against soft error [2].

In this paper, 6T type SOI SRAM cell structure was simulated directly by 3D device simulator. SNM including quantum and tunneling leakage current effects were evaluated. Next, investigating the possibilities of the α-particle and heavy-ion induced soft errors, the impacts of the SOI film thickness and the tunneling leakage current effect are also evaluated. Finally, we will show the perspective for scaling in the future.

II. SIMULATION METHOD

Fig.1 shows 6T type SOI SRAM cell simulation structure. It was constructed with the combination of ISE 3D process emulator and 3D device simulator. We also constructed the via and wire structure.

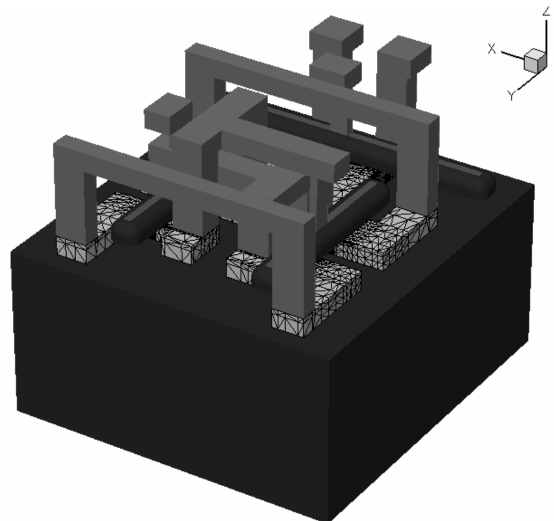

Figure 1: Simulated 6T SOI SRAM structure. This structure is constructed by ISE 3D process emulator and simulated by 3D devise simulator.

SRAM characteristic was calculated directly from Poisson equation and electron and hole continuity equations (not Mixed-mode). By this method, real circuit structure can be calculated directly and it proves very powerful tool for future perspectives. The gate length was assumed at 40 nm and I_{off} of NMOS and PMOS devices were adjusted. The gate material is polysilicon and aluminum wire is used.

The SRAM cell circuit is described in Fig.2. For example, Fig. 3 shows the potential distribution in write-state. And SRAM SNM is calculated by butterfly curves.

For soft error simulation, α-particle energy was assumed to be 5 MeV, and it was injected vertically into center of the

channel of high voltage node NMOS device (in Fig.2).

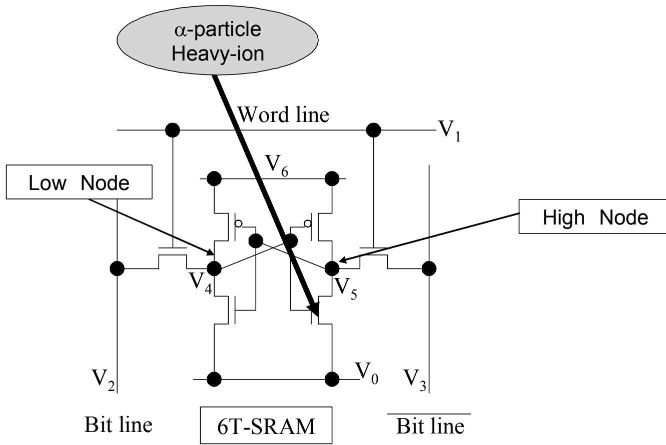

Figure 2: Simulated 6T SOI SRAM circuit. α-particle and heavy ion are injected vertically into the center of high voltage NMOS node.

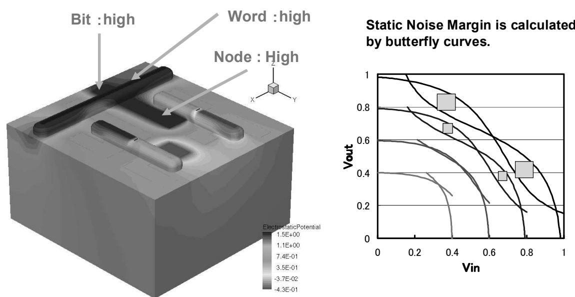

Figure 3: Calculated structure for SRAM Static Noise Margin. Potential distribution in write-state is shown.

For heavy-ion injection, Carbon and Magnesium ions are injected, and injection energy was also 5 MeV. Linear Energy Transfer (LET) values were calculated by modified Stopping Code [3]. In both calculations, impact ionization was included.

III. RESULTS AND DISCUSSIONS

Fig.4 shows the dependence of the SNM on the thickness of the gate oxide film.

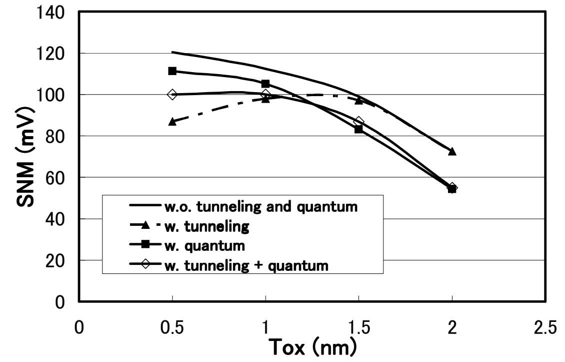

Figure 4: SNM characteristics as a function of gate oxide thickness.

We also calculated the influences of the gate direct tunneling current, quantum effect and both combination. With over 1.5 nm gate oxide film thickness, gate direct tunneling leakage effect was negligible. Increase of equivalent oxide thickness due to quantum effect loses gate controllability. This leads to decrease of SNM by 20 mV. When oxide thickness becomes below 1.0 nm, SNM becomes decreasing because the gate leakage current increases dramatically. In this region, with quantum effect, gate direct tunneling current decreases because of the increase of the equivalent oxide thickness. So, SNM including both gate direct tunneling current and quantum effect becomes larger than that including only gate direct tunneling current.

To understand the influence of the gate direct tunneling effect in detail, the gate oxide thickness dependencies of ΔSNM (SNM_wo_tunneling - SNM_w_tunneling) and the gate direct leakage current are shown in Fig.5.

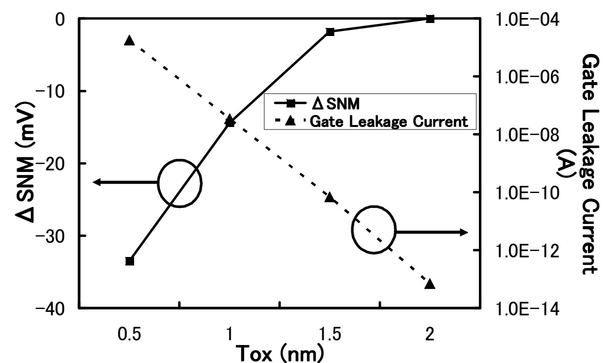

Figure 5: The gate oxide thickness dependence of ΔSNM and the gate direct leakage current.

The Gate leakage current increases exponentially as gate oxide thickness decreases. This causes heavy decrease of SNM.

Next, we analyzed the transient behaviors of 6T SOI SRAM cell when α-particles and heavy–ions were injected. Fig.6 shows the transient response of high node voltage for α-particle injection.

We changed the SOI film thickness from 10 nm to 100 nm, but the bit error didn't occur for all thicknesses. So, it was concluded SOI device is very strong for α-particle injection.

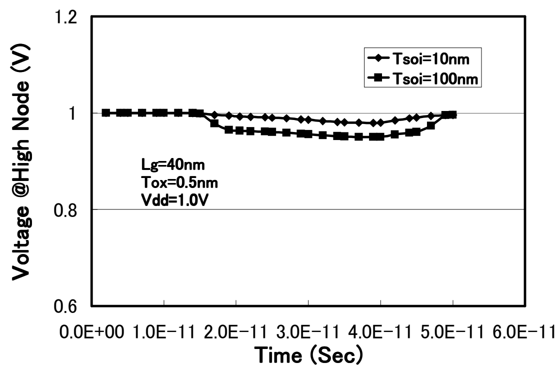

Figure 6: The transient response characteristics of α-particle injection.

Fig.7 shows the result for heavy-ion particle injection. Compared with α-particle injection, the voltage drop by secondary charges induced by heavy-ion particles becomes influential.

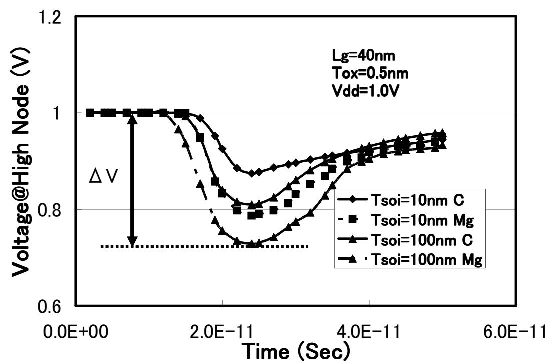

Figure 7: The transient response characteristics of heavy-ion particle injection

This is because total induced charges by heavy-ion injection are much larger than those by α-particle injection. But, the bit error doesn't occur even for heavy-ion particles. Further, the thinner the SOI channel layer thickness becomes, the less the bit errors occur. These results indicate thin SOI structure is very strong against secondary charge disturbances.

Then, we show the perspectives for future scaling in SOI devices. Fig.8 shows the influence of the gate direct tunneling leakage current effect for heavy-ion injection.

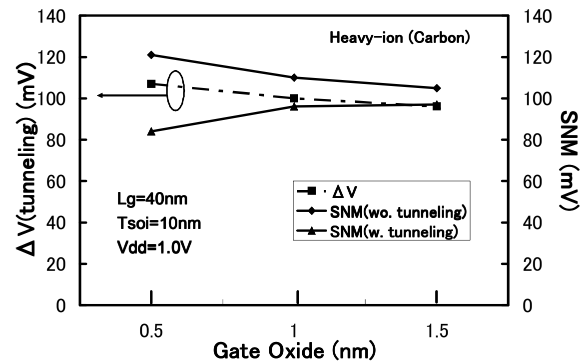

Figure 8: The influence of the gate direct tunneling effect for heavy-ion injection. Only ΔV calculation accounts for heavy-ion injection.

For 1.5 nm gate oxide thickness, the voltage drop by heavy-ion is comparable with SNMs of both with tunneling and without tunneling. But below 1.0 nm thickness, the voltage drop becomes larger than SNM of tunneling model. So, in the oxide thickness scaled regime, soft error becomes easy to occur. Tunneling effect has strong influence on soft error behavior in the future.

Finally, we show the supply voltage dependence. We changed the voltage from 1.0 to 0.4 V. As shown in Fig.9, the voltage drop decreases as the supply voltage decreases.

It is because by decreasing the electrical field, it becomes difficult for impact ionization to occur, so the bipolar current is reduced. On the other hand, SNM decrease dramatically as the supply voltage decreases.

As a result, it becomes serious problem for soft error to occur easily in the future scaling SRAM cell

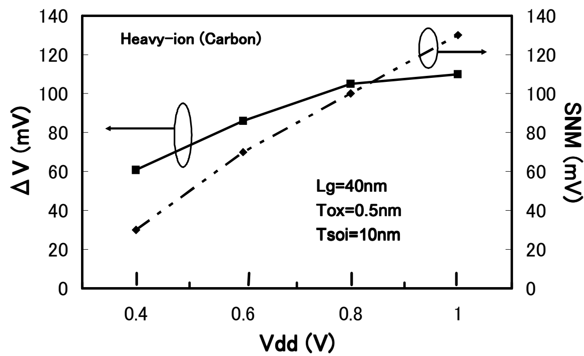

Figure 9: The dependence of the supply voltage. We changed the value from 0.4 to 1.0 V. Only ΔV calculation accounts for heavy-ion injection.

IV. CONCLUSION

For 6T type SOI SRAM, impacts of the tunneling leakage current and quantum effect on SNM and soft error phenomenon were investigated by direct 3D process and devise simulations. Below 1.0 nm gate oxide thickness, because the tunneling current becomes remarkable, its influence on SRAM SNM cannot be negligible. Soft error calculations for SOI SRAM cell show SOI devices are very strong for α-particle injections, but for heavy-ion injection, soft error might occur easily and both quantum and tunneling leakage current effects should be considered for accurate future scaled SRAM cell simulation.

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