Gate Tunneling Current Fluctuations associated with Random Dopant Effects

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***Abstract*— Random-dopant-induced gate tunneling current fluctuations are studied for the first time. It is shown that gate leakage currents considerably fluctuate among MOSFETs even if there is no gate oxide thickness fluctuation. The physical origin of random-dopant-induced gate tunneling current fluctuations near the stand-by ($V_g \approx$ +0 V) is the fluctuations in source-to-channel p-n junction location rather than the fluctuations in normal oxide field. Statistical variations of p-n junction location due to random impurities are essential for ultra-small MOSFETs and should be appropriately taken into account in the device simulation.**

I. Introduction

It is already well recognized that threshold voltages V_{th} fluctuate among sub-micron MOSFETs as the discreteness of impurities becomes actualized [1], [2], [3]. However, effects of random dopant fluctuation (RDF) on device characteristics other than V_{th} are rarely studied. Recently, we have shown that Schottky contact resistance variations due to RDF lead to an additional unreliability in future MOSFETs, by clarifying that an impurity sited near the Schottky barrier makes the tunneling potential steep and the current density concentrated in Schottky barrier diodes [4]. From a viewpoint that RDF modulates the tunneling barrier, gate tunneling currents, in this case the oxide barrier corresponds to the Schottky barrier, may also fluctuate among transistors. In this study, we show, for the first time, that RDF brings about gate tunneling current fluctuations considerably even if there is no oxide thickness fluctuation.

II. Simulation method

A. Gate Tunneling Current

Simulations are carried out using in-house 3D Drift-Diffusion device simulator DIAMOND implemented with the WKB approximation for the direct tunneling currents. Figure 1 schematically shows the components of gate tunneling currents taken into account for this study. [1] These components are calculated and then added to the recombination-generation term in the current continuous equation at the gate/oxide and the oxide/substrate interface, that is, detail carrier transport in the oxide is not considered. As Fig. 1 indicates, I_{gcv} and I_{gvc} are appeared if $|V_g - V_{fb}|$ exceeds the energy gap of Si, therefore in the simulated V_g bias ranges (-0.4 V$\leq V_g \leq$ 1.0 V), I_{gcc} is the dominant.

[1] In addition, we have developed to handle impactionization-generated hole currents by the tunneling electrons for the sake of simulating gate oxide reliability due to the anode hole injection [5].

Although the amounts of tunneling flux depend on both the energy level of carriers and their spatial distributions, our simulator does not involve any quantum confinement effect. With this and due to the lack of rigorous justification of the WKB assumption on ultra-thin gate oxides, we restrict our discussion to the qualitative argument.

B. Random Dopant Effect

Only the long-range parts of coulomb potential of impurities are incorporated in the Poisson solver so as to avoid unphysical capture of majority carriers around impurity atom [6]. The number of impurities included in each control volume is determined from the Poisson distribution with respect to macroscopic impurity concentration at that volume and the position of impurities in the volume is determined from uniform random numbers. RDFs in all semiconductor domains are taken into consideration and thus a robust 3D Drift-Diffusion simulator is developed to handle intrinsic gate tunneling current fluctuations associated with random dopant effects.

All simulation samples are n-type MOSFETs with using p-Si substrate and n-doped single crystal silicon gate of $L = W = 20$ nm (Fig. 2). Throughout the simulation, pure SiO_2 is assumed to be the gate oxide material. In order to consider statistical variations of p-n junction location more realistically, X_{js} of source/drain extension and deep source/drain, which are usually assumed to be extremely shallow in previous studies, say 7 nm [3], are set as 15 and 30 nm, respectively in our simulation. Statistical analyses are performed over 50 up to 100 simulation samples.

III. Results and discussion

Figure 3 shows the calculated $J_g - V_g$ characteristics of 100 n-MOSFET samples with t_{ox} = 1.4 nm. Figure 4 is the corresponding $I_d - V_g$ characteristics. Notice that throughout this study, physical gate oxide thickness fluctuations are not included. The histograms of J_g at V_g = 0.05 V, 0.4 V and 1.0 V are shown in Figs. 5(a), (b) and (c), respectively. The gate tunneling current density fluctuates significantly under low gate bias $|V_g| \approx 0$ V conditions, which clearly shows that RDF mainly affects the electrostatic potential at the depletion condition and its power of influence is gradually screened by carriers as V_g increases [7]. The J_g distributions at V_g = 0.4 V and 1.0 V, which are above threshold, are well characterized by the Gaussian distribution, whereas the distribution near standby exponentially deviates.

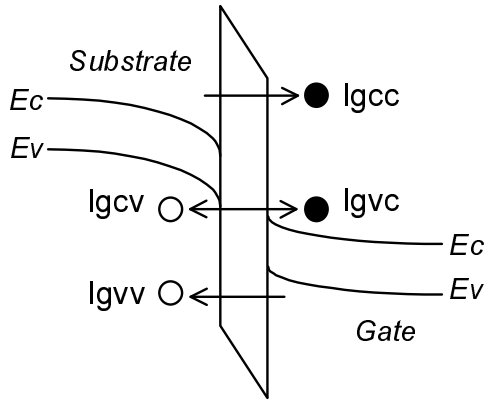

Fig. 1. Schematic drawing of band diagram and the components of gate tunneling currents taken into account during this study; electron currents from the conduction band of one side to the conduction band of the other side (I_{gcc}), electron currents from the valence band of one side to the conduction band of the other side (I_{gvc}), hole currents from the conduction band of one side to the valence band of the other side (I_{gcv}), hole currents from the valence band of one side to the valence band of the other side (I_{gvv}). In the simulated V_g bias ranges, I_{gcc} is the dominant.

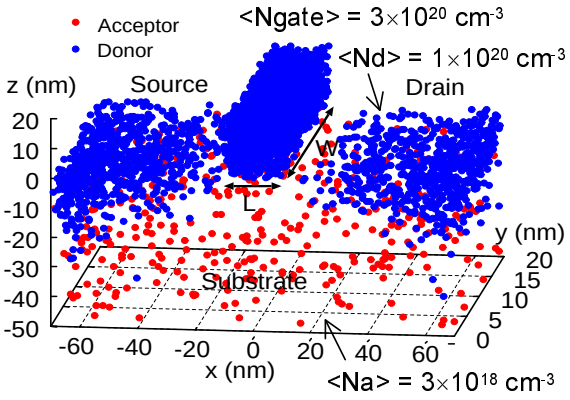

Fig. 2. Bird's eye view of a simulated n-MOSFET structure with $L = W =$ 20 nm. Random dopant fluctuations (RDF) of all semiconductor domains are taken into consideration. Pure SiO_2 is assumed to be the gate oxide material.

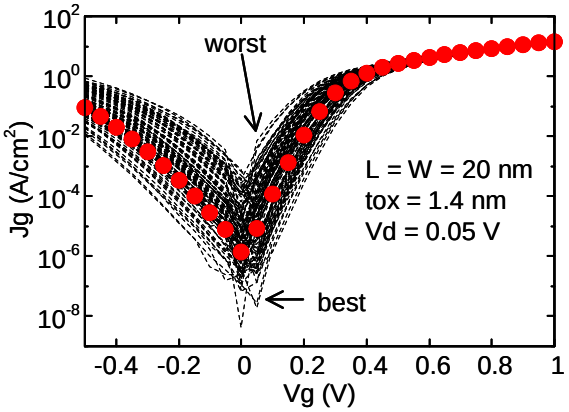

Fig. 3. Simulated $J_g - V_g$ curves of n-MOSFETs. Solid circles and broken lines represent a sample without RDF and samples with RDF, respectively.

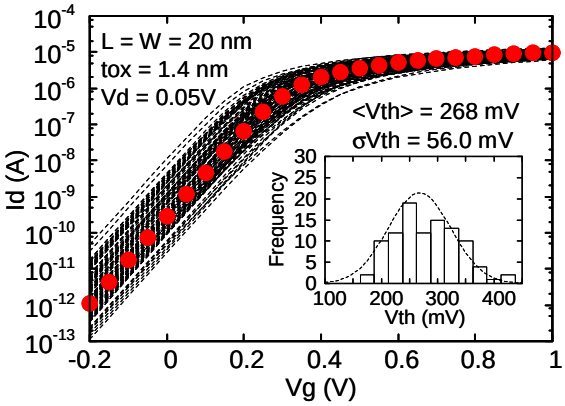

Fig. 4. $I_d - V_g$ characteristics corresponding to Fig. 3. The inset is the histogram of V_{th} extracted by the maximum Gm method. During the course of this study, V_{th} is defined as the gate voltage at which Gm reaches its maximum.

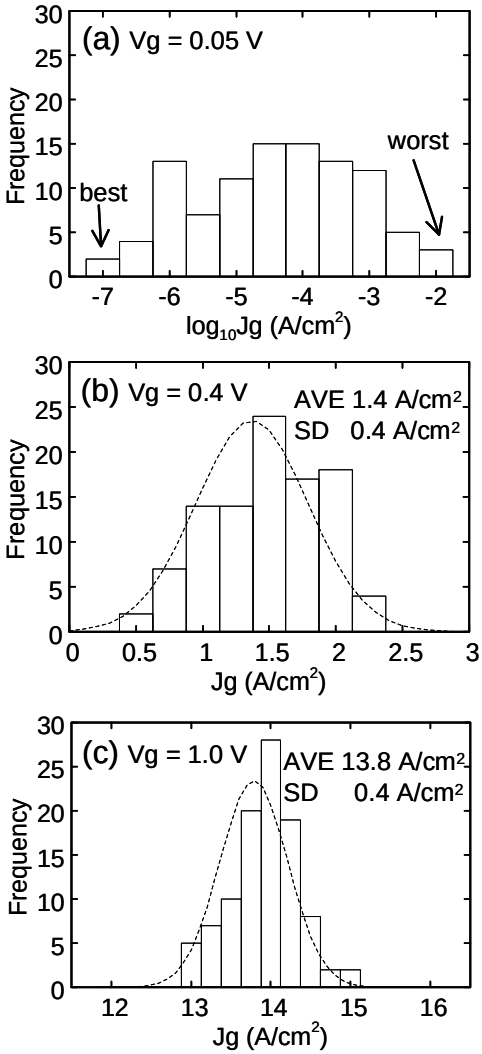

Fig. 5. The histograms of J_g at V_d = 0.05 V are plotted for V_g = 0.05V, 0.4 V and 1.0 V. Note that the horizontal axis in (a) is not linear, since the range of variation is so wide. In contrast, the J_g distributions above threshold $\langle V_{th} \rangle$ = 268 mV are well characterized by the Gaussian distribution.

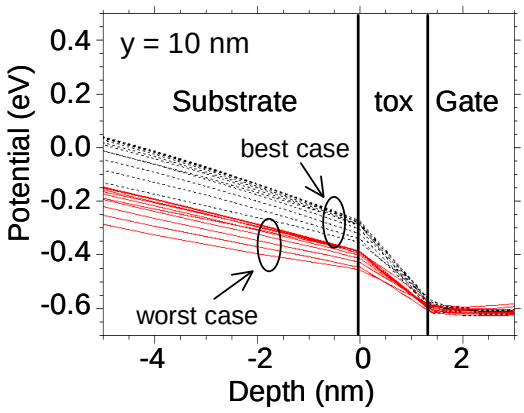

Fig. 6. Simulated vertical potential profile under the gate electrode along the depth direction at $V_g = V_d = 0.05$ V for the best/worst cases in Fig. 3. The effect of RDF on modulating the gate oxide field is not so clear.

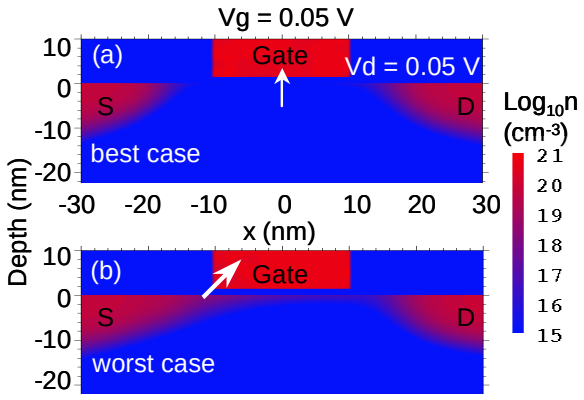

Fig. 7. Contour plots of electron concentration across the center plane ($y = 10$ nm) for the best(a)/worst(b) cases. The typical velocity vector of gate tunneling electrons in each case is indicated by arrows.

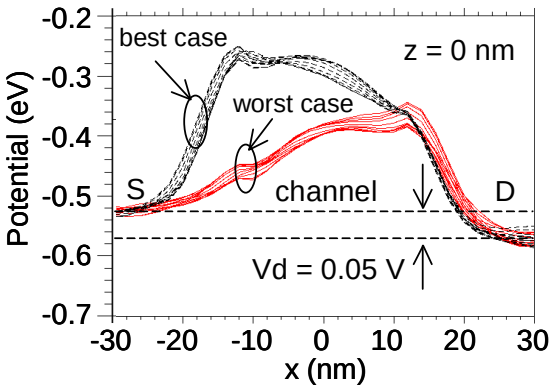

Fig. 8. Simulated surface potential along the channel length for the best(a)/worst(b) cases. The penetration of electron distribution from the source extension to the channel seen in Fig. 7(b) is derived from this low p-n junction barrier.

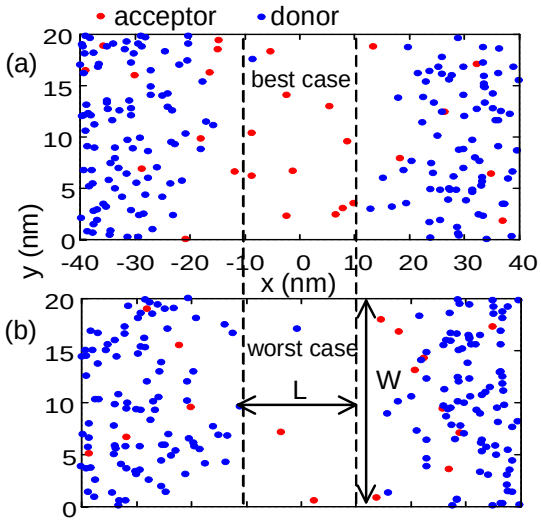

Fig. 9. Top view of the position of impurities in the substrate near the surface ($-5 \leq z \leq 0$ nm) for the best(a)/worst(b) cases. The worst case contains only two acceptors under the gate near the surface, thus the channel-source p-n barrier does not form well, or, equivalently, the location of source-to-channel p-n junction goes into the channel region. Figures 6 to 9 explain that the electron penetrated from the source to the channel due to the RDF-induced statistical variations of p-n junction is responsible for intrinsic J_g variations at $V_g \approx +0$ V.

To examine which factor contributes to J_g variations, the electron potential across the gate oxide and electron density profile of the worst and the best J_g case in Fig. 3 are shown in Fig. 6 and Fig. 7, respectively. Usually one can interpret that the stronger the normal oxide field F_{ox} is, the larger J_g flows.

$$J_g \propto \int_0^\infty dE\, D(E) \ln\left[1 + \exp[(E_f - E)/k_B T]\right],$$

$$\begin{aligned} D(E) &= \exp\left[-\frac{4\sqrt{2m_{ox}^*}}{3\hbar e F_{ox}}\right] \\ &\times \left((\phi_{ox} - E)^{3/2} - (\phi_{ox} - eF_{ox}t_{ox} - E)^{3/2}\right). \end{aligned}$$

However, interestingly, Fig. 6 illustrates that the normal gate oxide fields in the worst case are more moderate than those in the best case. Rather, Figs. 7(a) and (b) indicate that the electron penetrated from the source extension region to the channel is responsible for intrinsic J_g variations under positive bias conditions. The surface potential across the channel in Fig. 8 explains that the electron penetration is derived from the imperfect formation of source-to-channel p-n junction. The impurity profiles plotted in Figs. 9(a) and (b) confirm that the strong charge sharing effect (short-channel effect) by source in the worst case leads to this penetration. The effects of RDF-induced statistical variations of p-n junction location on J_g variations are more critical than the effects of RDF-induced normal oxide field variations.

In order to verify the relation between a device with strong short-channel effect and a device with strong gate leak current, the correlation between V_{th} and J_g at the same $V_g = \langle V_{th} \rangle$

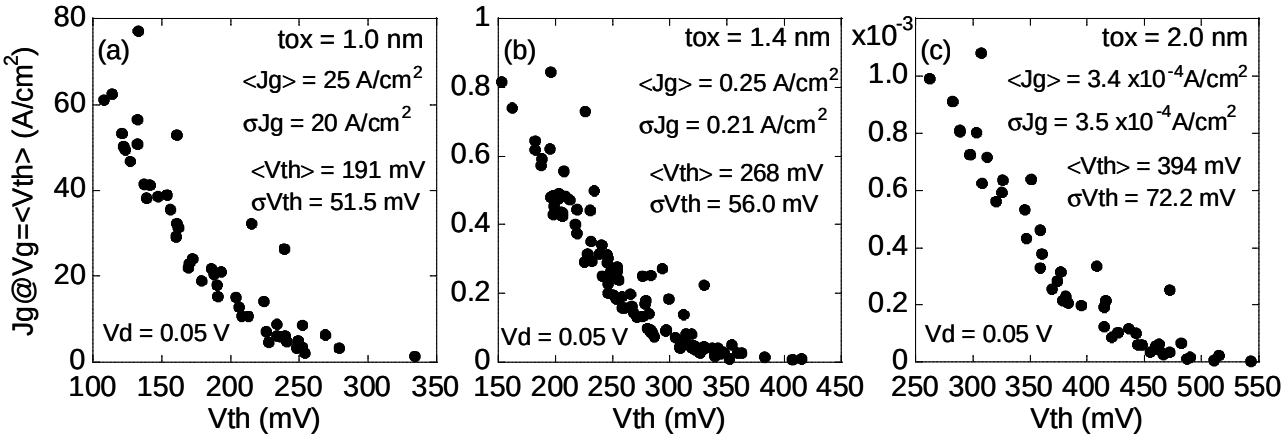

Fig. 10. Correlation plots between V_{th} and J_g at $V_g = \langle V_{th} \rangle$ with gate oxide thickness (a) t_{ox} = 1.0 nm, (b) t_{ox} = 1.4 nm, (c) t_{ox} = 2.0 nm. In all simulated t_{ox} cases, there is a negative correlation between V_{th} and J_g; as V_{th} decreases, J_g increases.

for t_{ox} = 1.0, 1.4, 2.0 nm devices are examined and plotted in Fig. 10. It is clearly seen that, for all simulated tox cases, there is a negative correlation between V_{th} and J_g; as V_{th} decreases, J_g increases. This is simply understood by that a MOSFET having low V_{th} stores more electrons as a MOS capacitor than the other MOSFETs compared on the same V_g; there is a large amount of electrons contributes to J_g. These results support that short-channel effects associated with the RDF-induced variations of p-n junction location enhance gate tunneling current fluctuations.

Mesh size dependencies of $\langle J_g \rangle$ and σJ_g are also studied and summarized in Fig. 11. The simulation region, -60 nm$\leq x \leq$ 60 nm, 0 nm$\leq y \leq$ 20 nm, -30 nm$\leq z \leq$ 0 nm in Fig. 2, is divided with a cube equal to this mesh size, whereas the grids in the other region are calculated automatically. Using only the long-range components of coulomb potential, no significant mesh dependence is observed [2] .

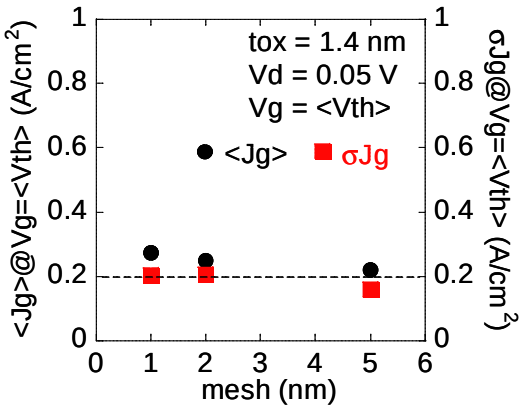

Fig. 11. Mesh size dependencies of $\langle J_g \rangle$ and σJ_g. Each point is derived from 100 statistical simulations. The broken line serves to guide the eye. No significant mesh dependence is observed.

IV. Conclusion

In summary, intrinsic gate tunneling current fluctuations induced by random dopant effects are investigated. It is shown that gate leakage currents considerably deviate among MOSFETs even if there is no gate oxide thickness fluctuation. The physical origin of the random-dopant-induced gate tunneling current fluctuations derive from the fluctuations in p-n junction location between source and channel region, rather than from the fluctuations in normal oxide field. Statistical variations of p-n junction location are essential for ultra-small MOSFETs and should be appropriately taken into account.

To incorporate fluctuations in quantum confinement effects due to random impurities is our next challenge.

[2]We also tried to incorporate the full or bare coulomb potential into the Poisson solver for the comparison, however, the simulation did not converge. Using only the long-range components of coulomb potential ensures good convergence as well.

Acknowledgment

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