MOSFET Modeling Beyond 100nm Technology: Challenges and Perspectives

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***Abstract* - Evolution of compact models is reviewed. The development trend leads to models based on the channel surface potential, allowing higher accuracy and a reduced numbers of model parameters. It is demonstrated that the model accuracy for higher-order phenomena, which is prerequisite for accurate RF circuit simulation, can be achieved without any new model parameters in addition to those for describing the I-V characteristics. Remaining problems to be solved are also discussed.**

I. INTRODUCTION

MOSFET technology is leading semiconductor industries through aggressive size reduction. To achieve further scaling down, also improvement of the device structure has been undertaken such as multi-gate MOSFETs [1]. Application of advanced MOSFETs to circuits is an additional urgent task to meet required high performances. For this purpose compact models of the devices are indispensable.

Here focus is given on compact modeling of advanced MOSFETs for circuit simulation. It is often believed that compact models are not directly based on device physics, and compact-model developers believed that precise device physics is much too complicated to be applied to circuit models. However, as microscopic device phenomena are becoming to dominantly affect device features [2], compact models cannot ignore the physics behind the phenomena any more. Otherwise the model cannot predict features of the devices and also the enormous increase of the number of model parameters cannot be stopped. Here some examples will be demonstrated, how compact models are evolving. This paper further aims at providing an analysis of serious device characteristics for circuit aspects. Measurements of higher-order device features used for developing compact models are shown to provide insight of microscopic carrier dynamics. RF applications of advanced devices are focused to attain this aim.

II. MEYER MODEL

The first circuit simulation model of MOSFETs was developed by Meyer is therefore called the Meyer model [3]. In stead of solving all coupled basic device equations, the Meyer model describes all device features with simple analytical equations as

$$I_{\rm ds} = \frac{\mu_s C_{\rm ox} W}{L}\left[V_{gs} - V_{\rm th} - 0.5V_{ds}\right]V_{ds}, \quad V_{gs} > V_{\rm th}, \tag{1}$$

$$C_{gs} = \frac{2}{3}WLC_{\rm ox}\left[1 - \frac{(V_{gd} - V_{\rm th})^2}{(V_{gd} + V_{gs} - 2V_{\rm th})^2}\right] \tag{2}$$

$$C_{gd} = \frac{2}{3}WLC_{\rm ox}\left[1 - \frac{(V_{gs} - V_{\rm th})^2}{(V_{gd} + V_{gs} - 2V_{\rm th})^2}\right] \tag{3}$$

$$C_{gb} = 0 \tag{4}$$

The current equation was originally derived by C. T. Sah and is based on the drift approximation valid beyond threshold voltage $V_{\rm th}$ [4]. Thus the modeling approach is often called $V_{\rm th}$based. All elements are shown in Fig. 1. An advantage of these equations is that they are functions of applied voltages, allowing designers to obtain required information for their design by hand calculations. These Meyer-model equations allow even deriving analytical formulations for circuit performances. This simplified MOSFET model has been good enough for predicting circuit performances for early technology generations. However, the Meyer model became insufficient for advanced technologies. The most serious problem of the Meyer model is the lack of short-channel effects in the model description. Worldwide used models of the BSIM generations are descendants of the Meyer model and included the advanced technology effects after requirements from the design community [5].

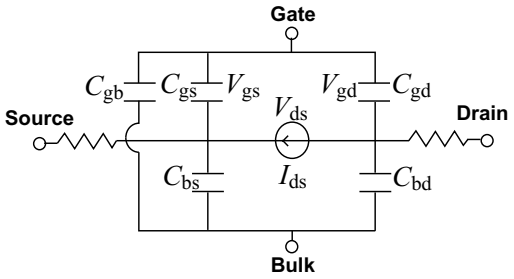

Fig. 1.. Basic equivalent circuit of a MOSFET developed by Meyer.

III. COMPACT MODELS

Circuit simulators solve the continuity equation in the form [6]

$$I_{ds}(t) = I_{ds0}(t) - \frac{dQ_{ds0}}{dt} \tag{5}$$

obtained by integrating the equation along the channel under the assumption that the potential respond spontaneously to the voltage change. The SPICE simulator solves the equation for an ensemble of many transistors in a circuit at the same time. The algorithm for solving the matrix consisting of the node times the number of transistors elements has been developed originally by Peterson and its basic concept is still kept [7].

Compact models treat the two remaining equations of the basic device equations. For this purpose two different major modeling approaches have been investigated in parallel during last decade [8]. One is the surface-potential based model with the drift-diffusion approximation, and the other is the inversion-charge based model, describing all device features as a function of this charge.

A. Surface-Potential Based Model

The surface potential is calculated by solving the Poisson equation. Here two different approaches have been developed. One is implemented in a model called HiSIM and solves the Poisson equation iteratively in the same way as numerical device simulators but with a quasi 2D algorithm. Calculated surface potentials are shown in Fig. 2 [9,10]. The other is implemented in a model called PSP and approximates the surface potential by mathematical functions with applied voltages as variables [11,12]. The reason for approximating with mathematical functions is to reduce simulation time by eliminating otherwise unavoidable iterations. However, the simulation time with the iteration approach turns out to be faster than for the analytical approach [13,14].

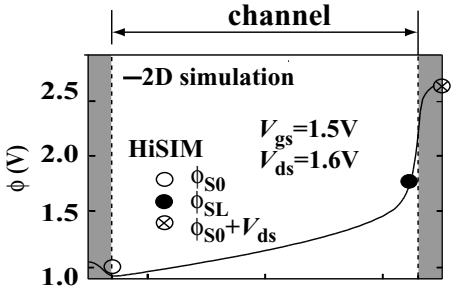

Fig. 2.. Calculated surface potential by HiSIM at source side ϵ_{s0} and at drain ϵ_{sl} under the saturation condition. Simulated surface-potential distribution along the channel with the 2D simulator is also depicted for comparison.

B. Inversion-Charge Based Model

To avoid the complicated formulations of surface-potential based models, inversion-charge based models have been developed [15-18]. The models describe all device features with charges calculated in different ways. Mostly they are formulated as functions of applied voltages. The linearization of the charges as a function of applied voltages simplifies all descriptions. One disadvantage of this method is that the subthreshold characteristics are described by a parameter n, which causes disconnection of the model with technology used for MOSFET fabrication.

IV. RF APPLICATIONS

Application of MOSFETs to RF circuits is very tough due to many undesired characteristics of the MOSFETs. RF circuits consist of many different functions as shown in Fig. 3 [19]. Timing core of RF-circuits is often a PLL providing high frequency oscillations. Under high-frequency operation higher-order phenomena of MOSFETs become obvious. Typical higher-order phenomena include harmonic distortion, noise, and carrier response delay. The effects of these phenomena on circuits are schematically shown in Fig. 4 [20]. The harmonic distortion is originated by non-linearity of the device response to applied voltages, which induces additional signals as schematically shown in Fig. 5. Each additional signal is widened by noise contributions as schematically shown in Fig. 5. This causes undesired signal couplings. Modeling of these phenomena is discussed with the use of HiSIM as an example.

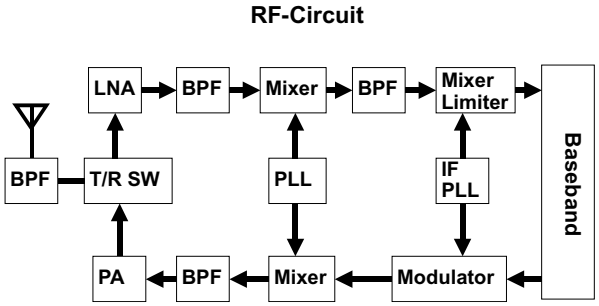

Fig. 3.. A typical RF circuit.

A. Harmonic Distortions

Under specific bias conditions the harmonic distortion can be analyzed from the device physics point of view. Fig. 6 shows a comparison of the harmonic distortion and derivative of mobility [21]. Singularities observed in the harmonic distortions can be attributed to those of the mobility. At high frequencies these singularities are governed by carrier dynamics rather than the mobility alone [22].

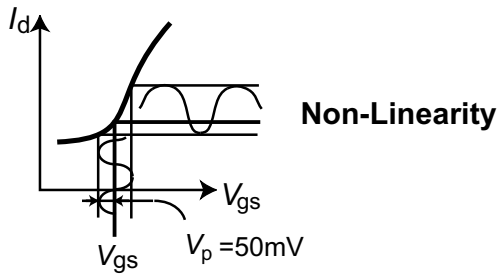

Fig. 4.. Input signal with sinusoidal small signal of amplitude V_p and frequency f_0. Due to the non-linearity of MOSFET response, harmonic amplitude with higher-order frequencies are observed.

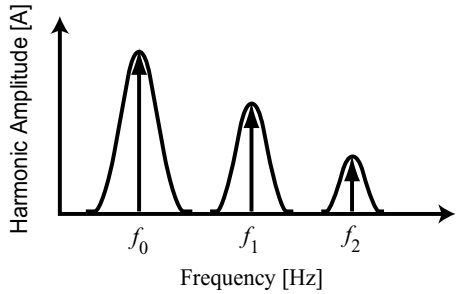

Fig. 5.. Harmonic distortions observed. The widening of the signals are caused by noise contributions.

B. Noise Features

Advanced MOSFETs are suffering from two dominating noise mechanisms: the $1/f$ noise and the thermal noise. The $1/f$ noise is mainly caused by trap/detrap at the oxide/substrate interface [23]. Thus modeling for the noise requires to integrate the carrier distribution along the channel, and the finial formula is a function of carrier concentration at source and drain [24].

Modeling of the thermal noise is based on the Nyquist theorem considering the noise source as a resistance [25]. This theory is extended to the transistor by van der Ziel, where the thermal noise is the integration of the channel conductance along the channel [26]. Fig. 7 shows predicted thermal noise with HiSIM in comparison to measurements [27]. The increase of the noise coefficient under the saturation condition with reducing the gate length is attributed to the potential increase along the channel.

Here it is worthwhile to notice that model parameters are required only for the $1/f$ noise to describe the trap density and the mobility modification due to the trapped charge. These parameters are nearly universal, if the technology is mature. Thus most of the higher-order phenomena can be predicted by simple measured I-V characteristics. This fact concludes that the majority of carrier dynamics is still governed by the drift-diffusion mechanism. Further noise investigation such as the gate-

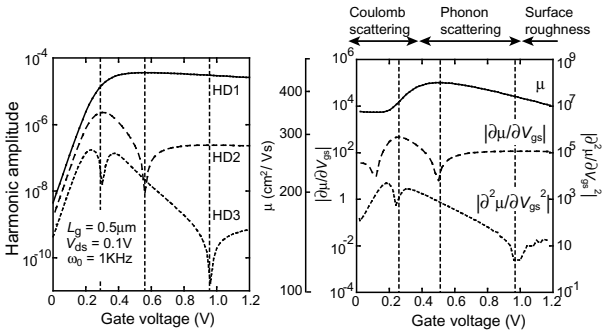

Fig. 6.. (a) Simulated harmonic distortion characteristics at low drain bias and low frequency (1KHz). (b) Mobility model of HiSIM and its derivatives.

current induced noise observed in the higher frequency regime [28], for example, might give important information about carrier dynamics in the tunneling.

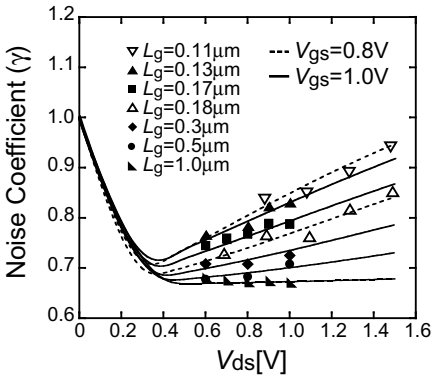

Fig. 7.. Calculated noise coefficient γ with HiSIM as a function of drain voltage V_{ds} compared with measurements.

C. Non-Quasi-Static Effect

Under high-frequency operation the current response is different from predicted results with a conventional model as shown in Fig. 8. These differences are known as the non-quasi-static(NQS) phenomena and they occur due to the approximation in modeling that carriers respond instantaneously to the changes of applied voltages. Such a response without delay is called quasi-static(QS) approximation. The strange behavior of the current shown in Fig. 8 is an artifact of the modeling assuming instantaneous response of carrier dynamics to a voltage change. The modeling NQS effects is done by including the carrier transit delay in the form [29].

The high-frequency operation is usually investigated in the frequency domain, which can be done by transforming from the time domain into the frequency domain through the Fourier transformation. The result of the harmonic distortions under high-frequency is shown

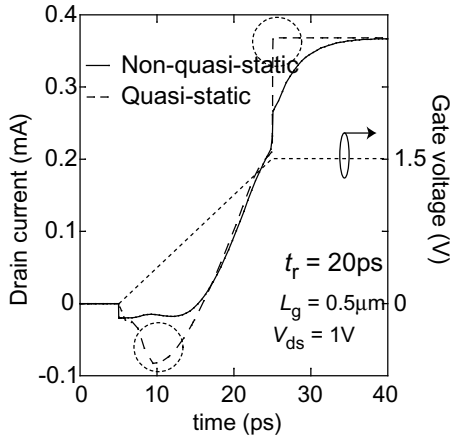

Fig. 8.. Transient drain current for 20ps rising input. Quasi-static artifacts are eliminated with non-quasi-static model.

in Fig. 9, where results of 2D device simulation are also compared [22].

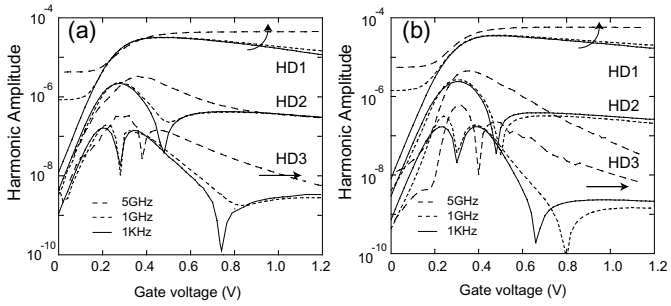

Fig. 9.. Harmonic distortion characteristics at different frequencies. (a) HiSIM results, and (b) 2D simulation results.

The most often used analysis for characterizing high-frequency response of devices is with the admittance matrix, of which the elements are called Y-parameters. There are approaches to model the response by solving the continuity equation together with the current density equation analytically. The final description reduces to an expression of the Bessel functions. Comparison of model calculation results and measurements are shown in Fig. 10 [30]. For the comparison the calculation results under the QS approximation are also depicted. For the QS calculation only linear terms of the frequency are considered. NQS effects become obvious at frequency beyond 1/3 of cut-off frequency.

V. SMALL GEOMETRY

One advantage of the size reduction is the improvement of the integration density as well as high-speed circuit operation. Logic circuits fully profit from the improvement by applying the smallest size transistors available.

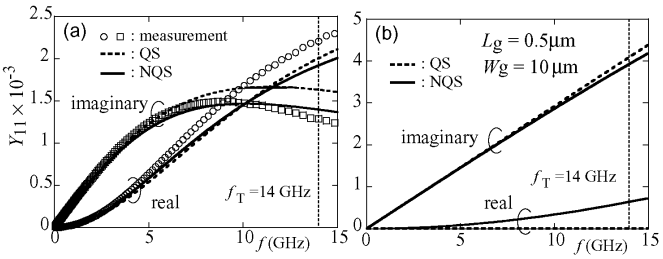

Fig. 10.. (a) Measured (open symbols) and calculated Y-parameters with the NQS model (solid lines) and the QS model (dashed lines). (b) Comparison of the NQS and the QS results without the gate-resistance contribution.

However, the reduction of device size enhances not only the noise as can be seen in Fig. 11 [24] but also the loss of technology control. From the compact modeling point of view it is impossible to predict the device features due to many fitting parameters introduced for reproducing measurements. On the other hand the 2D numerical simulations suffer from extracting accurate impurity profiles, where all device features are derivatives of the profile. Enhanced technology variations are also due to the lack of technology control as shown in Fig. 12 [31]. Intensive efforts have been given to understand the origin of these limitation of technology control, and to realize predictability not only by describing the variations just with fitting parameters. This is important to forecast the limits of the technology development which we are approaching now. On the circuit simulation side the number of model parameters increases accompanied with losing their physical meanings and this brings the end of reliable circuit simulation.

VI. TASKS IN FUTURE

Modeling of phenomena observed in advanced MOSFETs requires measurements which can be achieved with sophisticated techniques. Sophisticated numerical simulators such as Monte Carlo simulations support the analysis of the measurements by enabling microscopic insight of the measurements. Furthermore, they provide even supplements of the measurements, which is proved in its accuracy through analysis with compact models. Development of multi-gate MOSFETs will be one of such examples. With the numerical simulation results whose reliability has been proved through investigations in the past, the essence of the device features is extracted and required phenomena to be modeled are focused. Such compact model development parallel to the device development is important to achieve short turn-around times as well as to suppress high investigation cost. No reliable compact model with this capability exists yet and a lot of effort has to be given until it is available.

Accurate circuit simulation is eagerly requested. As

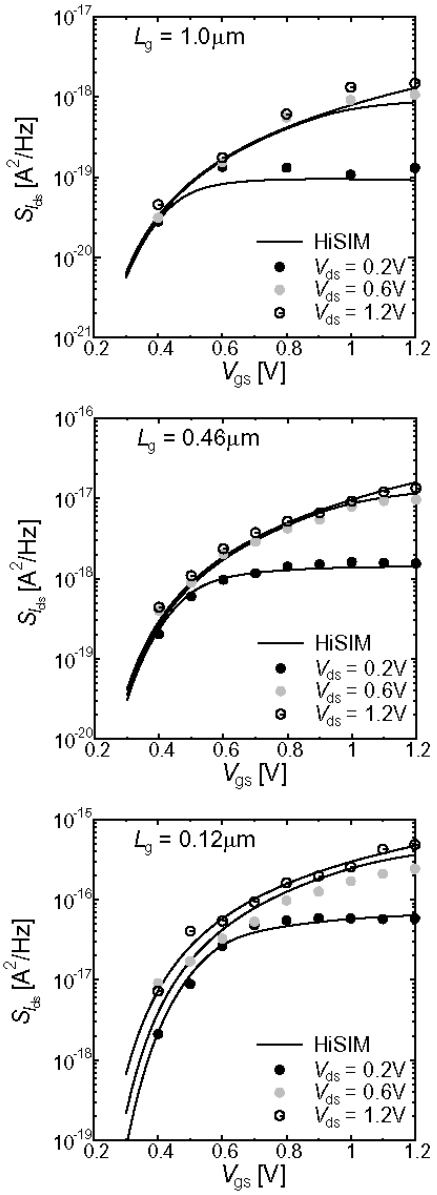

Fig. 11.. Comparison of the bias dependence of measured and simulated drain current noise by HiSIM at a frequency of 100HZ.

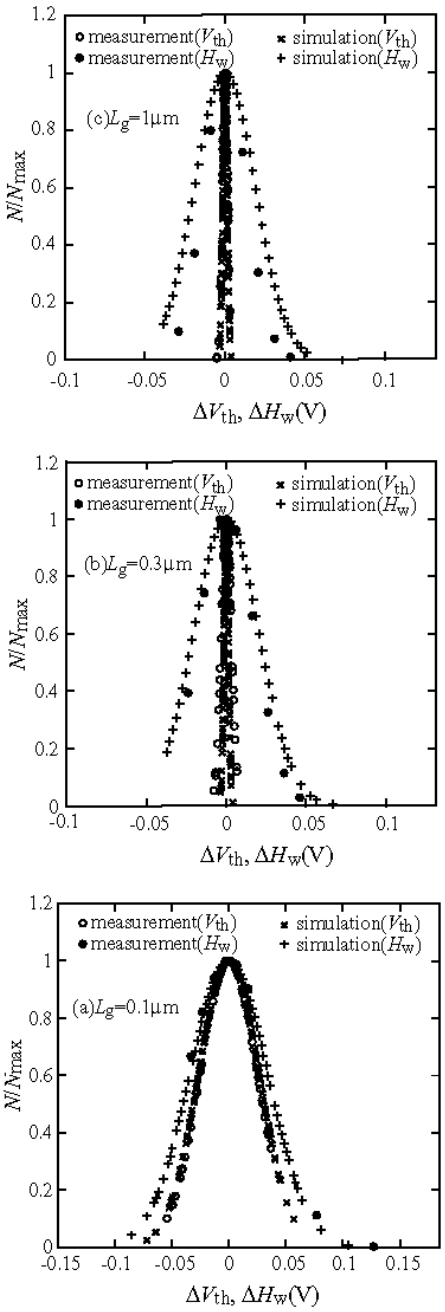

Fig. 12.. Comparison of variations for different gate length L_g. Variations are focused on the threshold voltage V_{th} and the hysteresis width H_w of a differential-amplifier-stage circuit.

can be seen in the RF circuit shown in Fig. 3, the circuit consists of many different functions. It is desired to simulate the ensemble of all these functions at the same time to secure the total circuit function. For this purpose not only modeling the intrinsic part of devices but also the interconnection of these devices has to be modeled. Extraction of interconnect features and their modeling have been intensively undertaken. To generalize each extraction is a difficult and time consuming task.

Circuit performance is basically originated from device characteristics. However, it is also governed by surroundings with different densities of neighbor devices. The well, introduced for realizing the CMOS monolithic integration techniques is causing many additional influences on device performances. In future even if the device itself is well understood, newly occurring problems caused by integration density and interconnects require still a lot of effort to understand.

VII. CONCLUSION

The development trend in compact modeling goes towards surface-potential based approaches and leads to

models with high accuracy and less model parameters. The main motivation for this trend is to realize RF circuits with MOSFETs, where many higher-order phenomena affect the circuit performance. The trend towards the surface potential brings compact modeling for circuit simulation much closer to higher dimensional numerical device simulation. Therefore, both can now come together and work united for the common goal of realizing rapid technology progress for the benefit of the society.

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