Physics and Modeling of Radiation Effects in Advanced CMOS Technology Nodes

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Abstract

The paper first describes the basic radiation-induced mechanisms such as transient effects, ionization phenomena and displacement damage. Subsequently, the impact of irradiation on advanced CMOS technology nodes is demonstrated in order to illustrate the underlying physical phenomena. Both bulk and silicon-on-insulator (SOI) technologies will be addressed. A third section discusses the present understanding and the difficulties associated with modeling of irradiation-induced device degradation. Finally, an outlook is given for some emerging semiconductor technologies such as e.g. SiGe, strained silicon, Ge and GeOI. Some aspects of cryogenic irradiations, of key importance for space applications, are also briefly mentioned.

1 Introduction

Although there exists a variety of radiation-harsh environments (space, nuclear, high energy physics, etc) here only semiconductor devices for space applications will be discussed. This implies that energetic particles such as electrons, protons, cosmic rays and heavy ions are important. For a long time radiation studies were a special research field and the used devices and circuits were only processed in so-called radiation-hard technologies. However, since the last decade the space community is more and more switching over to Commercially-Off-The-Shelf (COTS) components due to the need of high performing devices for e.g. imaging, data processing, etc. The use of standard devices strongly reduces the system design time and the overall system cost, but puts more emphasis on risk analysis. The authors have recently reviewed in depth the different aspects of radiation effects in advanced semiconductor materials and devices [1]. In this paper only technology aspects are treated, while for system optimization also hardness-by-design techniques are sometimes used.

2 Basic Radiation Mechanisms

In general, after irradiation the occurrence of two main mechanisms can be observed [see e.g. 1-3], i.e., ionization damage due to the generation of electron-hole pairs resulting into trapping effects in the device dielectric layers and/or at its interface with

the silicon, and displacement damage caused by the displacement of silicon atoms from their regular lattice sites. The amount of damage depends on the irradiation conditions (type of particle, fluence or dose, energy, temperature, etc) and has either a transient (e.g. single events upsets (SEU) or latch up (SEL)) or a permanent nature. The ionization effects in SiO_2 are well understood. The degradation of electrical device parameters, such asthreshold voltage and transconductance, is caused by hole trapping in the oxide leading to positive charge buildup. The latter elapses with time due to tunneling and emission phenomena and/or the generation of interface traps. In the case of advanced devices making use of a high dielectric constant material in combination with either polysilicon or metal gates the present knowledge is rather limited. This issue is further addressed in section 3.3. For silicon the displacement damage has been studied in detail and suitable models are available, while additional effort is needed for some of the alternative substrates (e.g. SiGe, strained Si, Ge, etc) which are gaining more and more interest for future technology nodes. This is briefly covered in the last section.

3 Radiation Effects in Advanced CMOS Technologies

This section focuses on advanced CMOS based technologies and will briefly address issues concerning deep submicron bulk devices, performance and new physical phenomena in SOI technologies, special effects in ultra-thin SiO_2 gates, and high-k dielectrics.

3.1 Bulk CMOS Technologies

Scaling down the minimum feature size of the devices goes along with a scaling of the gate oxide thickness, which has a positive impact on the radiation hardness.
For a positive gate bias the irradiation-induced threshold voltage shift is quadratic with the oxide thickness. However, for a thickness below 6 nm the trapped holes immedately recombine with electrons tunneling from the substrate so that the net hole trapping is zero. [4-5]. Therefore, deep submicron CMOS technologies are expected to be inherently radiation hard for not too high total dose. However, the generation of interface traps can create a lateral non-uniform device degradation whereby a different trap distribution is observed near source and drain [6]. The locally enhanced electric field is at the basis of the gate-induced drain leakage (GIDL), which increases after irradiation, especially for p-channel devices [7].
In addition, one has to take into account that the fabrication of these devices is based on the use of advanced processing steps (e.g. dry etching, e-beam or ion beam lithography, sputtering, etc) which may introduce plasma damage resulting in direct or latent damage in the oxide [8].
A good radiation performance has been reported for a 0.18 and 0.13 μm technology node, respectively [9-10]. The fact that these technologies use a shallow trench isolation (STI) technique has a beneficial impact due to the elimination of radiation sensitive thick field oxides and, especially, the non-existence of a bird's beak region, typical for LOCOS-based isolation techniques. However, for STI one has to take into account the radiation behavior of the trench filling dielectric and parameters such as

the high electric fields at the edges, the parasitic transistor threshold voltage and in some cases also the implantation damage [11].
For a deep submicron technology care has to be taken that displacement damage doesn't lead to a change in the doping profiles associated with the lowly doped drain and halo implantations implemented to control short-channel effects [10]. This effect can be observed as a gate length-dependent variation of the post-irradiation electrical parameters, as illustrated in Fig. 1 for the threshold voltage change of transistors processed in a 0.13 μm technology. In this case, a $5x10^{11}$ p/cm^2 60 MeV proton irradiations, causes a cross-over behavior [10].

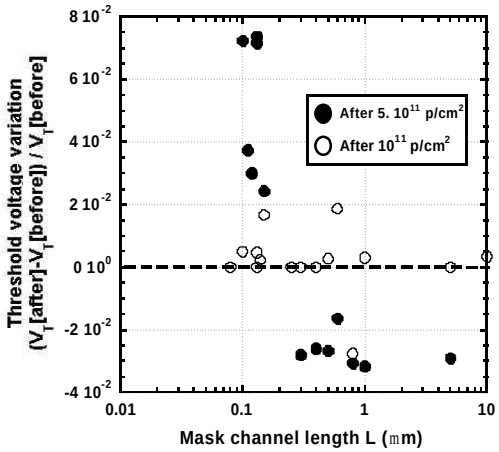

Figure 1: Normalized threshold voltage change versus channel length after a 60 MeV proton irradiation for RNO n-MOSFETs.

3.2 SOI Technologies

Originally, Silicon-on-Sapphire (SOS) and Silicon-on-Insulator technologies were only used for the niche market of radiation-hard applications. In recent years, however, SOI is more and more used for commercial applications and even expected to become a key technology for 45 nm and below technology nodes [12]. Some up-to-date reviews on radiation effects in standard SOI devices have been published [13-14]. An important difference with bulk devices is the presence of a buried oxide (BOX) under the thin silicon film. After irradiation, the irradiation-induced hole trapping in the BOX may cause an increase of the leakage current of partially depleted (PD) and an increase of the leakage current and a threshold voltage shift of fully depleted (FD) n-channel devices, respectively. In case of a LOCOS-based isolation technique one also has to take into account the possible hole trapping at the edge of the isolation regions [14]. Both effects will be reduced for thinner silicon films and are not present for p-channel devices as the hole trapping then causes accumulation of the film.

Recently, it has been observed that SOI devices with an ultra-thin gate oxide exhibit the Linear Kink Effect (LKE) in linear operation (i.e. low drain bias V_{DS}). As soon as the gate voltage is higher than the threshold for electron valence band (EVB) tunneling a kink effect is occurring, resulting in an increase of the drain current and the appearance of a second peak in the transconductance curve. This effect has been discussed in detail and the impact of different technological parameters is well understood [15]. After an ionizing irradiation the LKE effect becomes more pronounced so that the height of the second peak increases and shifts to higher front-gate voltages as shown in Fig. 2. The latter effect is caused by a reduction of the threshold voltage. The figure also clearly shows a hysteresis in the curve, caused by transient effect.

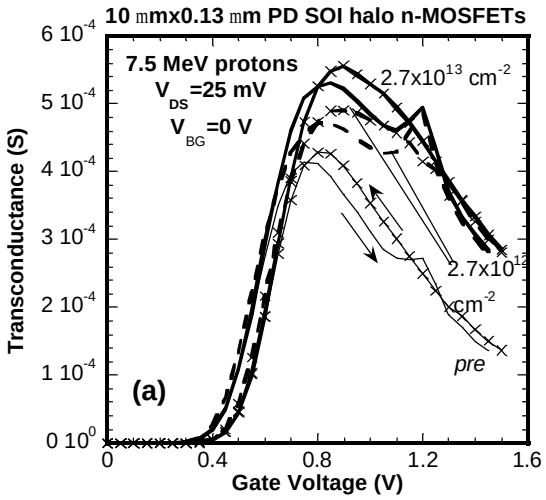

Figure 2: Transconductance versus gate voltage for two 10 μmx0.13 μm PD SOI n-MOSFETs, irradiated by 7.5 MeV protons to a fluence of $2.7x10^{12}$ and $2.7x10^{13}$ p/cm^2, respectively [15]. The arrows indicate the direction of the gate voltage sweep.

The majority carriers introduced in the silicon film by EVB tunneling also have a pronounced impact on the drain current transients observed when the drain current is switched from a high to a low front gate voltage [16-17]. This is illustrated in Fig. 3. A model based on the body potential behavior has been developed, explaining the transient shape dependence on the experimental conditions [18]. Figure 3 also clearly points out that after irradiation the removal of the excess majority carriers is faster, leading to shorter transient times.

Finally it is important to mention that the LKE is also associated with an excess Lorentzian low frequency noise component [19], caused by the RC filtered shot noise from both the forward-biased source-film junction and the EVB tunnel current [20]. After proton irradiation the excess noise increases for n-MOSTs, while it remains unchanged for p-MOSTs [21].

In the case of FD devices the front-back gate coupling can be very pronounced [22]. After irradiation the amount of coupling depends on the degradation of both the front and the back gate oxide [23].

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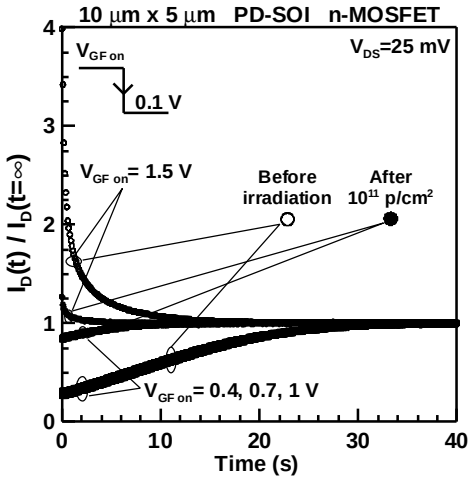

Figure 3: Normalized switch-off drain current transient before and after a 65 MeV 10^{11} p/cm^2 proton irradiation for a 10 μmx5 μm PD n-MOSFET. $|V_{DS}|$ =25 mV and $|V_{FG\,off}|$ = 0.1 V.

3.3 Gate Dielectrics

As discussed before, scaling also implies a reduction of the gate oxide thickness. For a gate oxide thickness around 6 nm some special phenomena have been observed. First of all there is the occurrence of Stress Induced Leakage Current, which is well known in the world of reliability studies. Closely related with SILC is the Radiation-Induced Leakage Current (RILC), which is obeying the same empirical conduction law that can be represented by a modified Fowler-Nordheim relation [24]. Both mechanisms can occur simultaneously in the devices. A model has been developed to describe RILC as a function of several parameters such as oxide thickness, applied electrical field during irradiation and total dose and dose rate [4]. RILC is attributed to trap-assisted tunneling (TAT) via radiation-induced neutral electron traps (NET) It is important to remark that RILC is mostly only observed for a high total dose (in the Mrad(Si) range) so that it should be less a problem for space applications. Bias and thermal annealing can be used to reduce the RILC [25].
Another post-irradiation observed phenomenon is the occurrence of Quasi Breakdown (QB). The leakage current is higher than for RILC and in contrast to RILC can not be fitted by a F-N law [4]. The origin is related to the formation of large area conductive paths in the oxide, but not resulting in catastrophic breakdown. This region can also be well characterized by using low frequency noise measurements.

For ultra-thin gate oxides below 3 nm the gate tunnel current will dominate the power consumption. Therefore, for low power applications the approach is to use a material with a higher dielectric constant (high-k material). A first step is to switch over a nitrided (NO) or reoxidized nitrided oxide (RNO). This has also a beneficial impact on the reliability and the resistance against boron penetration from the p-channel polysilicon gate electrodes. From a radiation hardness viewpoint, under optimized fabrication conditions, these dielectrics are in general performing as good or even better than standard SiO_2 (see [1] for an overview). The next step is to use new high-k materials Such as e.g. Ta_2O_2, TiO_2, HfO_2, ZrO_2, La_2O3, etc [26]. Although presently there is no clear 'winner' a huge amount of effort has been devoted to HfO_2. For only a few of these materials a very restricted number of publications are dealing with the radiation hardness performance and there is surely no clear overall picture. To some extent this is related to the fact that the pre-irradiation performance of these dielectrics is in many cases not optimized yet. For a not too high total dose irradiation can have a beneficial impact on the properties of the dielectric layer resulting in a reduction of the leakage current [27] or interface trap concentration [28]. Al_2O_3/SiO_xN_y stacks have a good radiation resistance up to 10 Mrad(SiO_2) in case that proper annealing steps are used, pointing out the promising potential of these high-k dielectrics [28].

4 Radiation Modeling

The major effect of ionizing radiation is the generation of electron-hole pairs, resulting in positive trapped charges in the oxide layer and an increase in the interface-trapped charge density. Several models have been developed to determine the charge generation as a function of the irradiation conditions (dose, energy, dose rate, etc). This requires in the first place a good understanding of he physical mechanisms involved, which can be obtained by either ab-initio calculations (see e.g. [29-30]) or semi-empirical approaches. Examples of the latter are e.g. the electron paramagnetic resonance investigations [31] performed to get an insight into the P_b centers (silicon dangling bond related centers) and the E' defects (trapped holes at oxygen vacancies), and the charge pumping measurements for pointing out the role of molecular hydrogen in the formation of interface traps [32]. Numerical or analytical modeling and statistical Monte Carlo simulations are used to explain the experimental results reported in the literature.
The basic radiation mechanisms and their effect on the electrical device performance are well understood and can with success be modeled. However, dedicated efforts are required to explain some specific technological issues such as e.g. the charge generation associated with isolation structures (the bird's beak region in LOCOS, edges and corners in STI structures, etc) and the charge trapping in buried oxides in SOI devices. The latter was discusses in section 3.2.

5 Outlook

Due to space restrictions only a selected number of topics have been issued. However, for near future advanced technologies it is important to mention that beside SOI also alternative substrates are getting a lot of attention. The most important ones are SiGe,

strained Si, strained SiGe on relaxed buffer layers and even Ge and GeOI. The driving force is the required enhancement of the carrier mobility, which is degraded by scaling down the technology due to enhanced Coulomb scattering and presently also to the use of high-k gate dielectrics. Using sandwich layers consisting of a high-k dielectric on a very thin SiO_2 interfacial layer can partly solve the latter. For most of these materials, except for SiGe and some older Ge work, the published information on radiation hardness is very limited.

Beside the use of alternative substrates, huge efforts are concentrating on alternative device structures such as e.g. vertical transistors, double and multiple gates, FinFETs, Silicon-on-Nothing, etc. The benefits of a multiple gate device were already demonstrated in 1990 when Gate-All-Around (GAA) transistors were realized [33]. Devices processed in a 3 μm technology have been tested up to a total dose of 30 Mrad(Si), as illustrated in Fig 4 for the threshold voltage and the transconductance {34]. The transconductance decreases monotonously with dose, while the V_T shows a rebound effect.

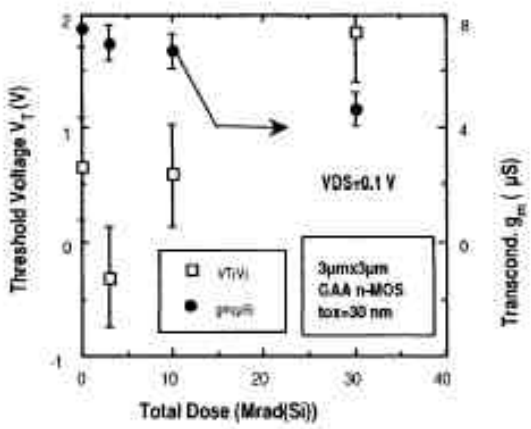

Figure 4. Variation of the threshold voltage and the maximum transconductance of Gate-All-Around nMOST as function of total dose [34].

Beside these early results, it can be stated that for the alternative device concepts radiation testing is still in an early phase. Computer simulations point out that double gate devices are expected to be less radiation sensitive than single gate ones [35].

Another important issue for space applications is the fact that, depending on the orbit of the spacecraft, the irradiations are done at cryogenic temperatures. For ionizing radiation this implies that due to the strong reduced transport a higher amount of charge is build up than at room temperature. For 90 K irradiations some modeling attempts have been reported [36]. However, for several space missions the readout electronics is operating at temperatures as low as 4.2 K. Therefore, for total dose effects the on-earth cryogenic irradiation testing is necessary, as room temperature testing is not corresponding with the worst-case situation. Dedicated set ups are

needed to allow cryogenic irradiation and in-situ testing [37]. The latter is needed as otherwise annealing effects will influence the experimental observations.

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