# Analytical Modeling of Ge and Si Double-Gate(DG) NFETs and the Effect of Process Induced Variations (PIV) on Device Performance

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## Abstract

In this paper, we present a self-consistent, analytical model that includes carrier quantization; short channel effects (SCE) and calculates the ballistic currents in DGFETs. We use this new tool to compare the effect of SCE and process induced variations (PIV) on Silicon (Si) and Germanium (Ge) NMOS DGFETs. Our results show that in the case of DGFETs designed to meet the ITRS High Performance (HP) requirements, even with PIV, Ge performs better than Si. Whereas, due to its poorer SCE, in the case of DGFET designed to meet the ITRS Low Standby Power (LSTP) requirements, Ge performs worse than Si.

## 1 Introduction

Due to its higher mobility and better transport properties, Ge seems to be an attractive candidate as a channel material in highly scaled MOSFETs [l]. However, its higher dielectric constant and lower band-gap make it very susceptible to Short Channel Effects (SCE) and Process Induced Variations (PIV). We present a methodology developed to compare scaled Si and Ge DGMOS devices.

## 2 Simulation Methodology

The analytical simulation methodology that was used to model the DGFET is shown in Fig. 1. The effective masses that have been used in the calculations are as given in [2]. The carrier quantization effects based on advanced variational techniques [3] show excellent agreement, with those obtained by a numerical self-consistent 1-D Poisson-Schrödinger solver, over a wide range of substrate orientations and body thickness for both Si and Ge (Fig. 2). Analytical models are used to capture short channel effects [4,5]. Due to its higher dielectric constant , the short channel effects (DIBL and $V_T$ roll-off) in Ge are much worse than in Si (Fig. 3). The drive current for the device is calculated using a ballistic transport model [6,7]. The analytical simulator self-consistently solves for the ballistic currents, taking into account short-channel effects and carrier quantization. The appropriate gate work-function is used to meet the ITRS leakage current specification for a given node. Fig. 4 shows the $I_{DS}$-$V_{GS}$ curves obtained by using this analytical simulator for different substrate orientations. Our results show that Ge<110> has the highest drive current. This is in

good agreement with previously reported data [8]. In the next section, we compare the effect of PIV on the performance of Si<100> DGFETs with that of Ge<110> DGFETs.

## 3 Process Induced Variations

With increasing chip sizes and scaling transistor dimensions, Process Induced Variations (PIV) are becoming an important consideration in designing integrated circuits. Since Ge has a lower transport effective mass, we expect the drive currents to be higher. However, due to its poorer electrostatics and worse short channel effects, we expect it to be more susceptible to variations. It is important to evaluate these tradeoffs carefully. Shown in Fig.5 is the 2-D process space of devices, having a spread in their channel length ($L_G$) and body thickness ($T_S$). Compared to the nominal device, the device with a shortest $L_G$ and the thickest $T_S$ will have worst short channel effects and consequently the highest leakage current (Worst-case OFF device). On the other hand, the device with the longest $L_G$ and the thinnest $T_S$ will have the highest $V_T$ and the lowest current driving capability (Worst-case ON device). In this paper, we have performed a worst-case analysis by assuming a Gaussian distribution for a nominal $L_G$=18nm and nominal $T_S$=Lg/3=6nm (for good channel control) and $3\sigma$ variation of 10% about the mean.

## 4 Results and Discussion

Fig.6 shows the spread in the leakage currents and the drive currents respectively, for the HP Ge and Si DGFETs. The spread in the leakage currents and the ballistic drive currents for the Ge DGFET are larger than the Si DGFET. The $I_{OFF}$ for the Ge devices ranges from 2.49 μA/μm to 5.29 nA/μm while the $I_{OFF}$ for the Si devices ranges from 0.8 μA/μm to 14.9 nA/μm (nominal value 100 nA/μm). The $I_{ON}$ varies by 18% from the nominal for the Ge devices and 12% from the nominal for the Si devices. As seen in Fig.7, despite their larger variation, in the case of the HP device, the Worst-Case ON Ge DGFETs still have a higher drive current than the Si DGFETs. The spread in the currents is much larger for the LSTP devices compared to the HP devices and Ge devices show a much wider distribution than the Si devices. The $I_{OFF}$ for the LSTP Ge devices ranges from 11.3 nA/μm to 0.74 pA/μm while the $I_{OFF}$ for the Si devices ranges from 3.18 nA/μm to 3.8 pA/μm (nominal value 80 pA/μm). The $I_{ON}$ however, varies by 50% from the nominal for the Ge devices as compared to 29% from the nominal for the Si devices. The spread in the LSTP Ge DGFETs is so large that the drive current for the Worst-Case ON device drops below the worst-case on Si DGFET (Fig.8). The spread in the drive currents becomes even larger for both Si and Ge DGFETs as technology is scaled, due to worse immunity to PIV and short-channel effects. In the case of the HP DGFETs, Ge performs better than Si even at $L_G$=14nm. However, for the LSTP DGFETs, the spread in the Ge devices is very large and they perform much worse than Si. As we scale the channel length to 18nm, this effect is exacerbated and the Worst-Case ON Ge DGFET exhibits a much lower drive current than the Si device.

## 5 Conclusions

We have developed a self-consistent, analytical simulator that captures all the physical phenomena in DGFETs accurately. The simulator includes models to capture carrier quantization in thin bodies, short channel effects and ballistic currents. Using this new tool to compare the effect of variations on Si and Ge NMOS DGFETs, we find that Ge devices are very strongly affected by Process Induced Variations. In the case of DGFETs designed to meet the ITRS High Performance (HP) requirements, Ge outperforms Si. However, due to its lower immunity to PIV, in the case of DGFETs designed to meet the ITRS Low Standby Power (LSTP) requirements, Ge performs worse than Si. This effect is further exacerbated as we scale the technology node to smaller dimensions.

## References


[1] Takagi S., "Re-examination of subband structure engineering in ultra-short channel MOSFETs under ballistic carrier transport", Symposium on VLSI Technology, vol. A46-47, pp. 115, 2003.

[2] Ando T., et. al., "Electronic Properties of two dimensional systems", Rev. Modern Physics, pp. 437, 1982

[3] Ge L., et. al., "Analytical modeling of Quantization and volume inversion in thin Si-film DG MOSFETs", IEEE Transactions on Electron Devices, pp. 287, 2002

[4] Kim K., et. al., "Physical compact model for threshold voltage in short-channel double-gate devices", Simulation of Semiconductor Processes and Devices, pp. 223, 2003

[5] Chen Q. et. al., "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs", IEEE Transactions on Electron Devices, pp. 1086, 2002

[6] Natori K., et. al., "Ballistic metal-oxide-semiconductor field effect transistor", Journal of Applied Physics, pp. 4879, 1994

[7] Lundstrom M., et. al., "Essential physics of carrier transport in nanoscale MOSFETs" IEEE Transactions on Electron Devices, pp.133, 2002

[8] Low T., et. al., "Investigation of performance limits of germanium double-gated MOSFETs",International Electron Device Meeting, pp. 691, 2003


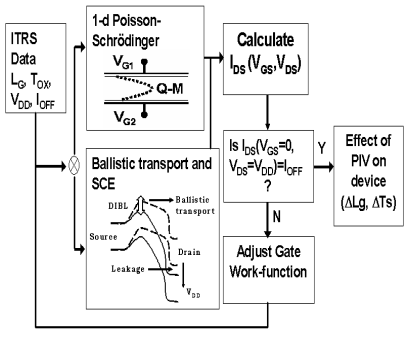


**Fig 1**: Flowchart depicting the simulation methodology used

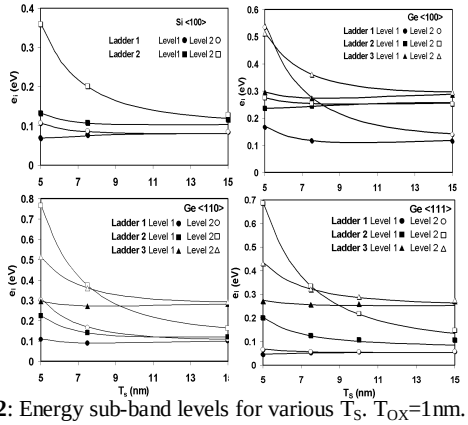


**Fig 2**: Energy sub-band levels for various $T_S$. $T_{OX}$=1nm. The symbols represent results from a 1-d Poisson-Schrödinger simulator. The solid lines represent results of the variational model used in this work.

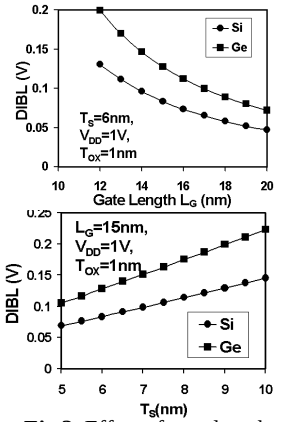


**Fig 3**: Effect of gate length and film thickness variation on DIBL

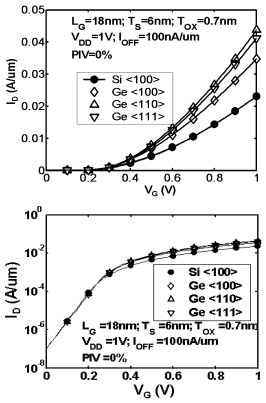


**Fig 4**: $I_D$-$V_G$ for $L_G$=15nm. Ge<110> has highest $I_{ON}$

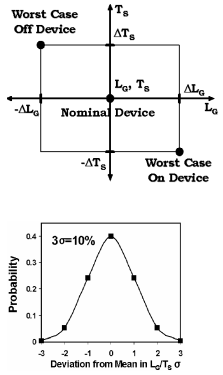


**Fig 5**: PIV:Gaussian distribution over $L_G/T_S$ was assumed with 3σ=10 % of $L_G/T_S$.

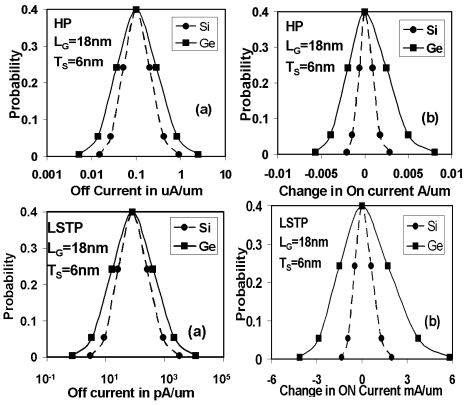


**Fig 6**: Distribution of the Off and On state currents for worst-case variations of σ, 2σ and 3σ in $L_G$ and $T_S$.

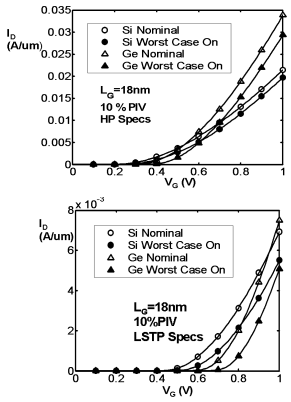


**Fig 7**: Comparison of $I_D$-$V_G$ for worst-case on device to nominal for Si and Ge

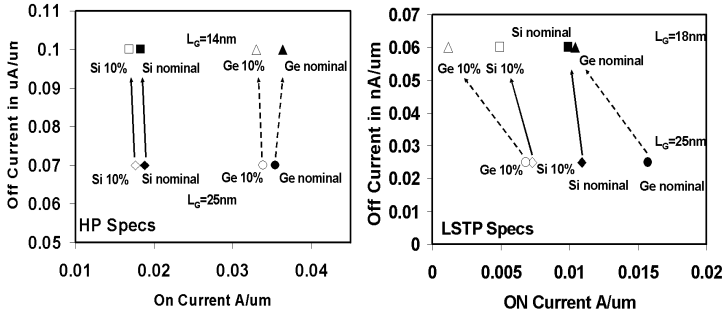


**Fig 8**: Effect of worst-case PIV on scaling devices from 25nm to 14nm.