Modeling and Simulation of Combined Thermionic Emission-Tunneling Current through Interfacial Isolation Layer

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Abstract

We present computer analyses of *I-V* and *C-V* characteristics based on an enhanced transport model, where the tunneling current through Schottky and MOS structures with a very thin interface insulation layer is properly included. Assuming a tunneling transmission probability T_{tr} through a potential-dependent barrier height in our model, which is calculated by the Global Matrix Method, the conformity of experimental and simulated data is significantly improved.

1 Introduction

Current transport mechanisms through structures with very steep doping profiles and narrow space charge regions including a very thin isolation layer are still not completely understood. Various sophisticated analytical models describing the tunneling effect in Schottky structures have been developed [1-3], but they hardly take into account the whole complexity of mutual interactions of different cooperating current flow mechanisms through the interface. In previous work [4,5] the tunneling effect had been included in the transport model by adding tunneling to the general generation-recombination term in order to improve the agreement between experimental and simulated characteristics.

2 Transport Model

The resulting compact formula for the total current flow comprehends drift and diffusion, thermionic emission, tunneling, Shockley-Read-Hall generation and recombination, Auger recombination, impact ionization, and their mutual interactions. In the case of a N-type semiconductor, the hole current for can be neglected, and thus we may write

$$J_{e} = q \frac{v_{TEe} v_{De}}{v_{TEe} + v_{De}} \left[n_{0} \left(\exp\left(\frac{qVa}{kT}\right) - 1 \right) + n_{SRH} + n_{IMP} + n_{TUNe} + \frac{J_{TUNe} \left(x_{max}\right)}{qv_{TEe}} \right]$$
(1)

where the tunneling current is given by

$$J_{TUNe}(x) = \frac{q \, m_e^*}{2\pi^2 \hbar^3} \int_{E_C(\min)}^{E_C(\max) = \Phi_b} T_{tre}(E_x) \left\{ \int_0^{\infty} \frac{1}{1 + \exp\left(\frac{E_x + E_\perp - E_{fn}}{kT}\right)} - \frac{1}{1 + \exp\left(\frac{E_x + E_\perp}{kT}\right)} dE_\perp \right\} dE_x$$
(2)

and n_{SRH} , n_{IMP} , n_{TUN} denote the virtual concentrations of free carriers, which describe

the contributions of the individual generation-recombination mechanisms:

$$n_{SRH, IMP, TUNe} = \int_{x_m}^{L} \left[\frac{q}{kT \,\mu_n} \exp\left(-\frac{q \,\psi_e}{kT}\right) \int_{x_m}^{x} U_{SRH, IMP, TUNe} \,dx' \right] dx \tag{3}$$

All other symbols have their usual meaning. It can be clearly seen that the tunneling transmission coefficient T_{tr} has a direct impact on the tunneling current and the thermionic emission velocity. The inclusion of tunneling in the model improves the agreement between simulated and experimental *I-V* characteristics significantly; however, some non-negligible discrepancies still remain. Hence, as further enhancement, we additionally take a thin interfacial insulating layer into account by including the tunneling transmission probability T_{tr} through the layer. Employing the Global Matrix Method and splitting the Schrödinger equation over *N* intervals with approximately constant energy values E_i (corresponding to the mean value of the potential barrier $E_c(x)$ in then i-th interval), we arrive at [6]

$$\nabla^2 \Psi_i + k_i^2 \Psi_i = 0 \qquad \text{where} \qquad k_i = \frac{\sqrt{2m_i^* (E_i - E_x)}}{\hbar} \tag{4}$$

For the global transfer matrix, we first determine

$$S_{i} = \frac{1}{2} \begin{bmatrix} 1 + \frac{m_{i-1}^{*}k_{i}}{m_{i}^{*}k_{i-1}} & 1 - \frac{m_{i-1}^{*}k_{i}}{m_{i}^{*}k_{i-1}} \\ 1 - \frac{m_{i-1}^{*}k_{i}}{m_{i}^{*}k_{i-1}} & 1 + \frac{m_{i-1}^{*}k_{i}}{m_{i}^{*}k_{i-1}} \end{bmatrix} \text{ and } P_{i} = \begin{bmatrix} \exp(-k_{i} d_{i}) & 0 \\ 0 & \exp(k_{i} d_{i}) \end{bmatrix}$$
(5)

where S_i is the wave transfer matrix between the intervals i and (i-1) and P_i is the transfer matrix for wave propagation through the potential barrier of thickness d_i . Here it is essential to introduce a voltage-dependent potential barrier height for the interfacial isolation layer (Fig.1). The tunneling transmission coefficient T_{tr} can then be calculated from the global transfer matrix

$$G = P_0 \prod_{i=1}^{N} S_i P_i \qquad => \qquad T_{ir}(E_x) = \frac{k_N}{k_0} \left(g^*_{11} \cdot g_{11} \right)^{-1} \tag{6}$$

The electric charge located at the interface traps reads $\begin{bmatrix} r & r \\ r & r \end{bmatrix}$

$$Q_{interface} = q \int_{E_{v}}^{E_{c}} D_{it}(E) \left[\frac{\exp\left(\frac{E - E_{fn}(x_{m})}{kT}\right)}{1 + \exp\left(\frac{E - E_{fn}(x_{m})}{kT}\right)} \right] dE$$
(7)

where D_{it} is the energy-dependent interface trap density as obtained from experiment.



Fig. 1. Interface trap density D_{it} as experimentally obtained from C-V measurement.

3 Experimental Results and Discussion

The I-V characteristics simulated with this new improved model conform very well with experimental findings. An example is the GaN Schottky diode the characteristics of which is shown in Fig. 2.



Fig. 2. Voltage-dependent potential barrier and I-V characteristics at the Schottky interface.

It is evident that using the simple thermionic emission model as well as the complex model without voltage-dependent potential barrier of the interfacial layer leads to an intolerable discrepancy between simulation and experimental data, whereas the new approach yields excellent agreement.

The *I-V* and *C-V* characteristics for the MOS structures were simulated with the oxide thickness varying from 1.5 nm to 4 nm (Fig. 3).



Fig. 3. Band gap diagram and charge at interface state of simulated MOS structure.

For oxide thickness \geq 3 nm, we observe a behavior of the C-V characteristics typical of MOS structures (Fig. 4) [7]. By decreasing the thickness of the oxide layer below 3 nm the shape of the C-V curves changes significantly in the strong inversion regime, which can be attributed to increasing conductivity due to tunneling and other quantum-mechanical effects. When the thickness of the isolation layer is smaller than 2 nm, the I-V and C-V characteristics attain the shape typical of Schottky structures.



Fig. 4. Simulated C-V and I-V characteristics of MOS structure.

4 Summary

An advanced model of current transport mechanisms through Schottky and MOS structures with very thin interfacial isolation layer has been presented. The introduction of a potential-dependent barrier height in the calculation of the tunneling transmission coefficient from the global transfer matrix improves the agreement between experimental and simulated data significantly.

Acknowledgement

This work was supported by grant VEGA 1/9042/02 of the Slovak Ministry of Education and project APVT-20-013902 of the Science and Technology Assistance Agency.

References

- D. Schröder, Modelling of Interface Current Transport for Device Simulation, Springer - Verlag, Wien, New York, 1994.
- [2] J. R. Tucker, C. Wang and P. S. Carney, Appl. Phys. Lett. 65, 618, 1994.
- [3] K. Matsuzava, K. Uchida and A. Nishiyama, IEEE Trans. Electron. Devices, 47, 103, 2000.
- [4] J. Racko, V. Drobný and D. Donoval, Simulation of Current Transport in Highly Doped Semiconductor Structures Including the Tunneling Effect, Proceedings of the International Conference ASDAM, ed: J. Osvald, Š. Haščík, J. Kuzmík and J. Breza, pp. 35-38, Smolenice, 2000, Slovakia
- [5] J. Racko, P. Kúdela and D. Donoval, Computer Analysis of I-V Characteristics of Pt/Au-GaN Schottky Contacts Including Tunneling Current Flow Mechanism through Thin Interfacial Isolation Layer, Proceedings of the International Conference WOCSDICE, Smolenice, 2004, Slovakia
- [6] R. Redhammer and F. Urban, Wave Reflection Analysis of a Quasibound State Using a Global Transfer Matrix, phys. Stat. sol. (b) 182, 1994
- [7] A. Ghetti et al., Characterization of tunneling current in ultra-thin gate oxide, Solid-State Electronics 44, 1523 -1531, 2000