Simulation of the Cross-Coupling among Snap Back Devices under Transient High Current Stress

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Abstract

A main issue for on-chip protection of Smart Power ICs against ESD and other transient high current pulses is the cross-coupling between the protection device (PD) and the device to be protected. In many cases both are npn transistors (e.g. parasitic of DMOS), therefore we investigate the coupled triggering of such devices by numerical device simulations. We show that even considering the separate transient trigger voltages V_{tr} does not guarantee protective action. Under certain conditions, even though the PD shows a lower V_{tr} than the circuit and it conducts the current in the beginning of the pulse, the circuit device takes over the stress current, possibly being destroyed. This explains observations of low ESD robustness and enables design measures.

1 Introduction

In the design of Smart Power ICs, especially for automotive applications, it is necessary to guarantee a sufficient robustness against a large diversity of different, high current stress pulses. Besides standard ESD tests [1], which are applied to every electronic circuit, tests with even higher transient currents [2] are increasingly required for those ICs. Furthermore, the limits of the technologies are pushed towards the IC's voltage specifications. Robustness has to be ensured for the combination of protection devices (PDs) and related circuits under all required conditions.

Thus, apart from providing PDs that are robust themselves, the main issue for a successful protection scheme is a correct interplay between the PD and the circuit to be protected. It has to be ensured, that under all stress conditions the PD discharges the current, at least enough not to destroy the circuit. Those tests are time consuming and happen in a very late phase of a design project; therefore reliable TCAD investigations are important [3] to minimize costs and time to market.

Up to now, DC and pulsed current-voltage (IV) characteristics of the PD and the relevant circuit devices are regarded as the most important properties to be considered. Many investigations have been published to understand and predict the properties of single devices under transient high current stress (see e.g. [4] to [7]). The usual approach [8] for protecting a circuit is to ensure that the trigger voltage V_{tr} of the PD is lower than V_{tr} of the circuit. Generally, the transient V_{tr} of the single devices have to be considered [9]. This approach is based on the assumption, that in this case the PD will take over the total stress current - also in combination with the circuit.

In some few HBM stress tests however, we observe a low robustness due to circuit destruction, even though the PD has a 15V lower V_{tr} than the circuit (not shown).

To understand this effect and to be able to derive design measures, we investigate the coupled behavior of two parallel npn transistors, representing the PD and the circuit being stressed by a current pulse, by means of numerical device simulation.

2 Devices under Investigation

For the numerical investigations we choose simplified npn transistors, which represent the PD and the circuit to be protected (e.g. parasitic npn of a DMOS transistor). They are connected in parallel, with the collectors exposed to a transient current source and all base and emitter pins grounded (see fig. 1).

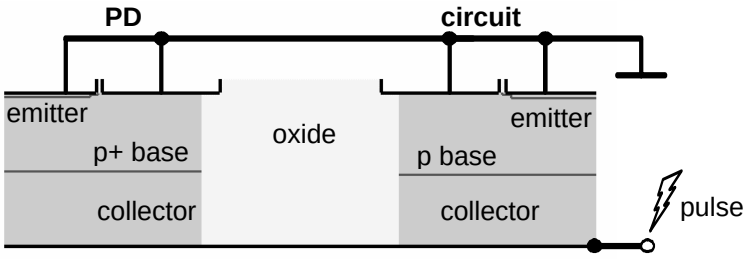

Fig. 1: Simulation structure. The PD (left) and the relevant device or parasitic of the circuit (right) are isolated by a dielectric region to avoid mixed mode simulation.

Mixed mode simulation was avoided here by isolating the devices by a dielectric trench. The PD (left device) has a highly doped, deep p-base, the circuit device (right) a lower doped base leading to about 16V higher breakdown and DC trigger voltages.

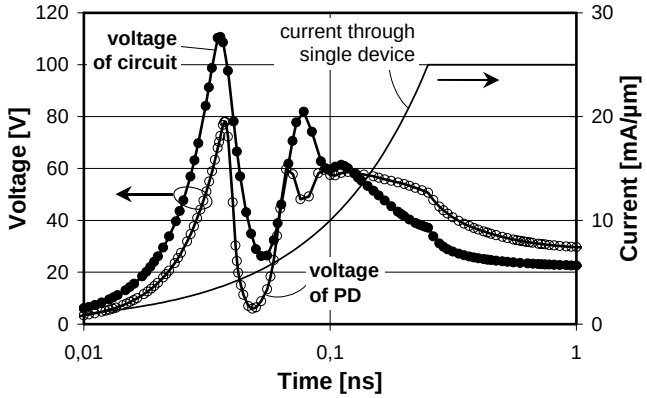

Fig. 2: Transient voltage across the single devices. Forced current I=25mA/µm with slope dI/dt = 100mA/(ns µm). The PD triggers lower and limits the voltage better than the circuit device, at least up to 0.13ns. This situation is commonly regarded as safe.

3 Results and Discussion

First, we simulate the DC characteristics and transient voltage response of the single devices (see fig. 2), i.e. on structures containing only either the PD or the circuit device. The DC-characteristics (not shown) reveal an about 16 V lower trigger voltage V_{tr} for the PD (39V instead of 55V). Also in the transient case (see fig. 2), the voltage

across the PD, V_{PD}, is clearly lower than the one across the circuit device, V_C, at least for times t<0.13 ns. Thus the first assumption would be that the PD will take over the current of the pulse also in the coupled case, and the circuit will be protected properly.

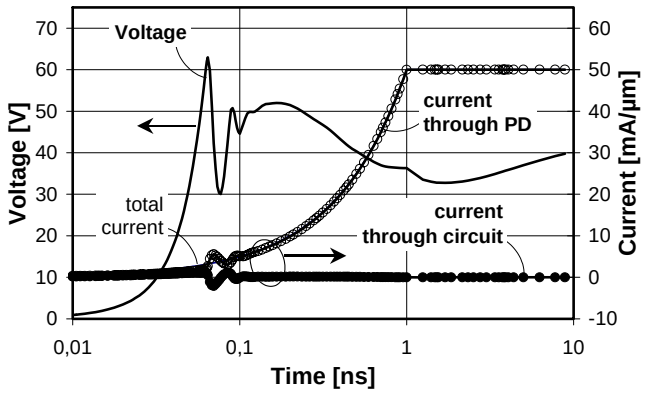

Fig. 3: Transient response from the electrically coupled devices. Forced current I=50mA/µm with slope dI/dt = 50mA/(ns µm). The PD carries the total current and limits the voltage, as expected from the DC characteristics (fig. 2).

In a second step we investigate the transient response of the coupled configuration from fig. 1 for different currents I and current slopes dI/dt. Fig. 3 shows the results after forcing I=50mA/µm with dI/dt=50mA/(ns µm). As can be seen, the PD carries all the current and limits the voltage to about 33V after 2ns (before the voltage rises due to self heating). This is the desired case and what could be expected from fig. 2.

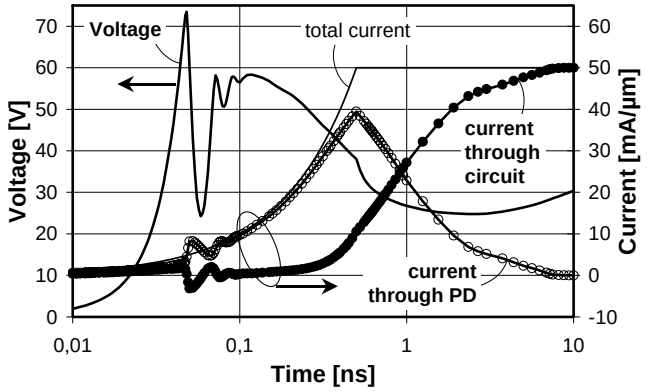

Fig. 4: Transient response from the electrically coupled devices. Forced current I=50mA/µm with slope dI/dt = 100 mA/(ns µm). The PD carries the current in the beginning, as in fig 3. But after about 0.3 ns the circuit device starts operating as well, and after 8 ns it carries the entire current . In reality this would lead to circuit failure even though the single PD starts to trigger well below the circuit to be protected.

However, the situation changes totally if we apply a similar pulse of double slope, dI/dt=100mA/(ns µm) (see fig. 4): though one can clearly see the current onset in the PD, the circuit device starts to operate after about 0.3 ns and for t>0.7 ns the main current flows through the circuit device. This switching is caused by a small base current from charges remaining in the circuit device after the decay of the avalanche-driven space-charge oscillations between 50 and 100 ps. That current slowly increases and finally activates the circuit npn which takes over the complete current.
Thus not only breakdown and trigger voltage (DC or transient) determine which of the devices carries the stress, because stored charges may cause a current redistribution among the coupled devices. An extended variation of system parameters shows that besides the base resistance controlling the trigger currents of the competing structures, the base profiles, controlling the bipolar gain and base transit time, play a decisive role for the coupled triggering. On the other hand, the possible final current distribution among the devices is affected by their individual IV-characteristics. In our case, one of the devices takes over the total stress current, other cases were simulated, where the devices share the current more or less equally in the end.
Because the parameters of the circuit devices are constrained by technology / application requirements, it is very important to understand the mechanisms of coupled triggering in more detail to deduce safe and feasible design measures. An actual design study additionally has to consider filamentation for timing [9] and robustness [7],[10].

4 Conclusion

As an important situation for the protection of ICs against high current disturbances, coupled triggering of two parallel npn transistors under transient high current stress is investigated by numerical device simulation. We demonstrate that it is not sufficient to consider the triggering behavior of the single devices. After increasing the slope of the forced current from 50 mA/(ns µm) to 100 mA/(ns µm), the behavior of the coupled devices is observed to change totally. Whereas for the slower current ramp only the protection device (PD) conducts, for the faster slope this is only the case until about 300 ps, when the circuit transistor is triggered by a transient base current and increasingly takes over the entire current. This explains experimental tests where a circuit was destroyed by fast pulses, even though the PD had a 15V lower triggering voltage than the circuit to be protected.

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