Very High Performance, Sub-20nm, Strained Si and $Si_x Ge_{1-x}$, Hetero-structure, Center Channel (CC) NMOS and PMOS DGFETs

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Abstract

We present novel, very high performance, NMOS and PMOS strained-Si and $Si_xGe_{(1-x)}$ heterostructure DGFETs suitable for scaling to sub-20nm dimensions. 1-D Poisson-Schrodinger simulations show that the devices exhibit Center-Channel (CC) operation. Full-Band Monte Carlo simulations show a ~50% increase in drive currents and ~2X increase in switching speeds at lower capacitance compared to conventional Si DGFETs. The cut-off frequencies for the devices are in the terahertz regime, making the device also well suited for analog applications.

1 Introduction

In order to enhance performance and continue scaling MOSFETs to the sub-20nm regime, novel, high-mobility materials like Si_xGe_{1-x} [1] and strained-Si [2] are actively being incorporated into the channel. However, due to the aggressive scaling requirements of ultra-thin bodies [3], high E-fields in the channel [4] and introduction of high-k dielectrics [5], the channel mobility is severely degraded. In this paper we introduce un-doped, Center Channel (CC) NMOS and PMOS FETs that incorporate novel transport principles, which fully exploit the advantage of high mobility materials. 1-D Poisson-Schrodinger [6] and Full-Band Monte-Carlo simulations [7] demonstrate that the CCFET exhibits very high performance due to its excellent transport and electrostatic properties.

2 Device Structure and Operation

Unlike a conventional DGFET with two surface channels, in the CCFET, the carriers are confined to the center of the channel, by means of a quantum well created by band offsets. As shown in Fig.1, the NMOS needs a band offset in the conduction band while the PMOS needs a band offset in the valence band. Fig.2 shows that a Si_xGe_{1-x}/strained-Si/Si_xGe_{1-x} heterostructure sandwich for the NMOS and a Si/ Si_xGe_{1-x} /Si structure for the PMOS can be used to realize these devices. As shown in Fig.3, 1-D Poisson-Schrodinger simulations demonstrate that confining the wavefunction to the center of the channel has several advantages even in the case of a conventional doped DGFET operated in the Depletion Mode (DM) [8,9]. The zero E-field in the center of the channel implies that the carriers do not suffer scattering due to surface roughness at the high-k interface and the high vertical E-field. Consequently, these devices exhibit very high mobility and allow for easier technology integration.

Further, since the carriers are away from the interface, they also show lower gate leakage. Fig.4 shows that due to the superior electrostatics of a DG structure, the center channel DMDG FET shows excellent sub-threshold characteristics and short channel effects, comparable to a conventional DGFET.

Previous work has demonstrated very high performance, center-channel, doped PMOS DGFETs operating in the Depletion Mode (DM) [8]. From a practical standpoint, introducing dopants into the channel creates problems like random dopant induced fluctuations in very small devices [10] and reduction of carrier mobility due to impurity scattering. In this paper, we present undoped, heterostructure CC NMOS and PMOS FETs which do not suffer from this problem. They utilize a quantum well created by band offsets to confine the carriers in the center of the channel. An optimum surface barrier layer thickness ensures a center-channel (volume inverted) operation for all gate voltages. The addition of a high mobility un-doped material like Si_xGe_{1-x} or strained Si layer in the center of the channel further enhances the carrier mobility.

3 Full-band Monte-Carlo Simulations

In the case of an un-doped heterostructure CCFET, which uses a quantum well for carrier confinement, one concern is the possibility of creating a second low-mobility surface channel at higher gate voltages. In order to confirm that the devices do not suffer from this problem, we have compared the undoped CCFETs with CCFETs that have their surface barrier layers doped (n+ doped Si_xGe_{1-x} for NMOS and p+ doped Si for PMOS) to raise their threshold voltage and prevent any surface inversion. Fig.5(a) shows that the undoped conventional Si DG NFET shows the lowest potential at the surface and the strongest band-bending. As expected, the undoped CC NFET shows a stronger band-bending than the doped CC NFET. However, the lowest potential is still in the quantum well and the surface is not inverted in the ON state. There is an optimum surface barrier layer thickness [11]. Making the barrier too thick increases the potential drop at the surface and causes surface inversion. Making the barrier too thin does not sufficiently confine the carriers. The wavefunction can then penetrate through the surface barrier layer and interacts with the dielectric interface, thus reducing the carrier mobility.

Fig.6 shows that the backscattering coefficient for the DGFET compared to the CCFET is ~90% higher for the NFET and ~40% for the PFET. Fig.7 shows that the injection velocity of the carriers in the CCFET is ~50% higher than a conventional DGFET for both the NMOS and the PMOS. The extremely high channel mobility and excellent transport properties of the device make the CCFET nearly ballistic. Since the channel in the CCFET is formed further away from the surface, it leads to a lower capacitance and consequently a lower channel charge. Fig.8 shows that the gate capacitance is ~10% lower for the NMOS and ~15% for the PMOS. The almost overlapping curves in the doped and un-doped CCFETs show that we do indeed have a center channel operation (volume inversion) even at high voltages in the undoped device. We find that the drive current in the CC NFET is ~55% higher than a conventional Si DG NFET and ~45% higher in the case of the PMOS (Fig.9). The higher drive currents and lower capacitance leads to very high intrinsic switching speeds (~2X higher for both NMOS and PMOS) and very high cut-off frequencies. As shown in Fig.10, the peak cut-off frequency for the CC NMOS is ~2000 GHz and ~1000 GHz for the CC PMOS.

4 Conclusion

In summary, we present novel, very high performance, CC NMOS and PMOS FETs suitable for scaling to sub-20nm dimensions. 1-D Poisson Schrodinger simulations verify that carriers are quantum mechanically confined to a very low E-field region in the center of the DG structure, leading to very high channel mobility. Full-Band Monte Carlo simulations show a ~50% increase in drive currents and ~2X increase in switching speeds at lower capacitance compared to conventional Si DGFETs. The cut-off frequencies for the devices are in the terahertz regime, making the device also well suited for analog applications.

References

[1] T. Tezuka et al, IEEE TED, May 2003, vol.50, no.5, p.1328-1333
[2] K. Rim et al, IEDM, Dec. 2003, p.3.1.1-4
[3] K. Uchida et al, IEDM, Dec. 2003, p.33.5.1-4
[4] S. Takagi, Short Course, IEDM, Dec. 2003
[5] M. Fischetti et al, JAP, Nov. 2001, vol.90, no.9, p.4587-608
[6] Schred-2.0, Nanohub-Purdue University
[7] C. Jungemann et al, Springer-Verlag, 2003
[8] T. Krishnamohan et al, IEDM, Dec. 2003, p.29.3.1-4
[9] T. Krishnamohan et al, SISPAD, Sept. 2003, p. 243-6
[10] A. Asenov et al, IEEE TED, Apr. 2001, vol.48, no.4, p.722-9
[11] M. Lee et al, IEDM, Dec. 2003, p.18.1.1-4

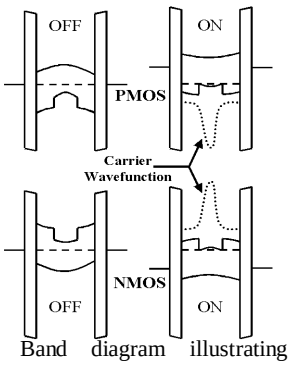

Fig.1 Band diagram illustrating the operation of the CC NMOS and PMOS

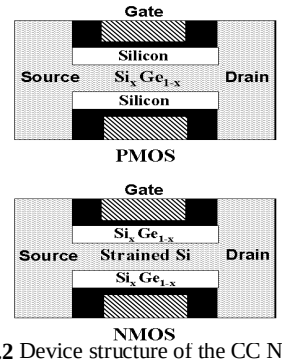

Fig.2 Device structure of the CC NMOS and PMOS

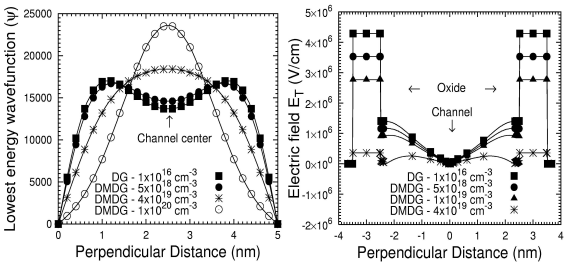

Fig.3 Electron wavefunction (left) and E-field (right) in a center-channel NMOS

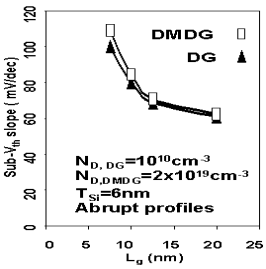

Fig.4 Sub-threshold slopes for conventional and CC DGMOS

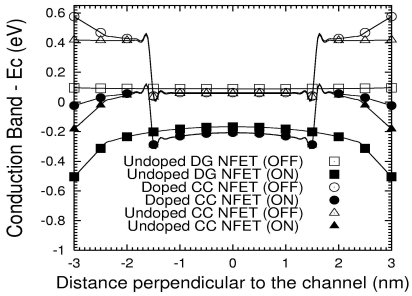

Fig.5 (a) Conduction band profile for the DG and CC (doped and undoped) NFETs

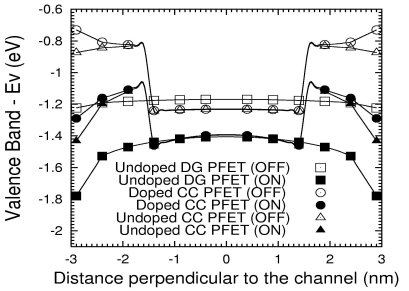

Fig.5 (b) Valence band profile for the DG and CC (doped and undoped) PFETs

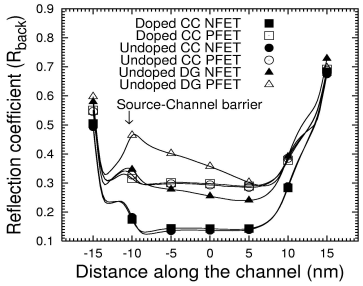

Fig.6 Backscattering coefficients for the DG and CC (doped and undoped) FETs

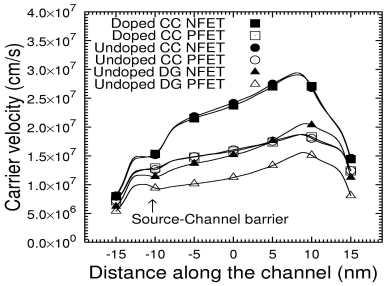

Fig.7 Carrier velocity along the channel for the DG and CC (doped and undoped) FETs

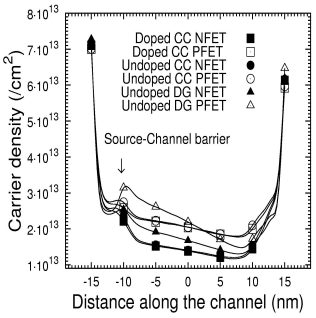

Fig.8 Carrier density along the channel for the DG and CC (doped and undoped) FETs

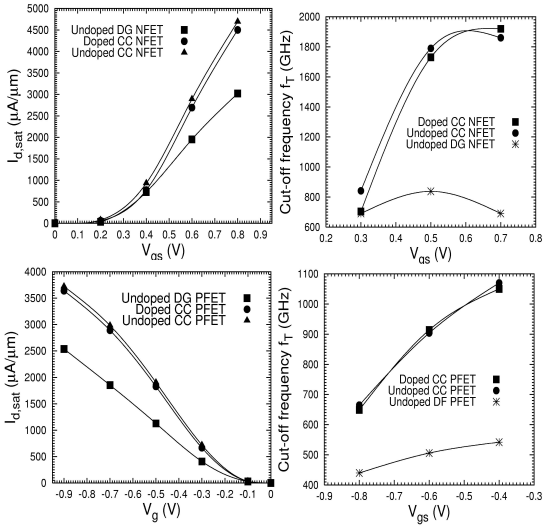

Fig.9 Drive currents for the DG and CC (doped and undoped) NFETs and PFETs

Fig.10 Cut-off frequencies (quasistatic approximation) for the DG and CC (doped and undoped) NFETs and PFETs